

1/3, 1/4 Duty LCD Driver

■ GENERAL DESCRIPTION

NJU6532 is a 1/3 or 1/4 duty segment type LCD driver. It incorporates 4 common driver circuits and 32 segment driver circuits. NJU6532 can drive maximum 96(84)* segments in 1/3 duty ratio and maximum 128(112)* segments in 1/4 duty ratio.

In addition, the NJU6532's useful functions and small package meet a wide range of applications.

■ PACKAGE OUTLINE



NJU6532FR3

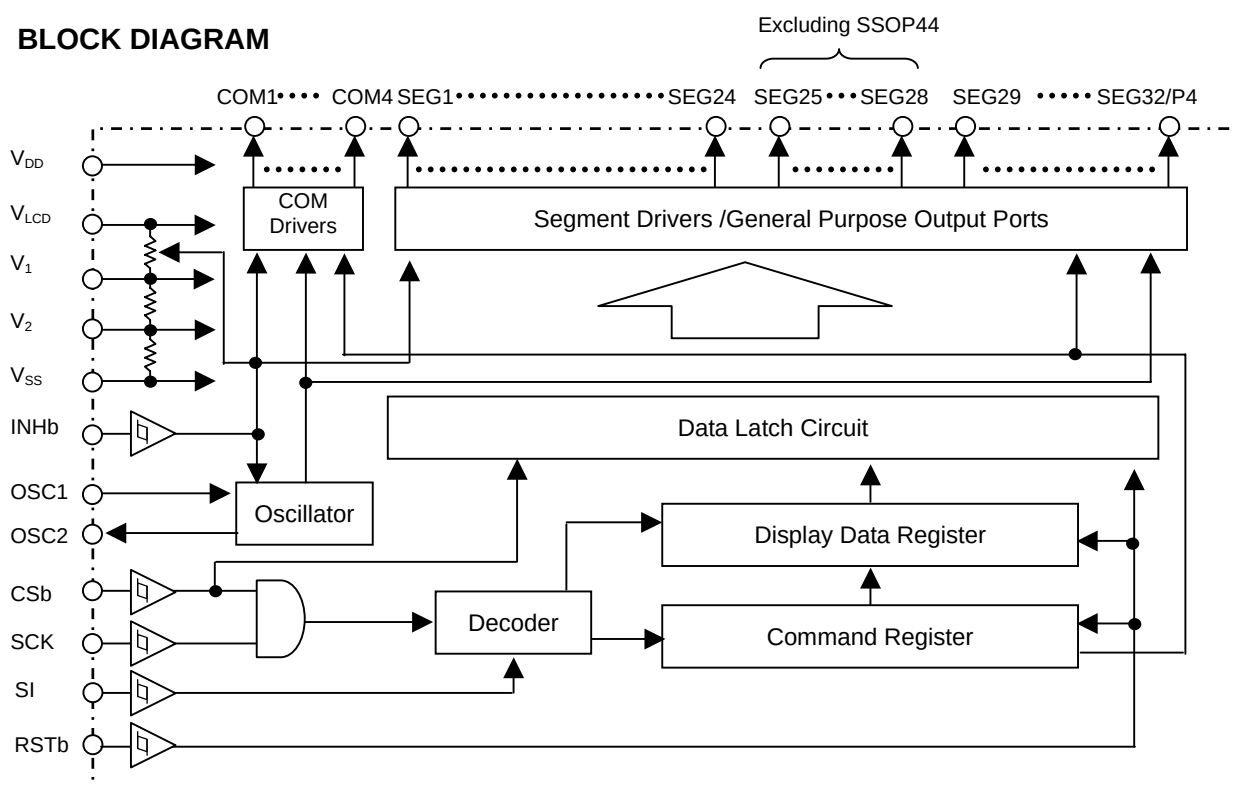


NJU6532V

■ FEATURES

- LCD driving circuit :Max. 32outputs (SSOP44: Max. 28outputs) (4 outputs as for general purpose ports)
- Programmable Duty Ratio
 - 1/3 duty ratio :Driving max. 96 segments (SSOP44:Driving max. 84 segments)
 - 1/4 duty ratio :Driving max. 128 segments (SSOP44:Driving max. 112 segments)
- Programmable Bias Ratio :1/2, 1/3 bias ratio
- Serial Data Transfer :Shift clock max. 2MHz
- Built-in Oscillator :CR oscillation with external resistor, or external oscillation signal input
- Display OFF :INHb terminal
- Operating Voltage :2.7 to 5.5V
- LCD Driving Voltage :Vdd to 8.0V
- C-MOS Technology :P-Sub
- Package Outline :SSOP44, LQFP48-R3

■ BLOCK DIAGRAM

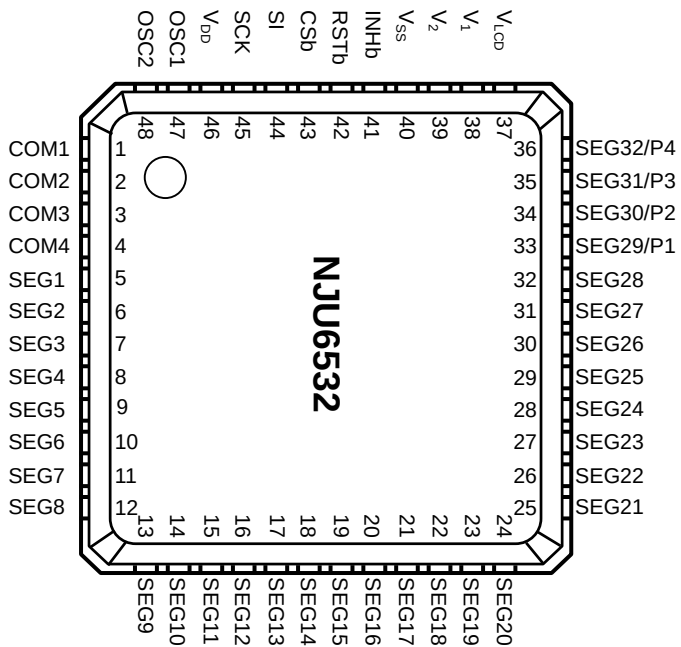


NJU6532

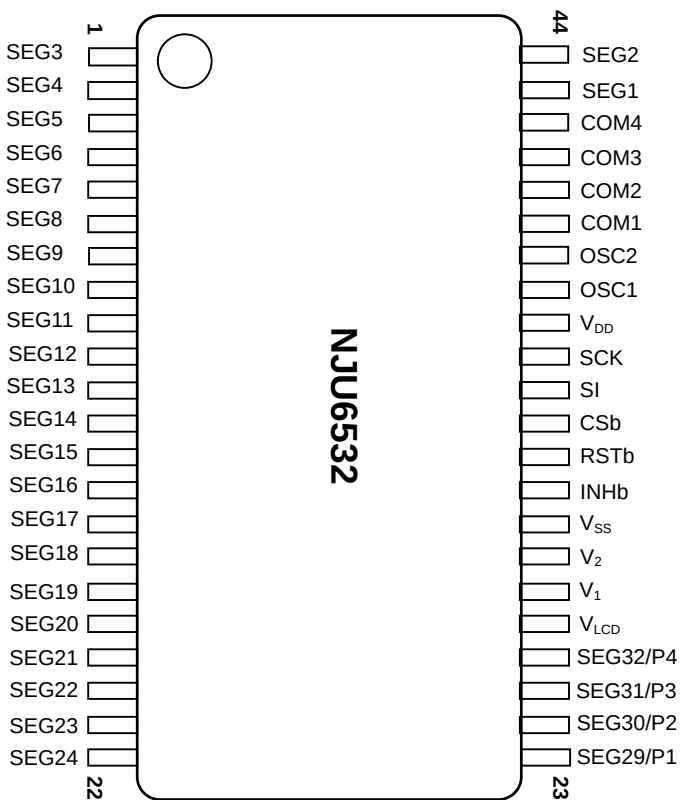
Preliminary

PIN CONFIGURATION

• LQFP48-R3



• SSOP44



■ TERMINAL DISCRIPTION

No.		Terminal	Function
LQFP48-R3	SSOP44		
46	36	V _{DD}	Power supply: 3V /5V
37	27	V _{LCD}	LCD driving voltage $V_{LCD} \geq V_1 \geq V_2 \geq V_{SS}$, $V_{LCD} \geq V_{DD}$
38, 39	28, 29	V ₁ , V ₂	Bias At 1/3 bias ratio, keep V ₁ - V ₂ open. At 1/2 bias ratio, short V ₁ - V ₂ .
40	30	V _{SS}	GND V _{SS} =0V
41	31	INHb	Display OFF * When INHb is "H", display is ON, and when INHb is "L", display is off. When SEG29(P1)~SEG32 (P4) are selected as general purpose output ports, even if input "0" to INHb terminal, SEG29~32 will still be recognized as general purpose output ports.
42	32	RSTb	Reset When RSTb is "L", command register and latch circuit is reset.
43	33	CSb	Chip select When CSb is "L", data can be read in.
44	34	SI	Serial data input (8 bit=1word)
45	35	SCK	Serial clock
47, 48	37, 38	OSC1, OSC2	External resistor connection terminal for CR oscillation, or external clock input terminal When external clock is used, input the signal to OSC1 and keep OSC2 open.
1~4	39~42	COM1 ~ COM4	Common driver outputs
5~28	43~44 1~22	SEG1 ~ SEG24	Segment driver outputs
29~32	-	SEG25 ~ SEG28	Segment driver outputs (Excluding SSOP44)
33~36	23~26	SEG29/P1 ~ SEG32/P4	Segment driver outputs/general purpose output ports These 4 terminals can be used as segment outputs or general purpose output ports by setting Command Register. When selected as general purpose ports, data can be outputted via these ports during COM1 timing. According to transferred data, "H"=V _{DD} or "L"=V _{SS} will be outputted.

*: For details about INHb, please refer to "7 FUNCTION DESCRIPTION (5) Display OFF function (INHb terminal)".

■ FUNCTION DESCRIPTION

(1) Block Function

(1-1) Oscillator

The oscillator includes a built-in capacitor and an external resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC1 and keep OSC2 open.

(1-2) Decoder

Input serial data is decoded and sent to the appropriate block.

(1-3) Command Register

Command data is written to this 8 bits command register to control **NJU6532** operation.

(1-4) Display Data Register

Data is written to this 8 bits register as display data.

(1-5) Latch Circuit

Data stored in display data register is assigned to the corresponding SEG/port.

(1-6) Segment Driver/General Purpose Ports

Basing on display data, segment drivers output LCD SEG driving signal.

And, SEG29/P1 ~ SEG32/P4 terminals can be selected as segment driver output or general-purpose ports by instruction.

(1-7) Common Driver

Common drivers output LCD COM driving signal.

(1-8) Reset Circuit

When RSTb="L", **NJU6532** is initialized.

(2) Serial data Transfer

The transfer of data is conducted by synchronizing clock via interface with CPU. During CSb="L", serial data is obtainable and will be write in at the rising edge of SCK signal. The data is latched at falling edge of the CSb signal condition.

After CSb becoming low, address or command data is distinguished by the first 8bit data.

In the case of address data, the 2nd data can be transferred continually and interrupted as display data even if CSb maintained low.

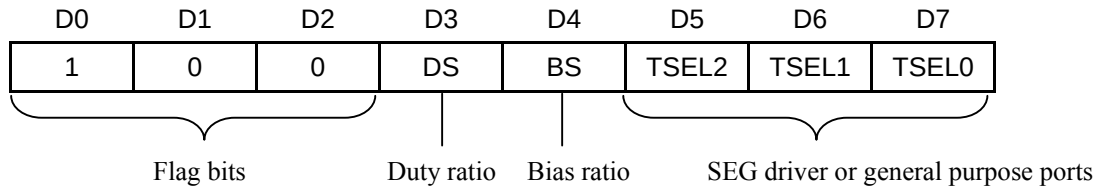
(3) Command Register

Command Register is used to set the duty ratio, the bias ratio, and the SEG driver/general purpose ports. When the D0 to D2 bits of the 1st word are (1,0,0), the D3 ~ D7 bits are recognized as command data.

The contents of Command Register will be initialized as following when applying input signal to Reset terminal.

The Default Value of Command Register

- Duty ratio : 1/4
- Bias ratio : 1/3
- SEG driver/General purpose ports : SEG drivers(SEG32, SEG31, SEG30, SEG29)



• Duty Ratio

DS	Duty ratio
0	1/4
1	1/3

*) Do not change the duty ratio during display ON.

• Bias ratio

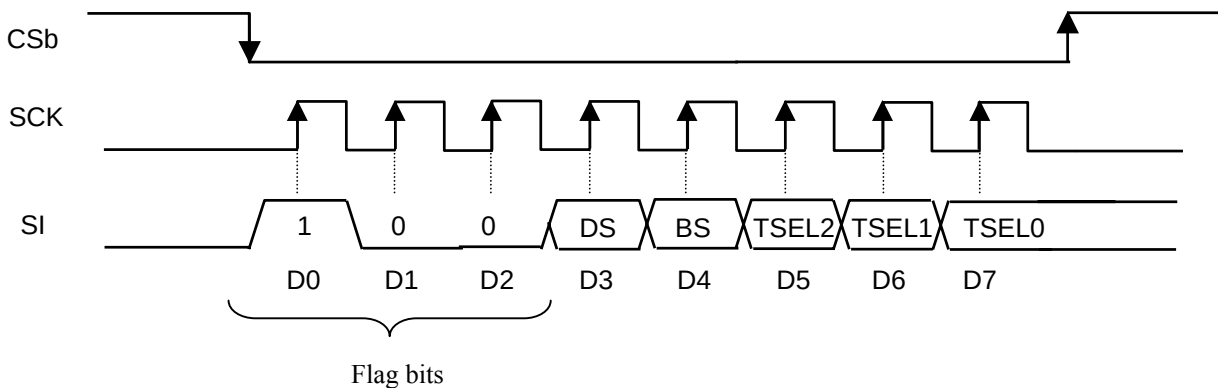
BS	Bias ratio
0	1/3
1	1/2

• SEG driver or general purpose ports

TSEL2	TSEL1	TSEL0	SEG29/P1	SEG30/P2	SEG31/P3	SEG32/P4
0	0	0	SEG29	SEG30	SEG31	SEG32
0	0	1	SEG29	SEG30	SEG31	P4
0	1	0	SEG29	SEG30	P3	P4
0	1	1	SEG29	P2	P3	P4
1	0	0	P1	P2	P3	P4

**) If TSEL2 ~ TSEL0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

Timing of Serial Data Transfer



(4) Shift Register Select

Output Address Counter will specify the addresses of the SEG and COM drivers for the display data.

When the 8bits (D0 to D3, D6, D7) of the 1st data is “011100”, the 8bits (D4, D5) specify the address of COM drivers, and after the 2nd data is display data which will be sent to the 1st-data –specified drivers.

• Address Data

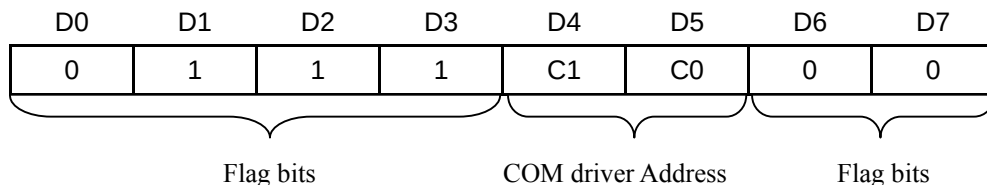


Table 1. The Relationship Between Output Address and SEG/COM Drivers

Increment Direction	C1	C0	COM Driver	SEG Driver							
	0	0	COM1	D8	D9	D10	D11	D12	D13	D14	D15
				SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
				D16	D17	D18	D19	D20	D21	D22	D23
				SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
				D24	D25	D26	D27	D28	D29	D30	D31
				SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
				D32	D33	D34	D35	D36	D37	D38	D39
				SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
	0	1	COM2	D8	D9	D10	D11	D12	D13	D14	D15
				SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
				D16	D17	D18	D19	D20	D21	D22	D23
				SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
				D24	D25	D26	D27	D28	D29	D30	D31
				SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
				D32	D33	D34	D35	D36	D37	D38	D39
				SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
	1	0	COM3	D8	D9	D10	D11	D12	D13	D14	D15
				SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
				D16	D17	D18	D19	D20	D21	D22	D23
				SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
				D24	D25	D26	D27	D28	D29	D30	D31
				SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
				D32	D33	D34	D35	D36	D37	D38	D39
				SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
	1	1	COM4	D8	D9	D10	D11	D12	D13	D14	D15
				SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
				D16	D17	D18	D19	D20	D21	D22	D23
				SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
				D24	D25	D26	D27	D28	D29	D30	D31
				SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
				D32	D33	D34	D35	D36	D37	D38	D39
				SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32

- ✧ If general purpose ports are selected by Command Register, under (C1, C0)=(0, 0), D36 to D39 are the addresses of (P1, P2, P3, P4) ports which corresponds to (SEG29, SEG30, SEG31, SEG32).
- ✧ When SEG29~SEG32 are set as general purpose output ports, data for SEG29~SEG32 during COM2~COM4 scanning will be ignored.
- ✧ When duty ratio is 1/3, do not set address (C1, C0)=(1,1).
Set to address (C1, C0)=(1,1), It is not reflected in the display.