16-SEGMENT X 14-Digit VFD CONTROLLER / DRIVER

■ GENERAL DESCRIPTION

The **NJU3426** is a VFD (Vacuum Fluorescent Display) controller/driver to dynamically drive up to 16 segments x 14 digits. It consists of display data RAM, an address counter, command registers, a serial interface and high voltage drivers. The NJU3426 features the direct connection to MPU and the high voltage drivers of 45V well-suited for various VFD displays.

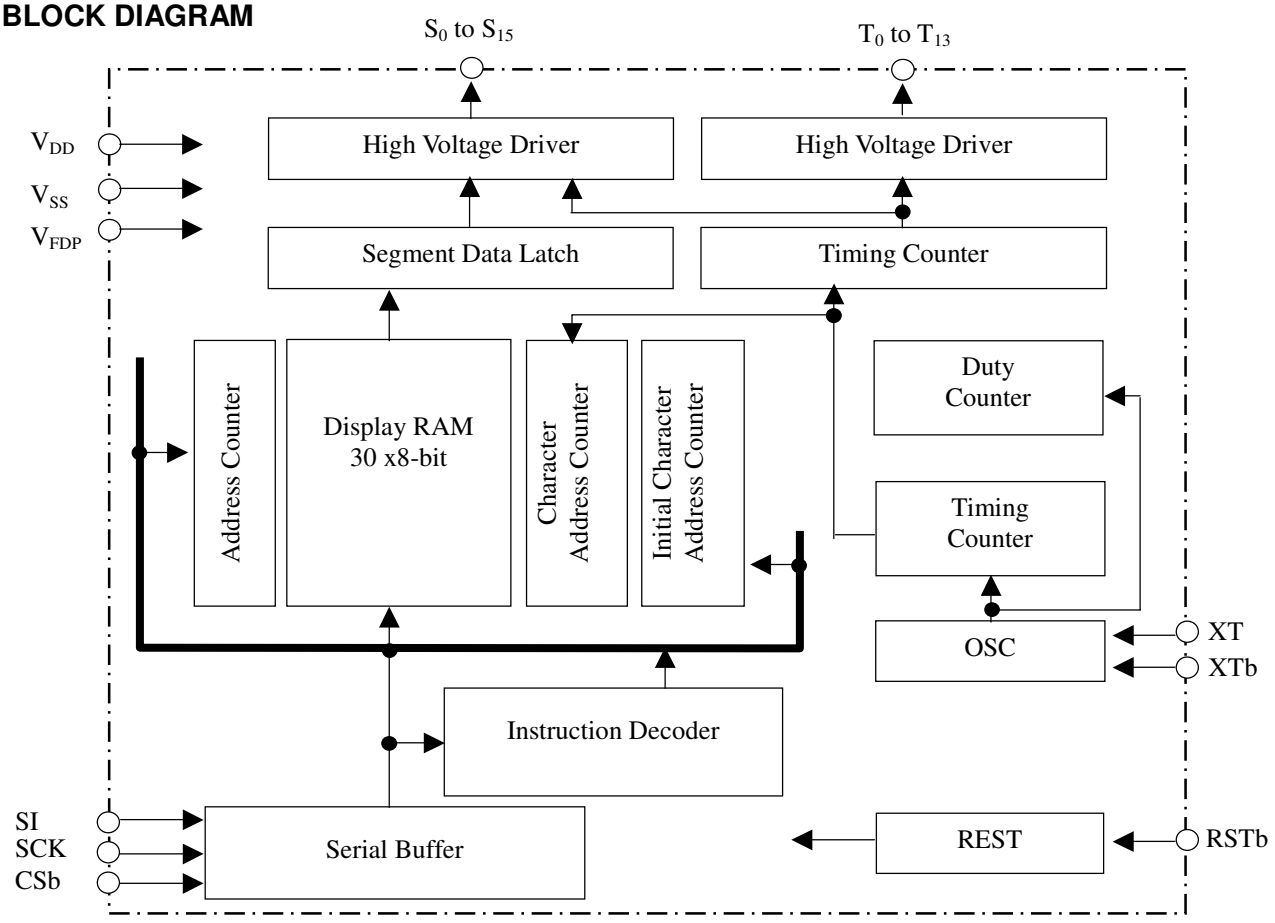
■ PACKAGE OUTLINE

NJU3426FP1

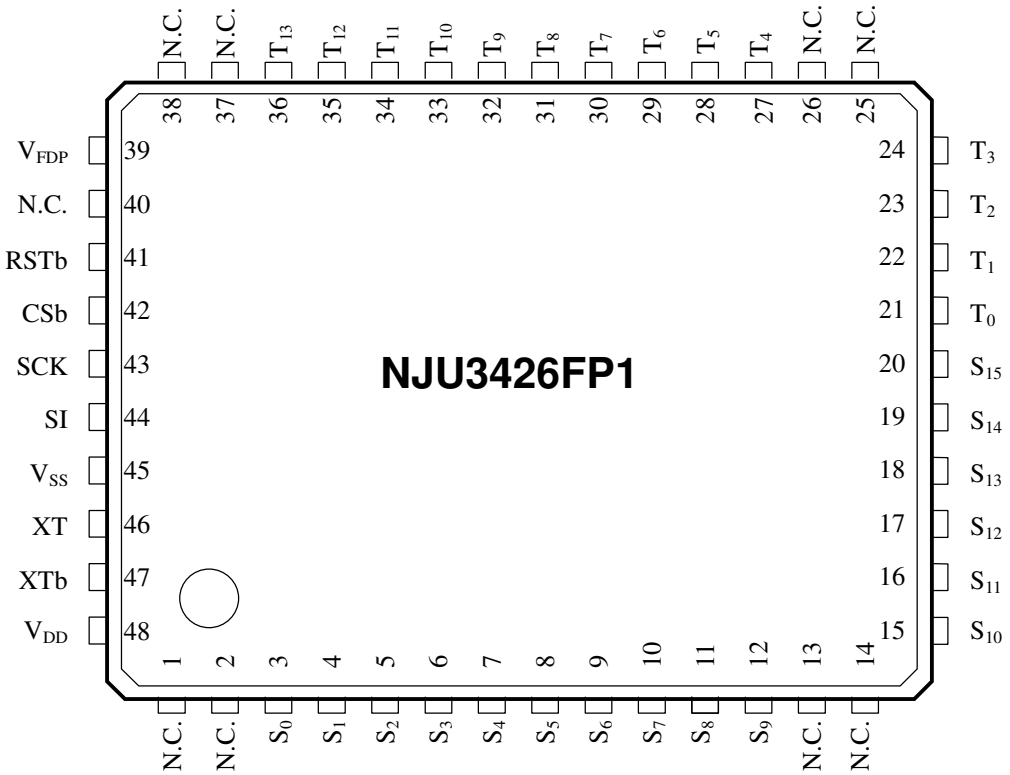
■ FEATURES

- Directly Drives 16-segment x 14-digit
- High VFD Driving Voltage : $|V_{DD}-V_{FDP}| \leq 45V$
- Display Shift Function
- Programmable Duty Ratio for Timing Signal
  :2/16, 4/16, 6/16, 8/16, 10/16, 12/16, 14/16, 15/16 duty
- Display ON/OFF Control Function
- Display Data RAM : 30 x 8-bit
- Built-in Oscillator (External Ceramic Resonator or External Resistor or External Clock)
- 8-bit Serial Interface
- Power-ON Reset Function
- Operating Voltage : 3.3V / 5.0V
- C-MOS Technology
- Package Outline :QFP48-P1

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DISCRIPTION

PAD No.	SYMBOL	FUNCTION
48	V_{DD}	Power Supply For Logic Voltage 3.3V / 5.0V
45	V_{SS}	Ground V_{SS}=0V
39	V_{FDP}	Power Supply For VFD Driving Voltage
46 47	XT XTb	Ceramic Resonator Connection, Resistor Connection, or External Clock Input The internal oscillator is formed by connecting an external ceramic resonator to these pins. When an external oscillator is used instead of the internal oscillator, the external clock is input to the XT and the XTb must be open.
3 to 12, 15 to 20	S_0 to S_{15}	Segment output terminals (Pulled down)
21 to 24, 27 to 36	T_0 to T_{13}	Timing output terminals (Pulled down)
41	RSTb	Reset terminal (Pulled up) Active “L”: Reset is executed when this pin is “L”. Reset does not change the contents of display data RAM.
42	CSb	Chip Select Active “L”: Data transmission is enable when this pin is ”L”.
43	SCK	Serial Clock Input
44	SI	Serial Data Input (8 bits = 1 word)
1, 2, 13, 14, 25, 26, 37, 38, 40	N.C.	Non connections These pins must be open.

■ FUNCTION DESCRIPTION

(1) ADDRESS COUNTER

The address counter specifies the "Display data RAM address", and the display data is transferred to or from this address. For the data transmission, once an initial RAM address is determined, the display data can be continuously transmitted without setting the RAM address. When the upper 2 bits (B7 and B6) of the 1st word are "0,0", the lower 5 bits (B4 to B0) are interpreted as RAM address data. And the 2nd word is interpreted as display data which is stored in the RAM address specified by the 1st word, and simultaneously the RAM address is counted up.

Although the "Display data RAM address" can be set only in the range of "0,0,0,0,0" (00_H) and "1,1,1,0,1" ($1D_H$), the auto-increment keeps counting up to "1,1,1,1,1" ($1F_H$), and the RAM address finally wraps to "0,0,0,0,0" (00_H) then begins counting up. Note that the display data, specified to the RAM address of "1,1,1,1,0" ($1E_H$) or "1,1,1,1,1" ($1F_H$), is ignored in this sequence.

DISPLAY DATA RAM ADDRESS

B7	B6	B5	B4	B3	B2	B1	B0
0	0	*	AD4	AD3	AD2	AD1	AD0

Recognition data — Display data RAM address

*:don't care

Character address		B7	B6	B5	B4	B3	B2	B1	B0	RAM Address	B7	B6	B5	B4	B3	B2	B1	B0	RAM Address
	C_0									01_H									00_H
T_0	C_1									03_H									02_H
T_1	C_2									05_H									04_H
T_2	C_3									07_H									06_H
T_3	C_4									09_H									08_H
T_4	C_5									$0B_H$									$0A_H$
T_5	C_6									$0D_H$									$0C_H$
T_6	C_7									$0F_H$									$0E_H$
T_7	C_8									11_H									10_H
T_8	C_9									13_H									12_H
T_9	C_{10}									15_H									14_H
T_{10}	C_{11}									17_H									16_H
T_{11}	C_{12}									19_H									18_H
T_{12}	C_{13}									$1B_H$									$1A_H$
T_{13}	C_{14}									$1D_H$									$1C_H$
										$1F_H$									$1E_H$
		S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8		S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	

: Non-existent Address

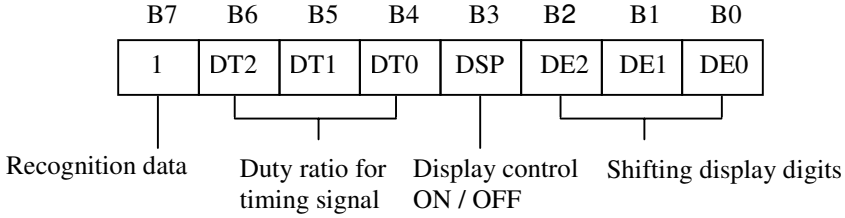
DISPLAY DATA RAM MAP

(2) COMMAND REGISTER 1

The "Command register 1" is used for setting "Duty ratio for timing signal", "Display control ON/OFF" and "Shifting display digits". When the upper 1 bit (B7) of the 1st word is "1", the lower 7 bits (B6 to B0) are interpreted as command data, and stored in the "Command register 1". The contents of the "Command register 1" are initialized to the default values by the power-ON reset or the reset signal, as shown below.

DEFAULT VALUES OF COMMAND REGISTER 1

- Duty ratio for timing signal : 2/16
- Display control ON/OFF : OFF
- Shifting display digits : 7



DT2	DT1	DT0	Duty ratio for timing signal
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

Note.) The output waveforms of timing signal are shown in "■ **TIMING SIGNAL / DUTY-CHANGE WAVEFORM**".

DSP	Display control
0	OFF
1	ON

Note.) When the "Display control OFF" is set, segment drivers output waveforms but all timing signal outputs are halted

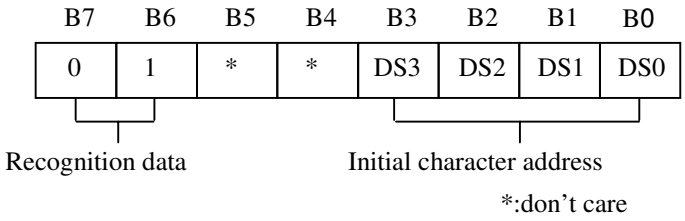
DE2	DE1	DE0	Shifting display digits
0	0	0	7
0	0	1	8
0	1	0	9
0	1	1	10
1	0	0	11
1	0	1	12
1	1	0	13
1	1	1	14

(3) COMMAND REGISTER 2

The "Command register 2" is used for setting the "Initial character address", which corresponds to the T_0 pin. When the upper 2 bits (B7 and B6) of the 1st word is "0,1", the lower 4 bits (B3 to B0) are interpreted as command data and stored in the "Command register 2". The contents of the "Command register 2" are initialized to the default values by the power-ON reset or the reset signal, as shown below.

DEFAULT VALUES OF COMMAND REGISTER 2

- Initial character address : C1 (0,0,0,1)



DS3	DS2	DS1	DS0	Initial character address
0	0	0	0	C_0
0	0	0	1	C_1
0	0	1	0	C_2
0	0	1	1	C_3
0	1	0	0	C_4
0	1	0	1	C_5
0	1	1	0	C_6
0	1	1	1	C_7
1	0	0	0	C_8
1	0	0	1	C_9
1	0	1	0	C_{10}
1	0	1	1	C_{11}
1	1	0	0	C_{12}
1	1	0	1	C_{13}
1	1	1	0	C_{14}
1	1	1	1	Prohibited

(4) DISPLAY SHIFT OPERATION

The display shift operation is performed by changing the "Initial character address" of the "Command register 2". And the number of digits for the display shift in the loop is determined by the "Shifting display digits" of the "Command register 1". In other words, shifting display area ranges from the "Initial character address" specified by the "Command register 2" to the last address specified by the "Command register 1".

The default value of the "Initial character address" is C_1 (0,0,0,1), as shown in the table of "Display data RAM". In addition, supposing that the value of the "Shifting display digits" is "N", the "Initial character address" should be set in the range of C_0 and C_N in order not to exceed the digit "N". Because the display shift operation is not applied to the addresses beyond the digit "N", the display images, which were initially set up, appear on these addresses. Just for reference, one character of display image is composed of 16 segments.

HOW TO SET LEFT DISPLAY SHIFT

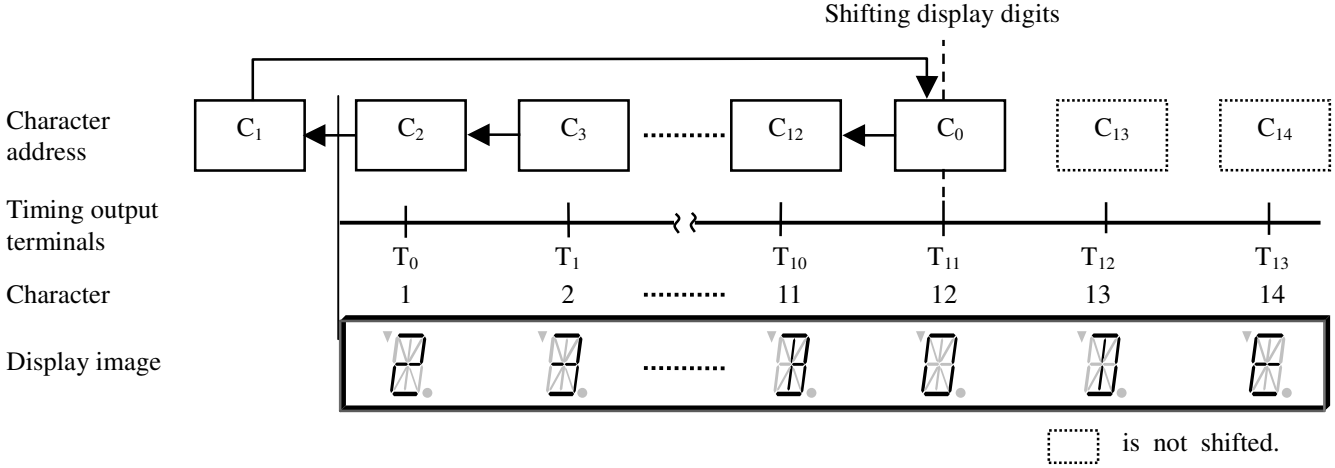
The left display shift is carried out by incrementing the "Initial character address" gradually like C_2, C_3, C_4, --- C_N. To the contrary, decrementing the address performs right display shift. The following description shows the example on how to set the left display shift, using alphanumeric display images such as "0", "1", "2", ---, "9", "A", "B", ---, and "E".

STEP1) Setting display images in the display data RAM

- Display RAM data

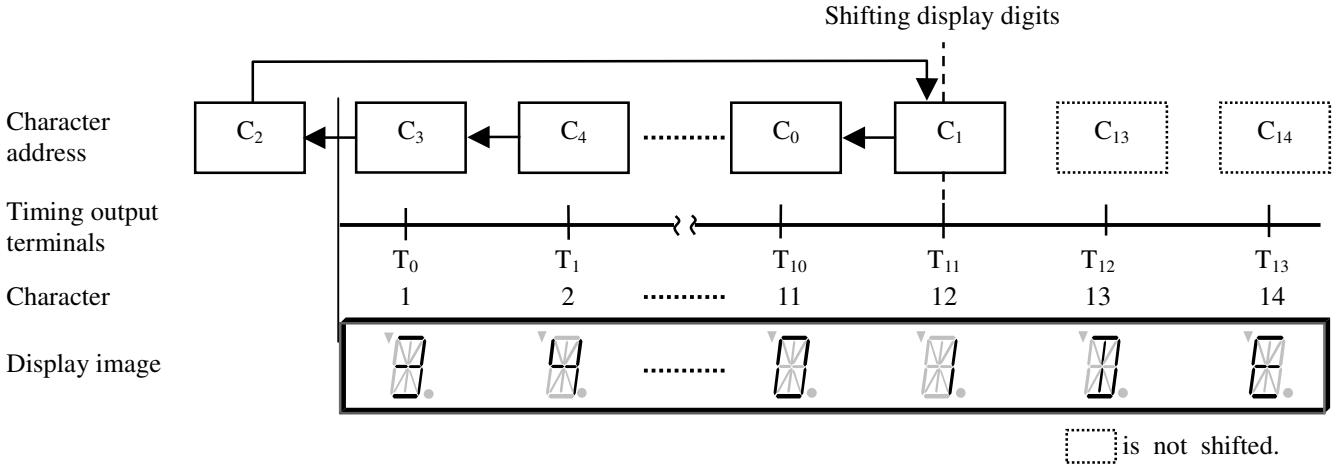
Character address	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
Display image	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E

SETP2) Setting the "Initial character address" to C_2 and the "Shifting display digits N" to 12 (T_{11}).

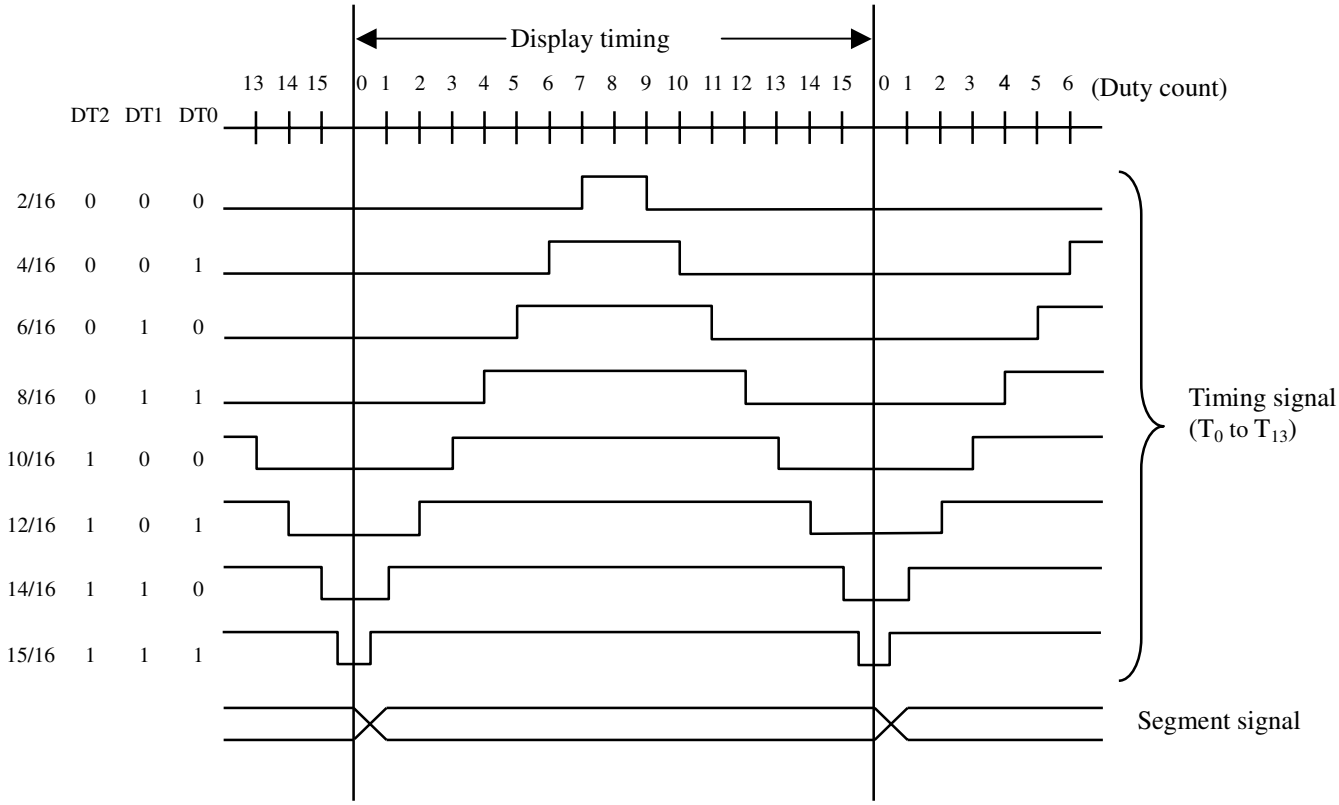


In this setting, the display images of "2", "3",- - - appear on the T_0, T_1, T_2, - - - T_{10} pins respectively, and the image "0" is on the T_{11} pin, which is assigned to the 12th character address. The display images "D" and "E" don't shift but remain on the T_{12} and T_{13} pins, assigned to the 13th and 14th characters respectively, because their character addresses are outside the digit "N".

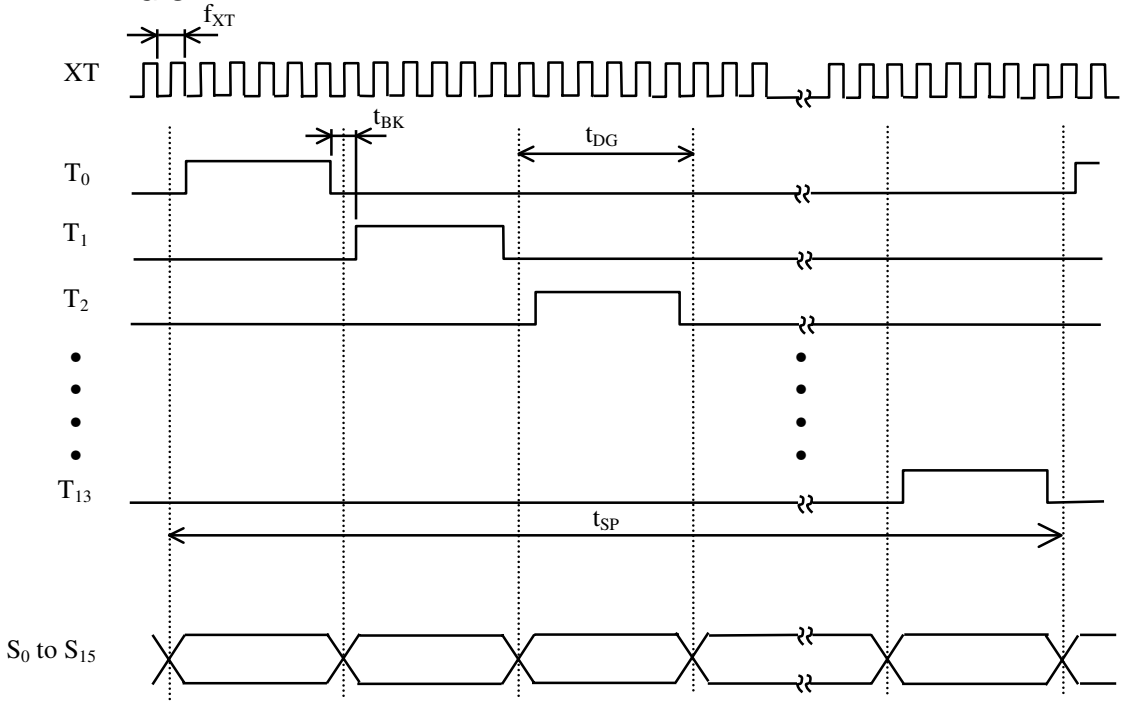
STEP3) Changing the "Initial character address" to C_3, and leaving the "Shifting display digits N" as 12 (T_{11}).



■ TIMING SIGNAL / DUTY-CHANGE WAVEFORM



■ DISPLAY TIMING CHART

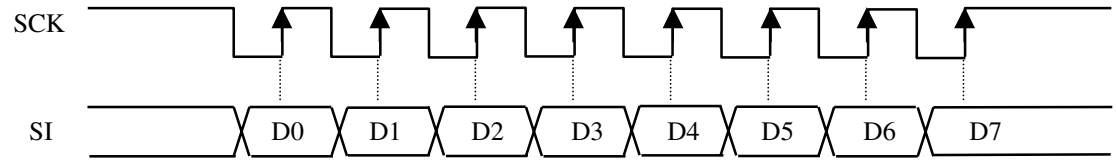


Oscillation frequency	: f_{XT}	:800kHz to 3.5MHz
Minimum blanking time (duty15/16)	: $t_{BK}=(1/f_{XT})$ x 16 x 2	:40µs to 9.14µs
1-character display time	: $t_{DG}=t_{BK}$ x 16	:640µs to 146.28µs
1-cycle display time	: $t_{SP}=t_{DG}$ x 14	:8.96ms to 2.05ms

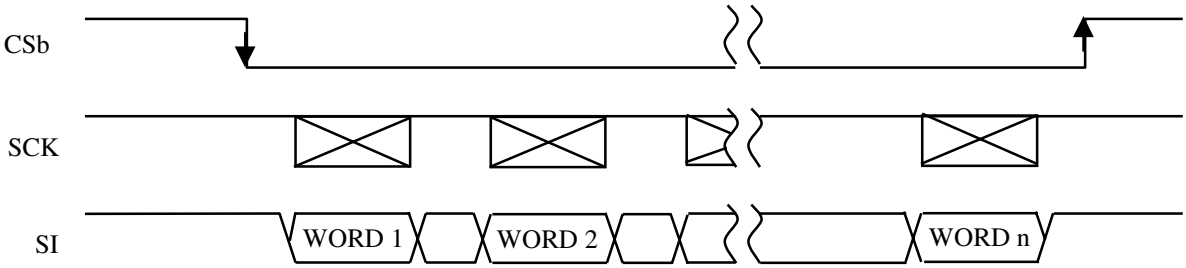
(5) SERIAL DATA TRANSMISSION

Communication between the **NJU3426** and MPU uses the serial data transmission with synchronous clock, and 8 bits serial data constitutes 1 word. Each bit on the SI pin is latched at the rising edge of the serial clock (SCK), and the entire 8 bits are loaded as 1 word at the rising edge of the chip select (CSb).

During a data transmission, multiple words are transferred continuously. The 1st word is either "Display data RAM address", "Command register 1" or "Command register 2". When the 1st word is RAM address data, the 2nd and ascending words are interpreted as display data. When it's the "Command register 1 or 2", the 2nd and ascending words are ignored.



SERIAL DATA TIMING



SERIAL DATA TRANSMISSION FORMAT

- Serial input data

DATA FORMAT FOR THE 1ST WORD

DISPLAY DATA RAM ADRESS

B7	B6	B5	B4	B3	B2	B1	B0
0	0	*	AD4	AD3	AD2	AD1	AD0

*:don't care

COMMAND DATA 1

B7	B6	B5	B4	B3	B2	B1	B0
1	DT2	DT1	DT0	DSP	DE2	DE1	DE0

*:don't care

COMMAND DATA 2

B7	B6	B5	B4	B3	B2	B1	B0
0	1	*	*	DS3	DS2	DS1	DS0

*:don't care

SERIAL DATA FOR THE 2ND AND ASCENDING WORDS

When the 1st word is the "Display data RAM address", the 2nd and ascending words are interpreted as display data. When the 1st word is the "Command register 1 or 2", the 2nd and ascending words are ignored.

■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply voltage	V_{DD}	-0.3 to +7.0	V	
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V	
VFD driving voltage	V_{FDP}	V_{DD}-45 to V_{DD}+0.3	V	Relative to V_{DD}.
"H" level output current 1	I_{OH1}	-15	mA	1 pin out of S_0 to S_{15} pins
"H" level output current 2	I_{OH2}	-35	mA	1 pin out of T_0 to T_{13} pins
"L" level output current	I_{OL}	20	mA	
Operating temperature	Topr	-40 to 85	°C	
Storage temperature	Tstg	-55 to 125	°C	
Power dissipation	PD	1500	mW	On two-layer board of based on the JEDEC.

Note 1): The LSI must be used inside the "Absolute maximum ratings". Otherwise, an electrical or physical stress may cause a permanent damage to the LSI.

Note 2): De-coupling capacitors should be placed on V_{DD} and V_{SS} and V_{FDP} and V_{SS} for stable operation.

Note 3): The following voltage relation must be maintained; $V_{DD} > V_{SS} \geq V_{FDP}$, V_{SS}=0.

■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

(V_{DD}=5.0V, V_{SS}=0V, Ta=-40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating voltage	V_{DD}	V_{DD} terminal	4.5		5.5	V
"H" level input voltage	V_{IH}	XT, RSTb, CSb, SCK, SI terminals	0.8V_{DD}			V
"L" level input voltage	V_{IL}				0.2V_{DD}	
Input off leak current	I_{IZ}	CSb, SCK, SI terminals V_{DD}=5.5V, V_I=0 or 5.5V			±1	μA
Display output current	I_{OH}	S_O to S_{15} terminals; V_{DD}=4.5V, V_{FDP}=V_{DD}-40V, V_{OH}=V_{DD}-2.5V	-4.5	-9		mA
		T_O to T_{13} terminals; V_{DD}=4.5V, V_{FDP}=V_{DD}-40V, V_{OH}=V_{DD}-2.5V	-10.5	-21		mA
Pull-up resistance	R_{UR}	RSTb terminal, Ta=25°C, V_I=V_{SS}	100		280	kΩ
Pull-down resistance	R_{DST}	S_0 to S_{15}, T_0 to T_{13} terminals, Ta=25°C V_I=V_{DD}, V_{FDP}=V_{DD}-40V	60		160	kΩ
Logic operating current	I_{SS}	V_{SS} terminal, All Segment/Timing output terminals open, RSTb terminal open, Ceramic resonator:1MHz, All Segment output OFF and All Timing output OFF		1	2	mA
Display operating current	I_{FDP}	V_{FDP} terminal, V_{FDP}=V_{DD}-40V, Ceramic resonator:1MHz, All Segment/Timing output ON		10	15	mA

• AC characteristics 1

(V_{DD}=5.0V, V_{SS}=0V, Ta=-40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating oscillation frequency	f_{XT}	Fig. 1	0.8		3.5	MHz
CR oscillation frequency *	f_{CR}	Ta=25°C R_f=27kΩ	0.85	1	1.15	MHz
External clock Input Rise time, Fall time	t_{CLH}, t_{CLL}	Fig. 2			250 *)	ns
Serial input data setup time	t_{SIS}	Fig. 2	35			ns
Serial input data hold time	t_{SIH}	Fig. 2	35			ns
Serial clock frequency	f_{SCK}	Fig. 3			1.5	MHz
Serial clock interval time	t_{SCI}	Fig. 3	10			μs
Reset palse width	t_{RSTb}	Fig. 4	10			μs
Power rise time	t_R	Fig. 5	0.05		10	ms

*) Noises on SCK during rise time or fall time may cause malfunctions. Testing samples in the application is recommended.

• DC characteristics 2

(V_{DD}=3.3V, V_{SS}=0V, Ta=-40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating voltage	V_{DD}	V_{DD} terminal		3.0		3.6	V
"H" level input voltage	V_{IH}	XT, RSTb, CSb, SCK, SI terminals		0.8V_{DD}			V
"L" level input voltage	V_{IL}					0.2V_{DD}	
Input off leak current	I_{IZ}	CSb, SCK, SI terminals V_{DD}=3.6V, V_I=0 or 3.6V				±1	μA
Display output current	I_{OH}	S_0 to S_{15} terminals	V_{DD}=3.0V, V_{FDP}=V_{DD}-40V, V_{OH}=V_{DD}-1.5V	-2	-4		mA
		T_0 to T_{13} terminals		-4.5	-9		mA
Pull-up resistance	R_{UR}	RSTb terminal, Ta=25°C, V_I=V_{SS}		100		280	kΩ
Pull-down resistance	R_{DST}	S_0 to S_{15}, T_0 to T_{13} terminals, Ta=25°C V_I=V_{DD}, V_{FDP}=V_{DD}-40V		60		160	kΩ
Logic operating current	I_{SS}	V_{SS} terminal, All Segment/Timing output terminals open, RSTb terminal open, Ceramic resonator:1MHz, All Segment output OFF and All Timing output OFF			0.8	1.5	mA
Display operating current	I_{FDP}	V_{FDP} terminal, V_{FDP}=V_{DD}-40V, Ceramic resonator:1MHz, All Segment/Timing output ON			10	15	mA

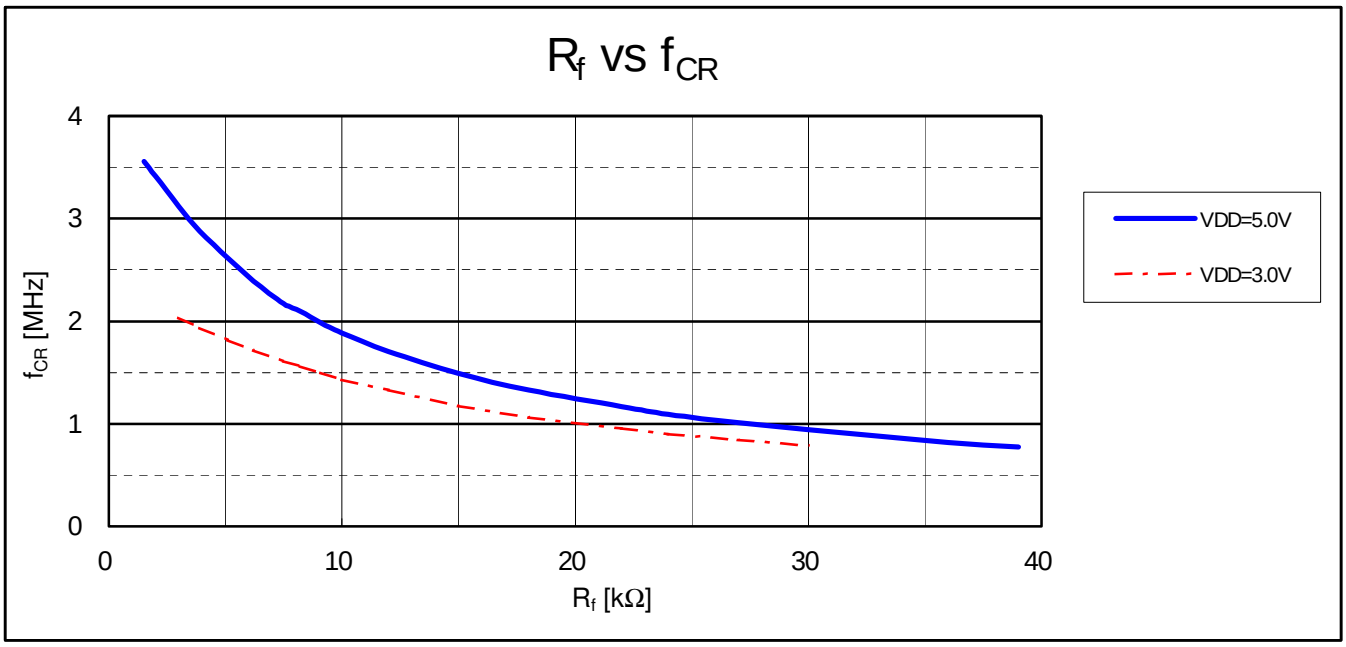
• AC characteristics 2

(V_{DD}=3.3V, V_{SS}=0V, Ta=-40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating oscillation frequency	f_{XT}	Fig. 1	0.8		2	MH_Z
CR oscillation frequency *	f_{CR}	Ta=25°C R_f=18kΩ	0.85	1	1.15	MHz
External clock Input Rise time, Fall time	t_{CLH}, t_{CLL}	Fig. 2			250 *)	ns
Serial input data setup time	t_{SIS}	Fig. 2	70			ns
Serial input data hold time	t_{SIH}	Fig. 2	70			ns
Serial clock frequency	f_{SCK}	Fig. 3			0.8	MH_Z
Serial clock interval time	t_{SCI}	Fig. 3	10			μs
Reset palse width	t_{RSTb}	Fig. 4	20			μs
Power rise time	t_R	Fig. 5	0.05		5	ms

*) Noises on SCK during rise time or fall time may cause malfunctions. Testing samples in the application is recommended.

* Relation between external resistor (R_f) and oscillation frequency (f_{CR}).
The frequency can be adjusted by the selection of external resistor R_f, as shown in "R_f vs f_{CR}".
Refer to circuit example of "■ **APPLICATION CIRCUIT** (b) CR oscillation".



This graph shows a reference characteristic, and this performance is not guaranteed.

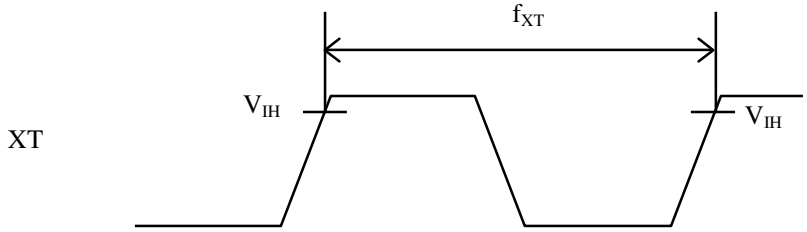


Fig. 1

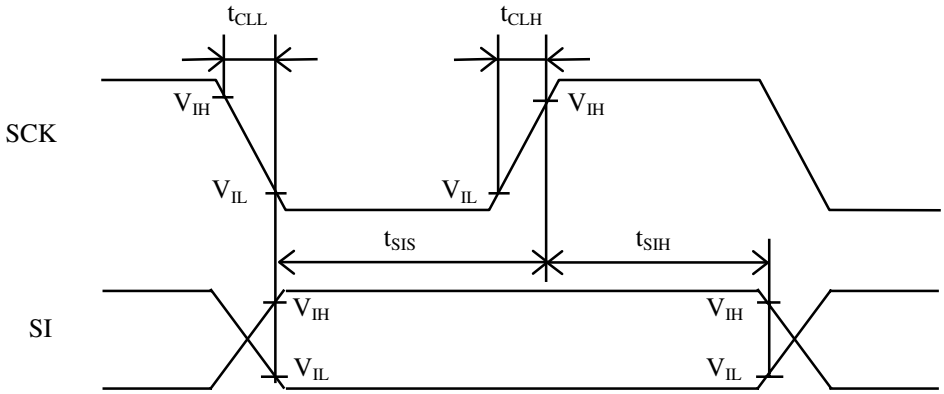


Fig. 2

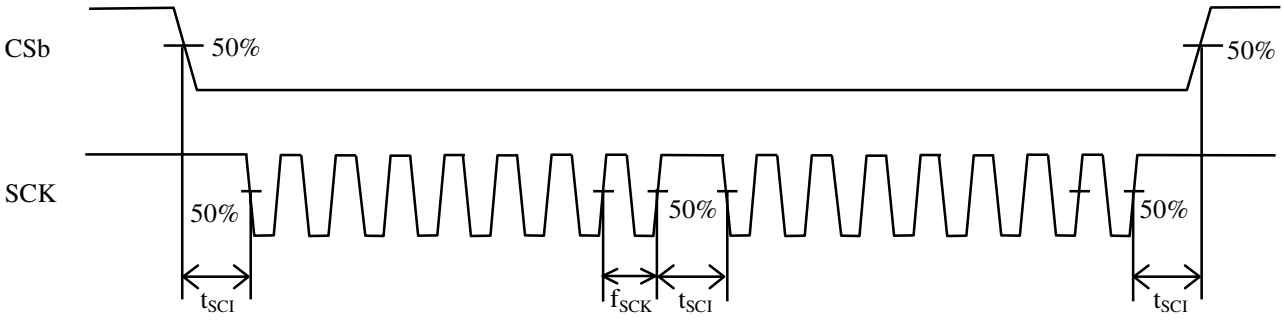


Fig. 3

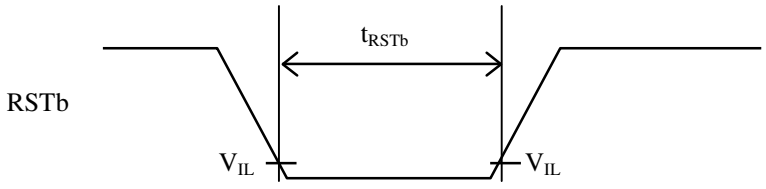


Fig. 4

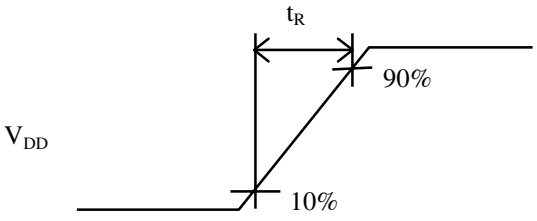
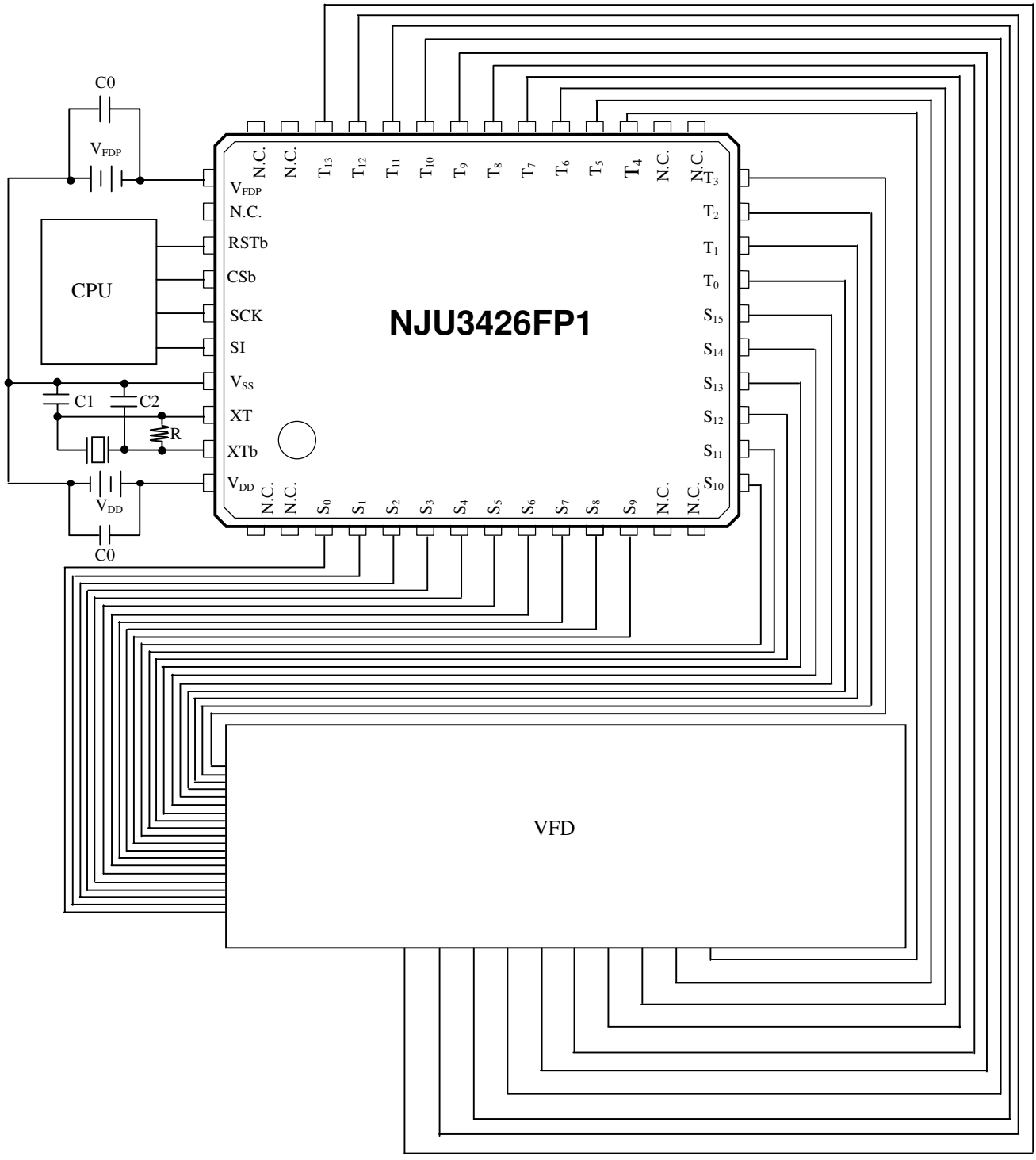


Fig. 5

■ APPLICATION CIRCUIT

(a) Ceramic Resonator Oscillation



(b) Ceramic Resonator Oscillation