

47 μ F AC-Coupling Capacitor Low Voltage Video Driver with LPF

■GENERAL DESCRIPTION

The **NJM2512A** is a Low Voltage Video Amplifier featuring small AC-coupling Capacitor.

The NJRC original Technology "ASC(Advanced SAG Correction)" realizes 47 μ F AC-Coupling Capacitor which enables to downsize mounting space.

No worrying about beat noise caused by charge-pump circuit, and over-current caused by circuit short out than Capacitor-less video driver.

The **NJM2512A** is suitable for any video application.

NJM2512: Gain=6dB

NJM2512A : Gain=12dB

■PACKAGE OUTLINE

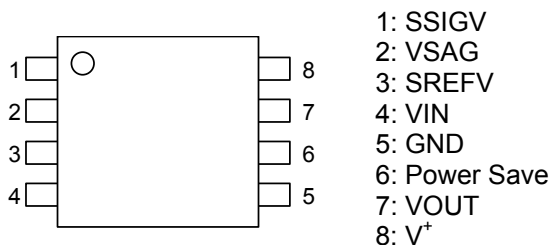


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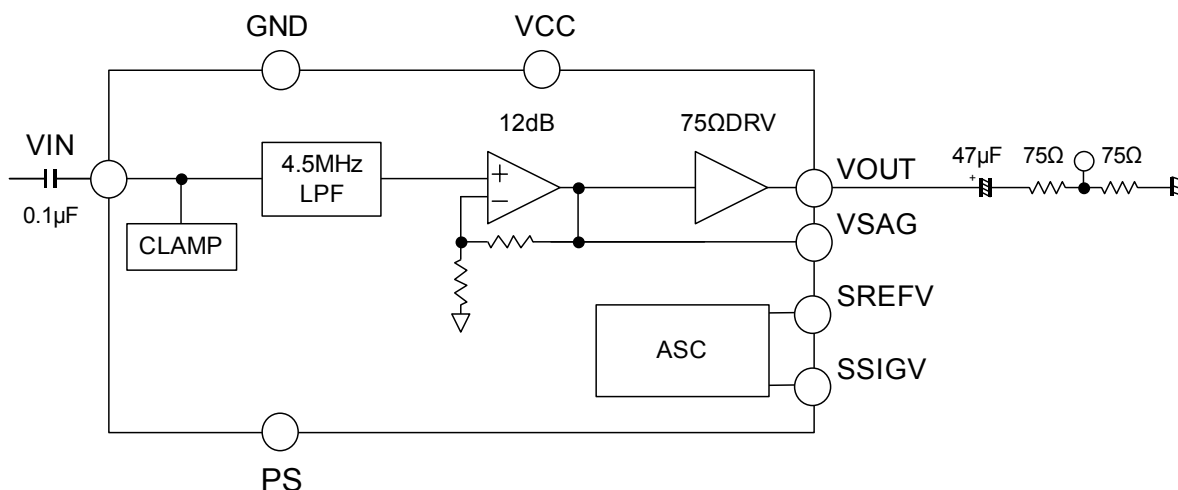
■FEATURES

- Operating Voltage 3.0 to 5.5V
- AC-Coupling capacitor 47 μ F
- 6dB Amplifier
- 75 Ω Driver
- Internal LPF 0dBtyp.at 4.5MHz
 -33dBtyp.at 19MHz
- Power-save Circuit
- Bipolar Technology
- Package Outline TVSP8

■PIN CONNECTION



■BLOCK DIAGRAM



NJM2512A

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	7.0	V
Power Dissipation	P _D	580(Note1)	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +150	°C

(Note1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm Two layers, FR-4)

■RECCOMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating voltage	Vopr		3.0	-	5.5	V

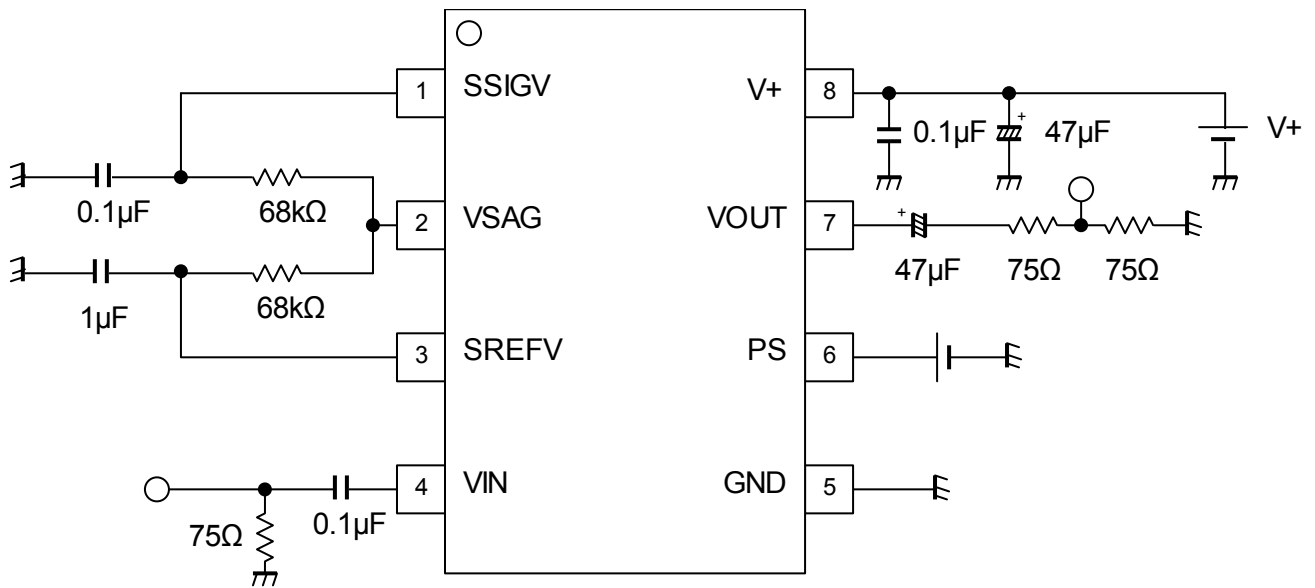
■ELECTRICAL CHARACTERISTICS (V⁺=3.3V, RL=150Ω, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I _{CC}	No signal	-	10	15	mA
Supply Current at Power Save Mode	I _{save}	Power save mode	-	20	50	μA
Maximum Output Level	V _{om}	Vin=100kHz, sin-signal, THD=1%,	2.2	-	-	Vp-p
Voltage Gain	G _v	Vin=1MHz, 1.0Vp-p sin-signal	11.5	12.0	12.5	dB
Low Pass Filter Characteristic	Gf4.5M	Vin=4.5MHz/1MHz, 1.0Vpp sin-signal	-0.6	-0.1	+0.4	dB
	Gf19 M	Vin=19MHz/1MHz, 1.0Vpp sin-signal	-	-33	-23	dB
Differential Gain	DG	Vin=1.0Vp-p 10step video signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step video signal	-	0.5	-	deg
S/N Ratio	SN	100kHz to 6MHz, Vin=1.0Vp-p 100% White Video Signal, RL=75Ω	-	60	-	dB
SW Voltage High Level	V _{thH}	Active	1.8	-	V ⁺	V
SW Voltage Low Level	V _{thL}	Non-Active	0	-	0.3	V
SW Sink Current High Level	I _{thH}	V=5V	-	-	300	μA
SW Sink Current Low Level	I _{thL}	V=0.3V	-	-	5	μA

■ CONTROL TERMINAL

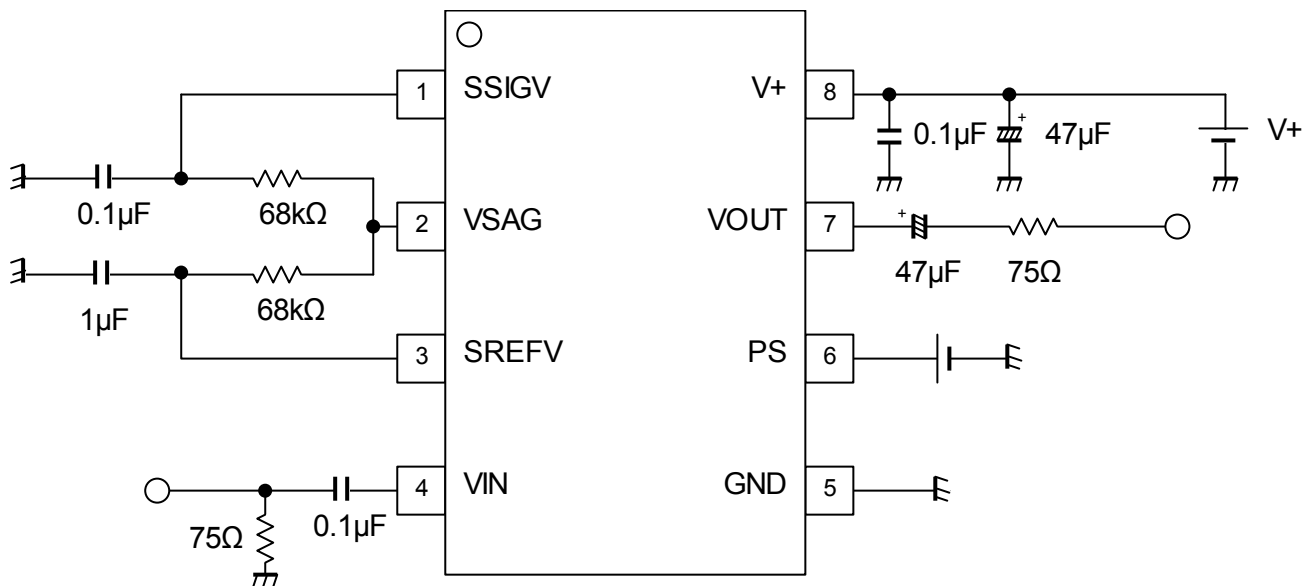
PARAMETER	STATUS	MODE
Power Save	H	Power save: OFF Active mode
	L	Power save: ON Non-Active mode (Mute)
	OPEN	Power save: OFF Non-Active mode (Mute)

■ TEST CIRCUIT

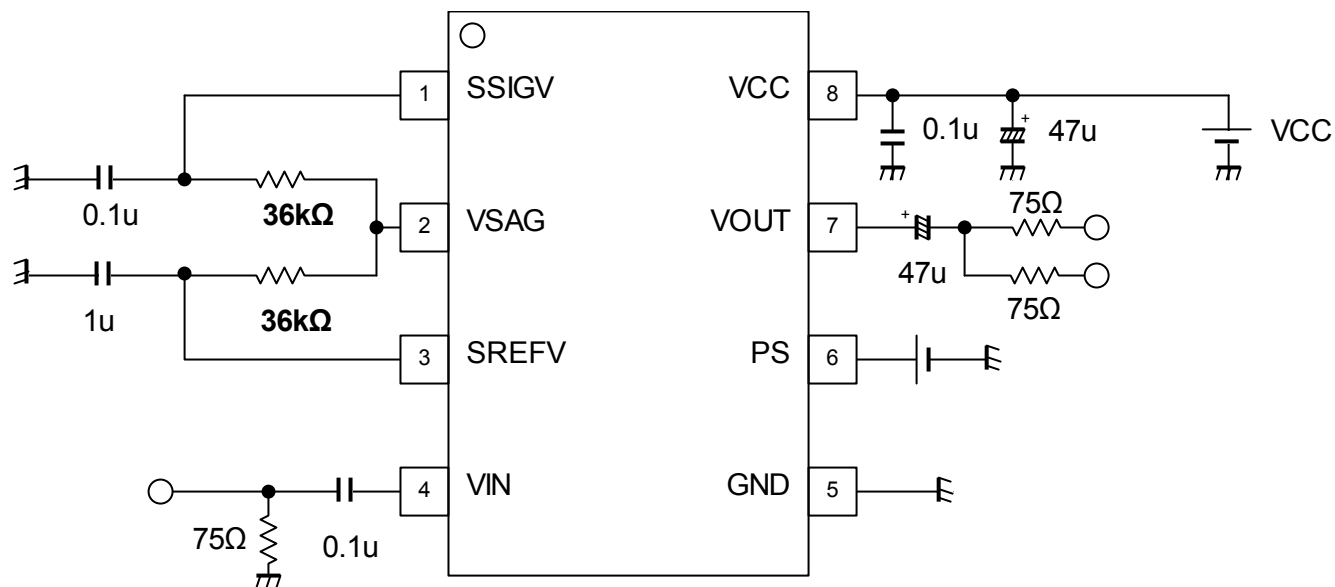


NJM2512A

APPLICATION CIRCUIT1



APPLICATION CIRCUIT2(2-line drive)



APPLICATION NOTE

NJM2512A has possibilities that decrease in the capacitance in low-frequency band when the ceramic capacitor is used (pin 7). It is a possibility that the sag is generated when the ceramic capacitor decreases capacity. Please verify it in consideration of the capacity drop of the ceramic capacitor.

◆Clamp circuit

1. Operation of Sync-tip-clamp

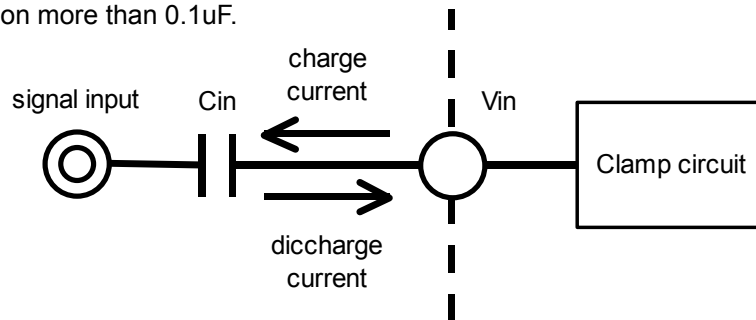
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input C_{in} . It is charged to the capacitor to the external input C_{in} at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor C_{in} at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of C_{in} and discharging of C_{in} at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor C_{in} .

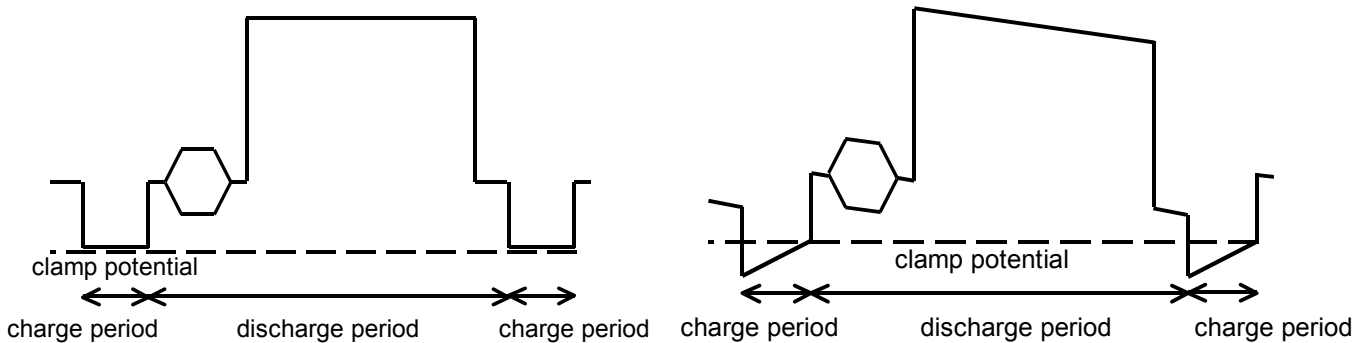
If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1 μ F.



< Clamp circuit >

A. C_{in} is large

B. C_{in} is small (H sag experience)



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few $k\Omega$. On the other hand, the input impedance of the discharge period is several $M\Omega$. Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

Source impedance to the input terminal, please lower than 200 Ω . A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

[CAUTION]

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