LOW VOLTAGE VIDEO AMPLIFIER WITH LPF

■GENERAL DESCRIPTION

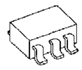
The **NJM2561B** is a Low Voltage Video Amplifier contained LPF circuit. Internal 75Ω driver is easy to connect TV monitor directly.

It corresponds to both AC-coupling and DC-coupling.*

The **NJM2561B** features low power and small package, and is suitable for low power design on downsizing of DSC and DVC.

*0.33V is always output from Vout.

■PACKAGE OUTLINE

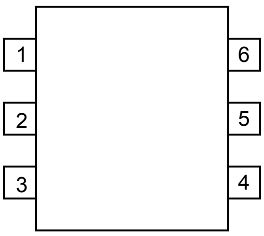


NJM2561BF1

■FEATURES

- Operating Voltage 2.8 to 5.5V
- 6th Order LPF -33dB at 19MHz typ.
- 6dB Amplifier
- 75Ω Driver Circuit
- Power Save Circuit
- Bipolar Technology
- Package Outline SOT-23-6 (MTP6)

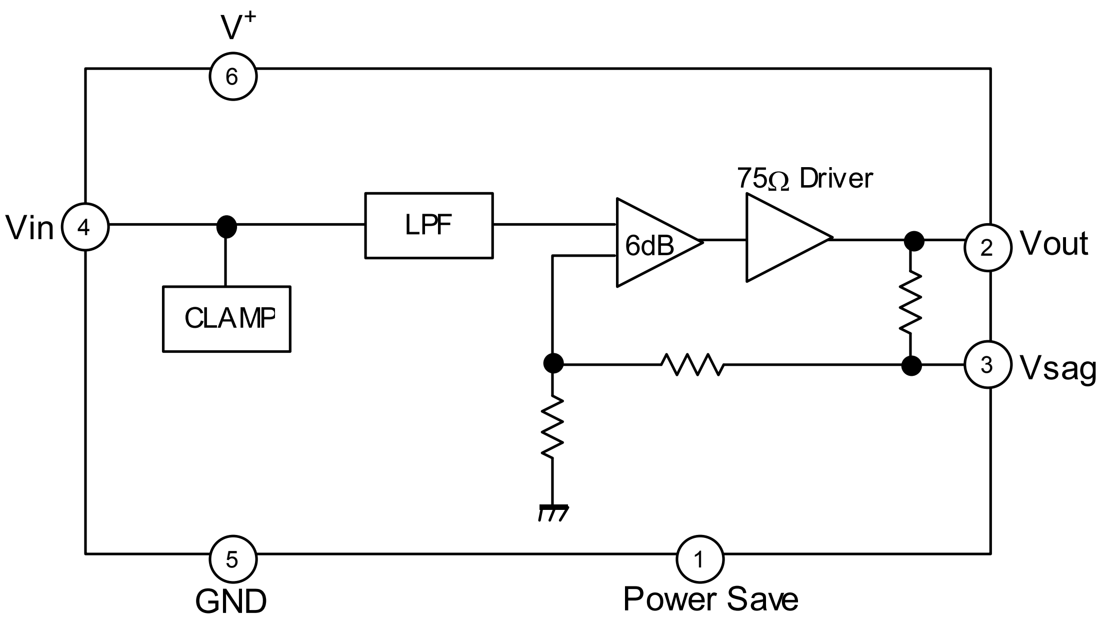
■PIN CONFIGURATION



MTP6

1. Power Save
2. Vout
3. Vsag
4. Vin
5. GND
6. V^+

■BLOCK DIAGRAM



Ver.3.1

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7.0	V
Power Dissipation	P_D	410(MTP6) Note	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(Note) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm 2 layers, FR-4)

■ RECOMMENDED OPEARATING CONDITION (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr		2.8	3.0	5.5	V

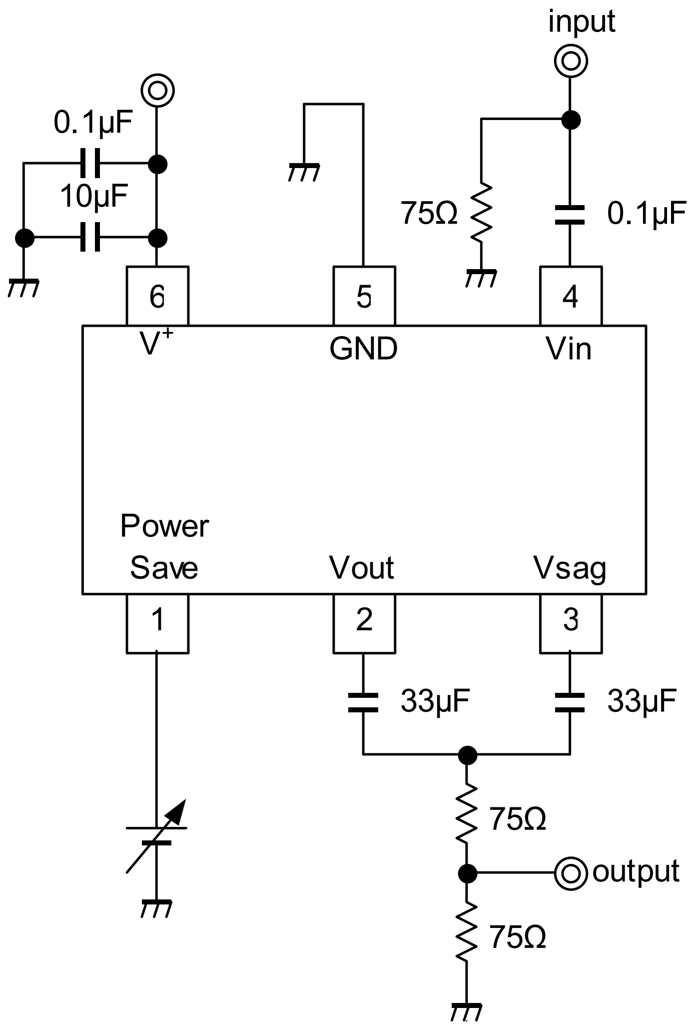
■ELECTRICAL CHARACTERISTICS (V^+=3.0V,R_L=150Ω,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	-	8.0	12.0	mA
Operating Current at Power Save	Isave	No Signal, Power Save Mode	-	30	50	μA
Maximum Output Voltage Swing	Vom	f=100kHz,THD=1%	2.2	2.5	-	Vp-p
Voltage Gain	Gv	Vin=100kHz, 1.0Vp-p, Input Sine Signal	5.6	6.0	6.4	dB
Low Pass Filter Characteristic	Gfy4.5M	Vin=4.5MHz/100kHz, 1.0Vp-p	-0.6	-0.1	0.4	dB
	Gfy19M	Vin=19MHz/100kHz, 1.0Vp-p	-	-33	-23	
Differential Gain	DG	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	deg
S/N Ratio	SNv	Vin=1.0Vp-p, R_L=75Ω 100% White Video Signal, 100KHz to 6MHz	-	+65	-	dB
2nd. Distortion	Hv	Vin=1.0Vp-p, 3.58MHz, Sine Signal, R_L=75Ω	-	-50	-	dB
SW Change Voltage High Level	VthPH	Active	1.8	-	V^+	V
SW Change Voltage Low Level	VthPL	Non-active	0	-	0.3	

■CONTROL TERMINAL

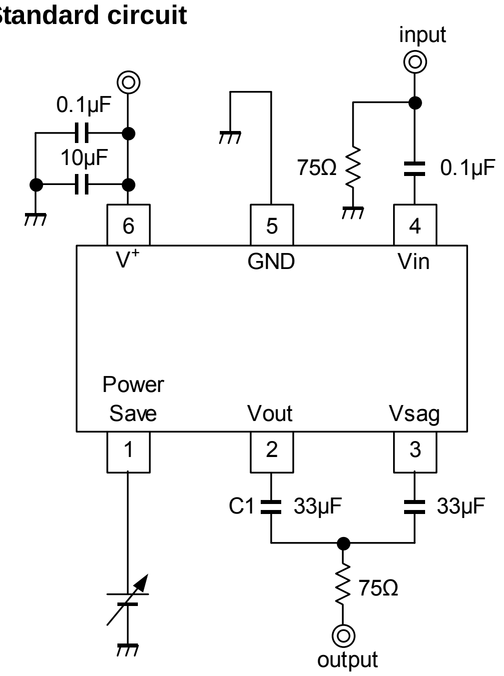
PARAMETER	STATUS	NOTE
Power Save	H	Power Save: OFF(Active)
	L	Power Save: ON (Mute)
	OPEN	Power Save: ON (Mute)

■TEST CIRCUIT

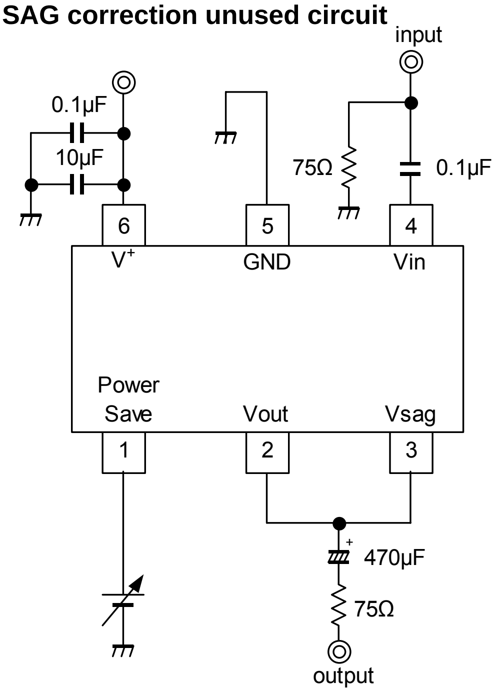


■ APPLICATION CIRCUIT (MTP6, in case AC-coupling)

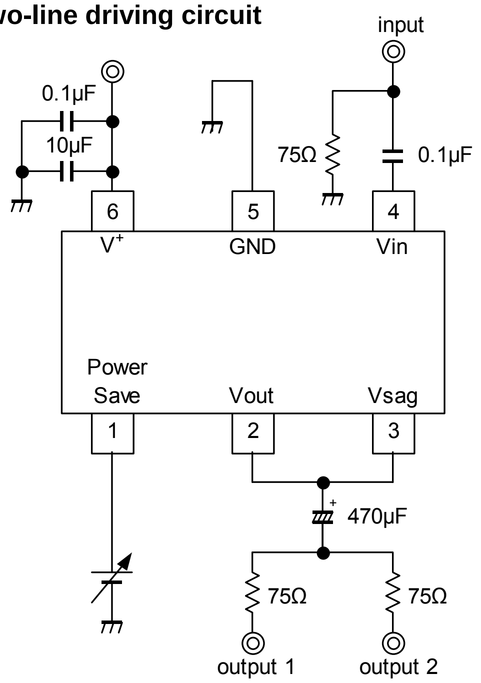
(1) Standard circuit



(2) SAG correction unused circuit



(3) Two-line driving circuit



(1) Standard circuit

This circuit is for a portable equipment of small mounting space.
The SAG correction reduces output coupling capacitor values.
However, this circuit may cause to SAG deterioration, and lose synchronization by luminance fluctuation.
Adjust the C1 value, checking the waveform containing a lot of low frequency components like a bounce waveform (Worst condition waveform of SAG). Change the capacitor of C1 into a large value to improve SAG.

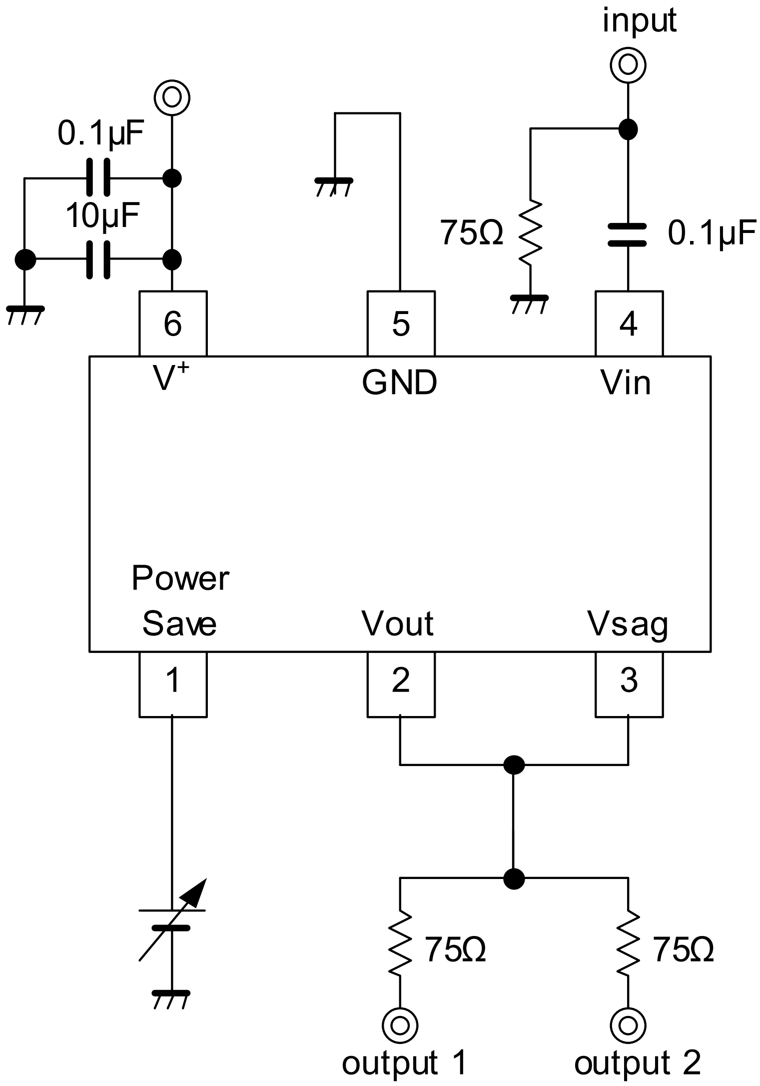
(2) SAG correction unused circuit

We recommend this circuit when there is no space limitation.
Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470µF or more.

(3) Two-line driving circuit

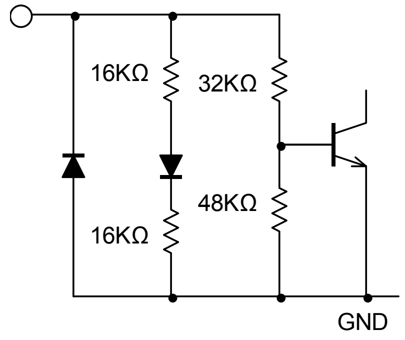
This circuit drives two-line of 150Ω. However, it may cause to lose synchronization by an input signal of large APL change (100% white signals more than 1Vp-p). Confirm the large APL change waveform (100% white signals more than 1Vp-p) and evaluate sufficiently.

■ **APPLICATION CIRCUIT (MTP6, in case DC-coupling)**



Note)
0.33V is always output from Vout.

■ TERMINAL DESCRIPTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>VOLTAGE</th><th>EQUIVALENT CIRCUIT</th></tr>
<tr><td>1</td><td>Power Save</td><td>-</td><td>
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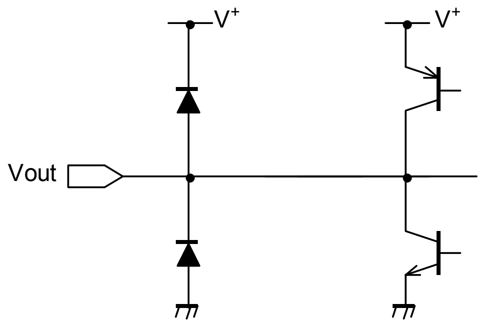
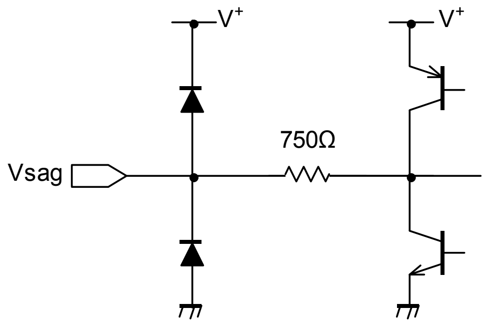
<tr><td>2</td><td>Vout</td><td>0.33V</td><td>
</td></tr>
<tr><td>3</td><td>Vsag</td><td>-</td><td>
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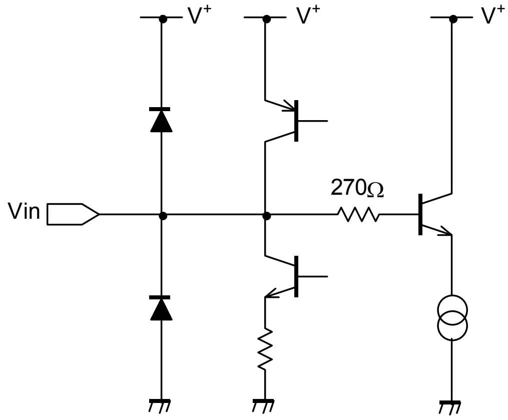
<tr><td>4</td><td>Vin</td><td>1.10V</td><td>
</td></tr>
<tr><td>5</td><td>GND</td><td>-</td><td></td></tr>
<tr><td>6</td><td>V^+</td><td>3V</td><td></td></tr>
</table>

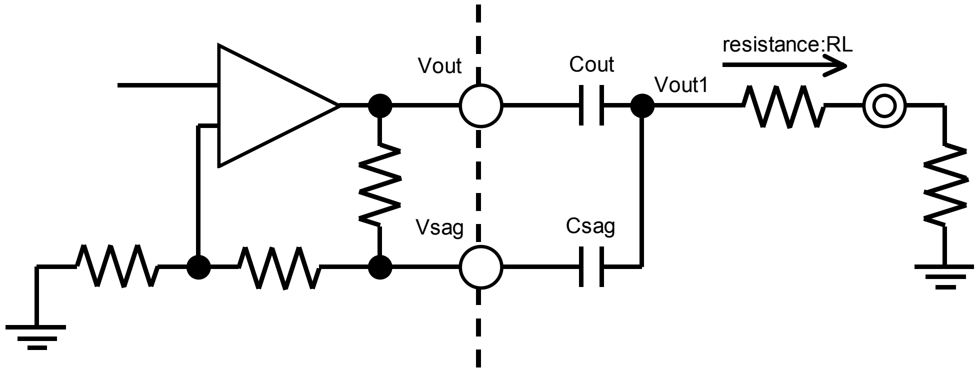
■ APPLICATION

♦ SAG correction circuit

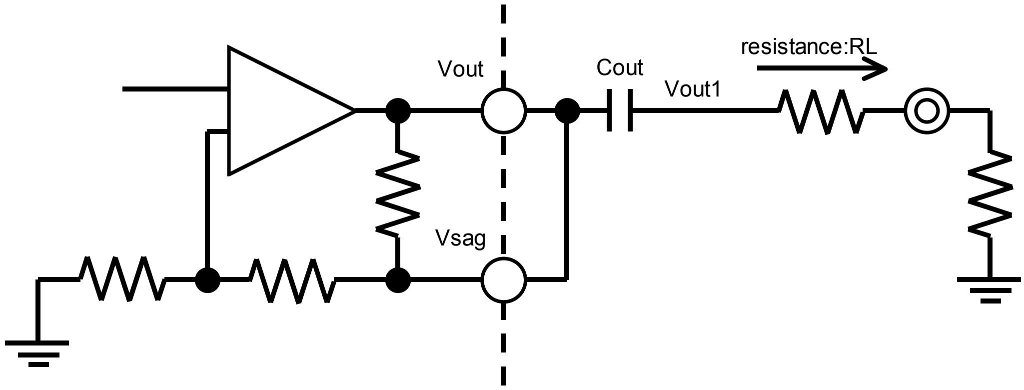
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for Vsag (Csag) is connected to the negative feedback of the amplifier. This Csag increase the low frequency gain to correct for the attenuation of low frequency gain.

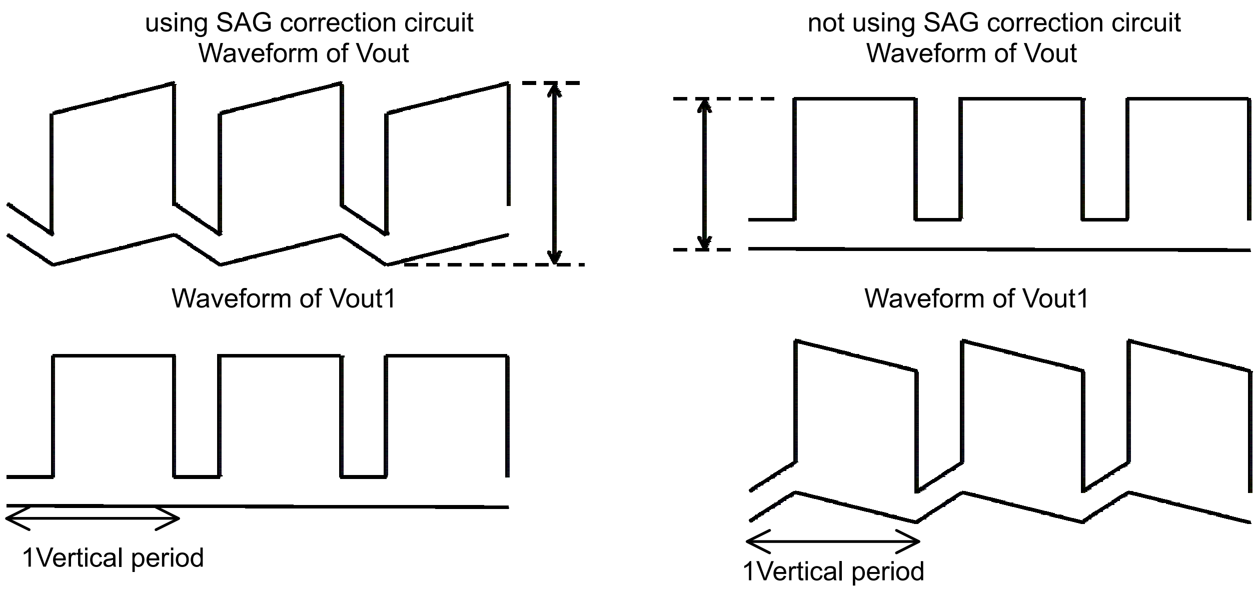
Example SAG collection circuit



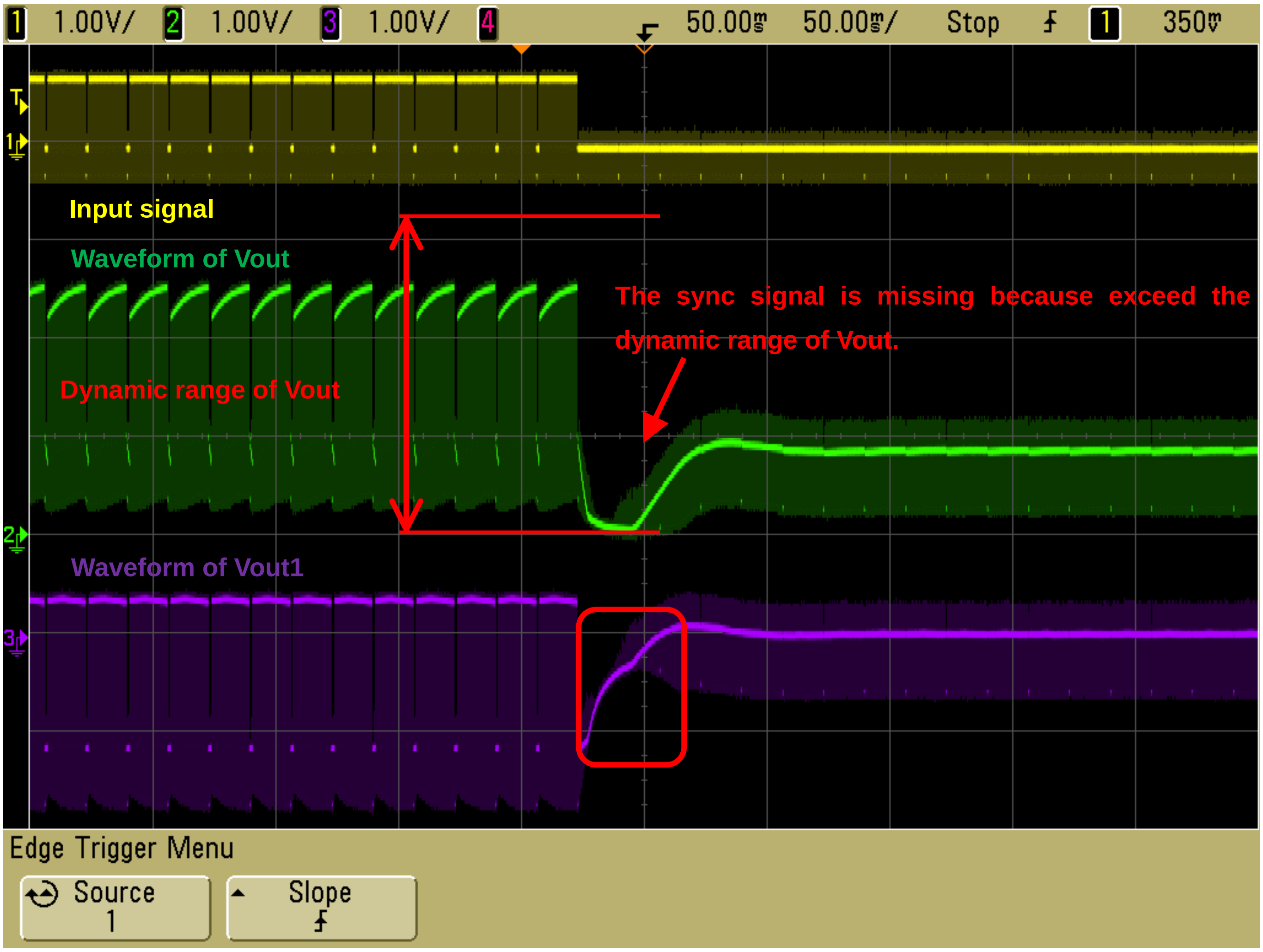
Example of not using sag compensation circuit



Waveform of Vout terminal and Vout1 terminal



SAG correction circuit generates a low frequency component signal amplified to Vout terminal.
Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin.
At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.
Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.



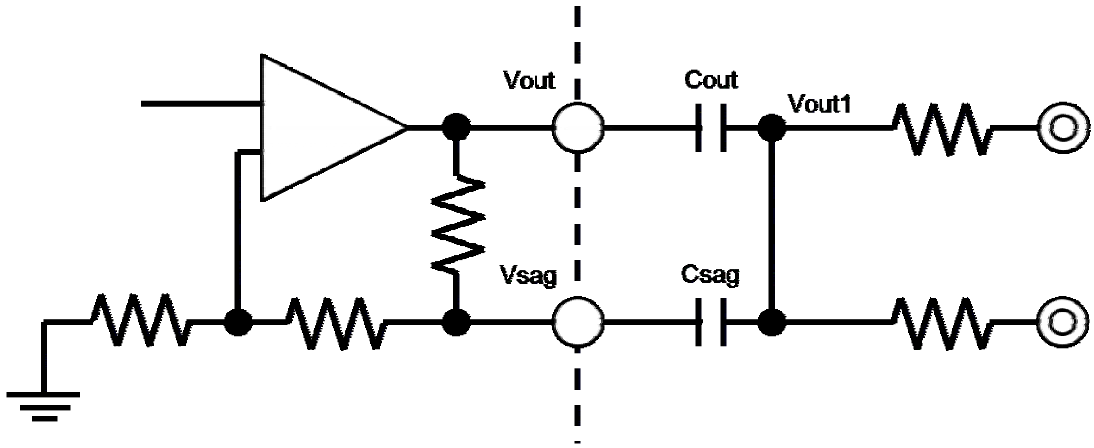
< Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).
It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.
Signal can output within dynamic range for reason it does not change the DC level of the output terminal.
However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate.
Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.

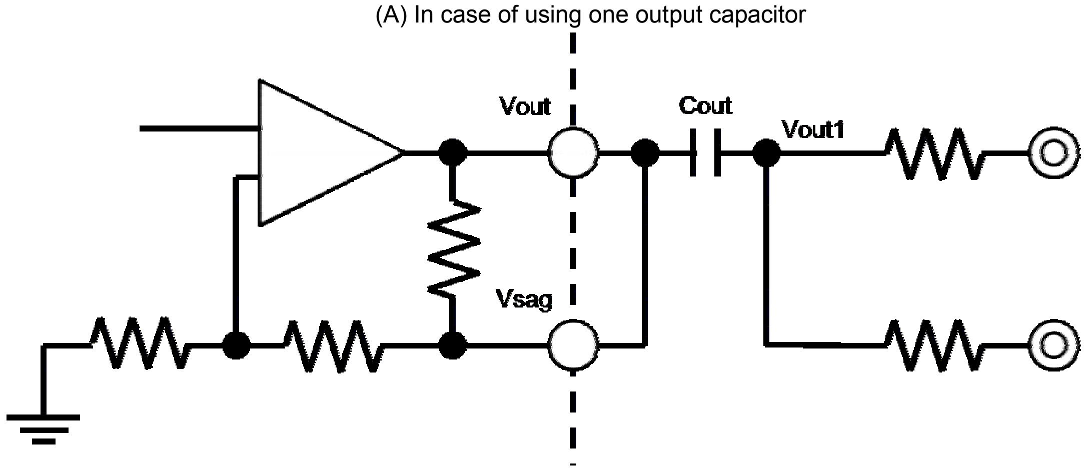


< Dual drive at not using SAG correction circuit >

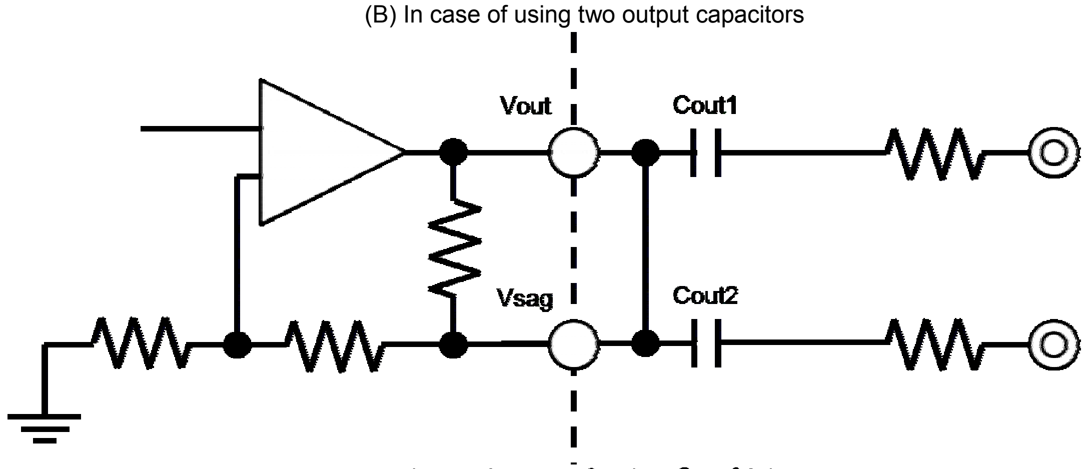
We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

$$Cout = Cout1 + Cout2$$
$$Cout1 = Cout2$$

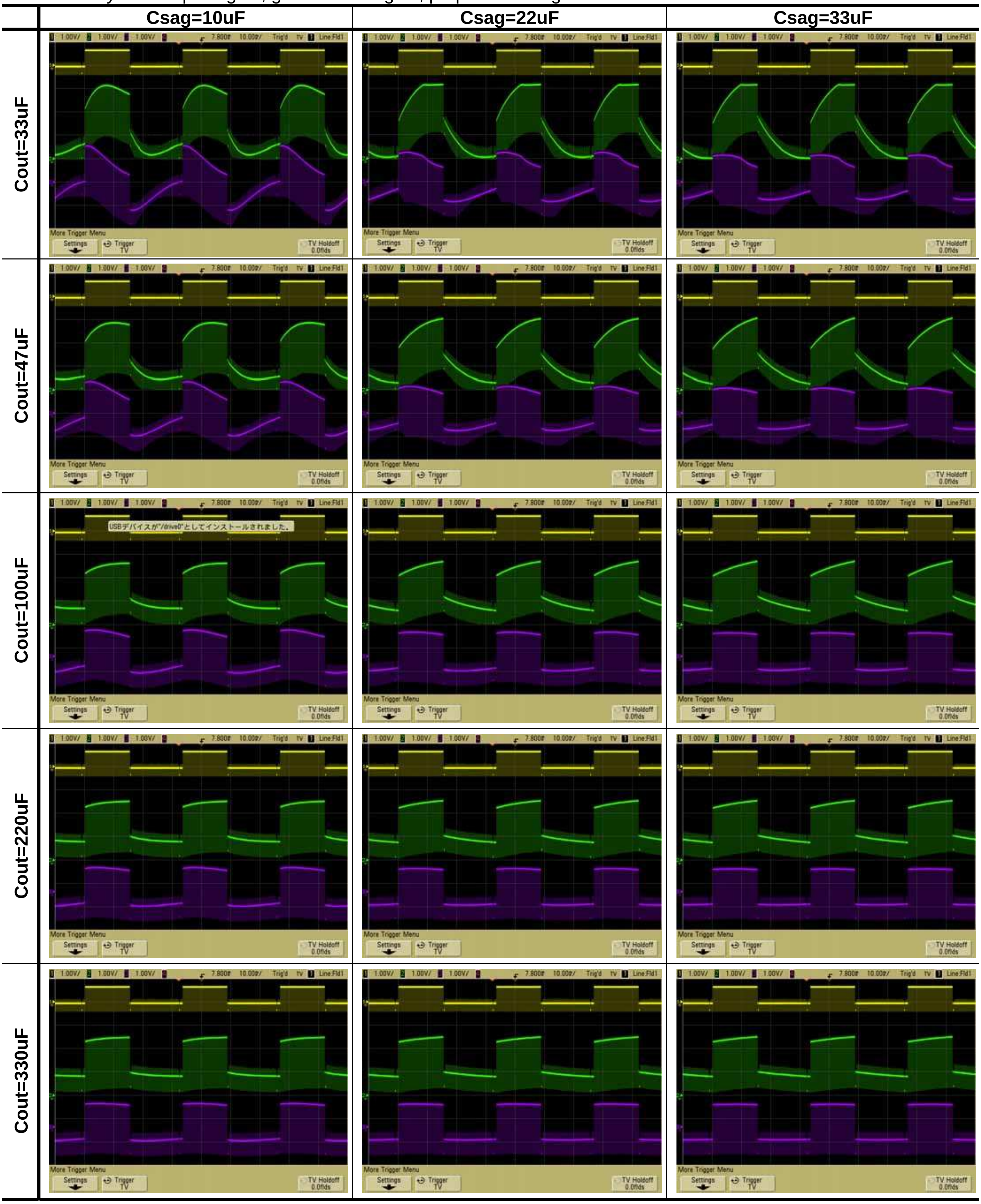
(A) In case of using one output capacitor



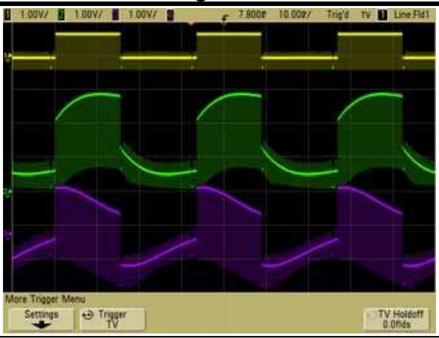
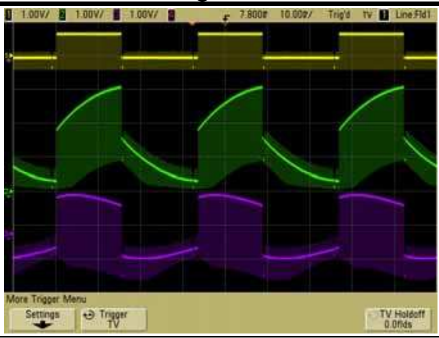
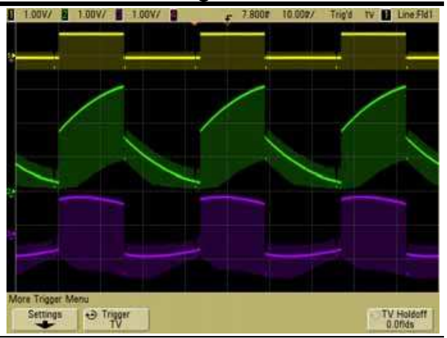
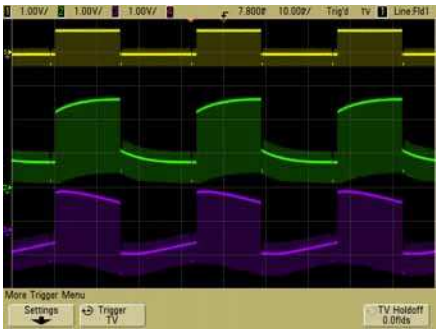
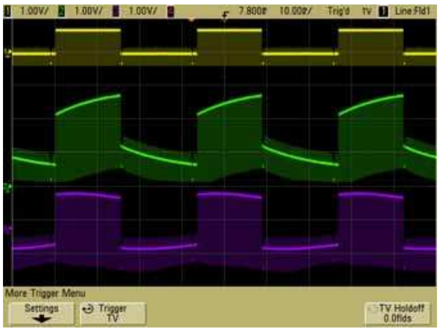
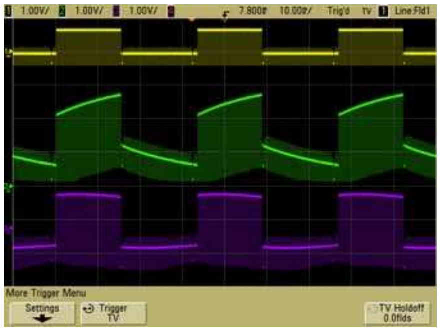
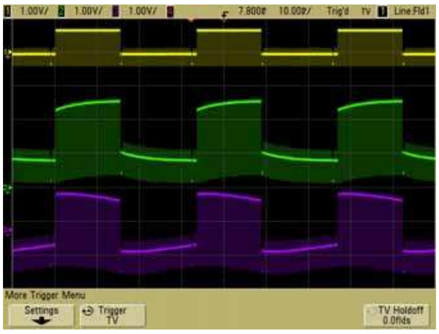
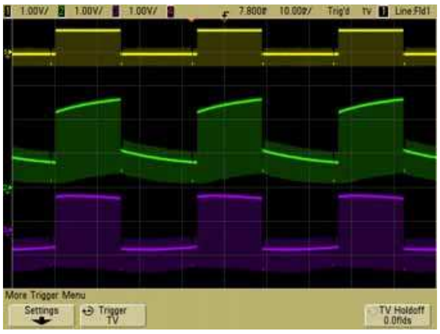
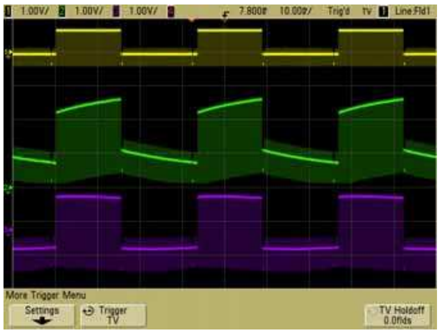
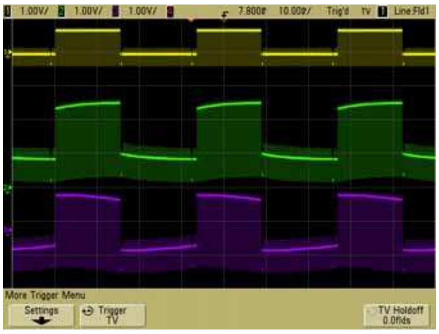
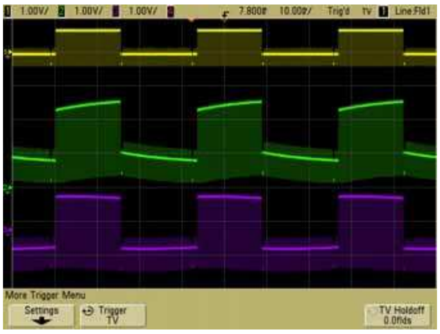
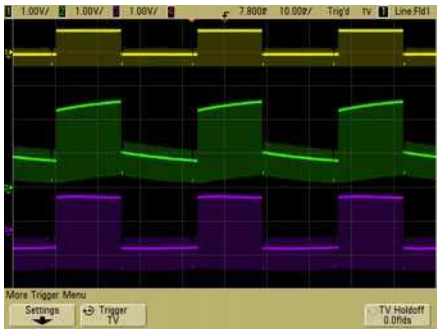
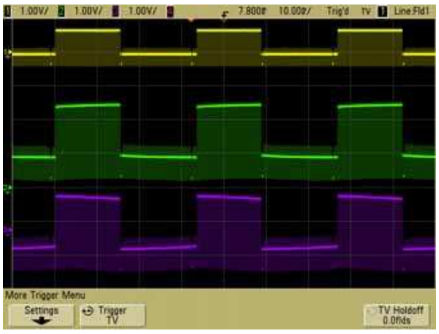
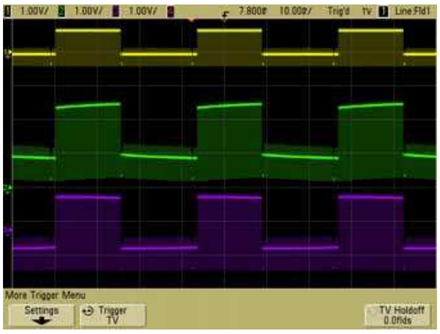
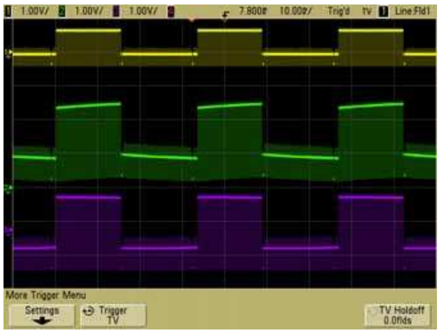
(B) In case of using two output capacitors



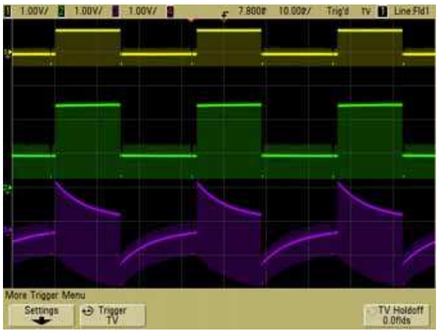
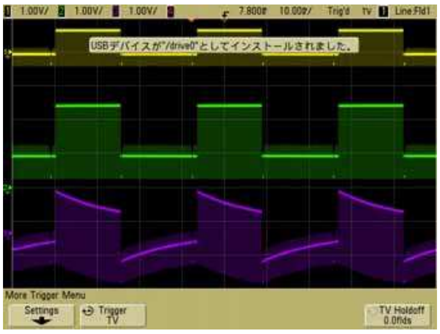
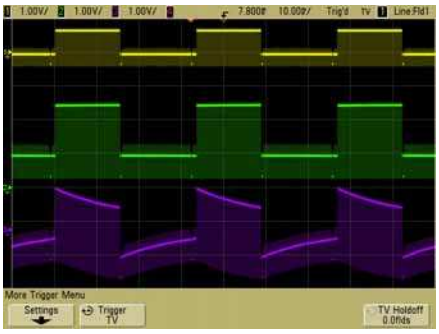
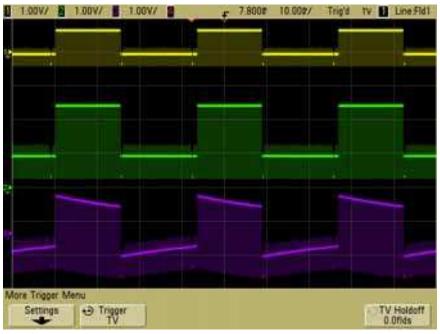
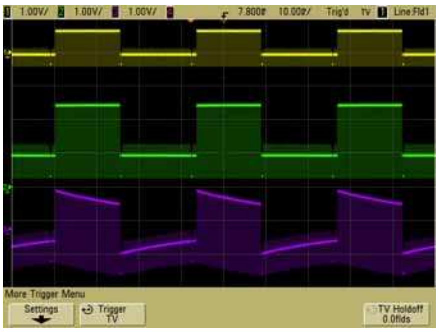
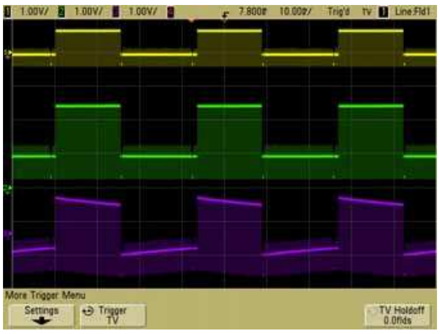
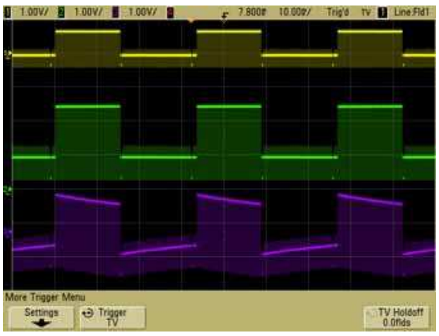
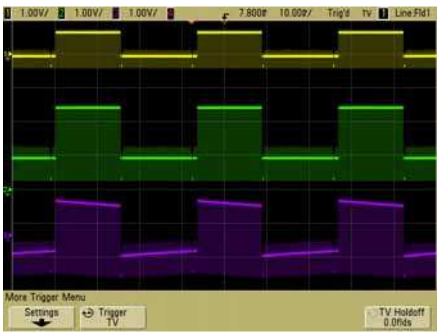
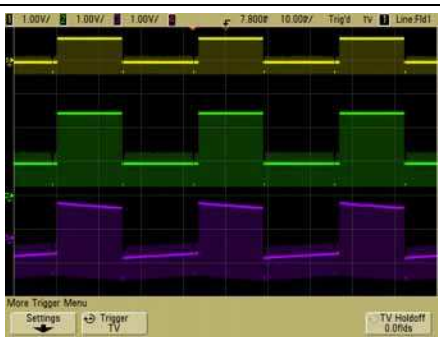
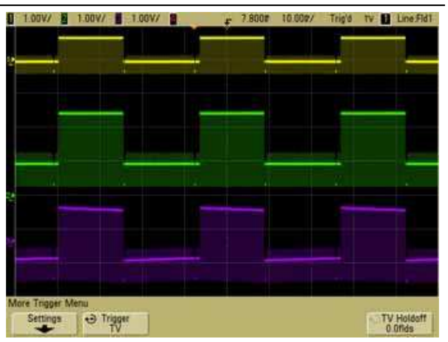
< Using SAG correction circuit >
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=100uF			
Cout=220uF			
Cout=330uF			
Cout=470uF			
Cout=1000uF			

< Not using SAG correction circuit >
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	RL=75Ω	RL=150Ω
Cout=100uF		
Cout=220uF		
Cout=330uF		
Cout=470uF		
Cout=1000uF		

< Using SAG correction circuit >
Input signal: Black to White100%, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

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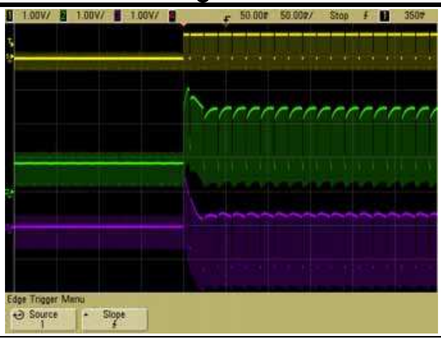
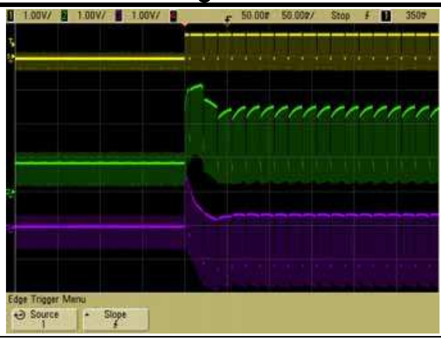
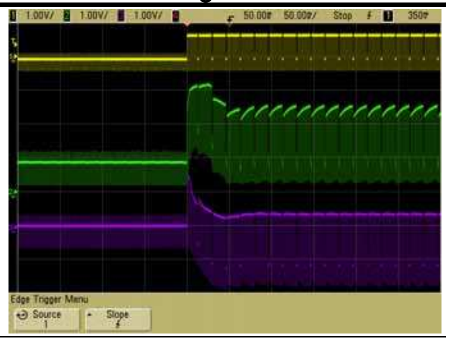
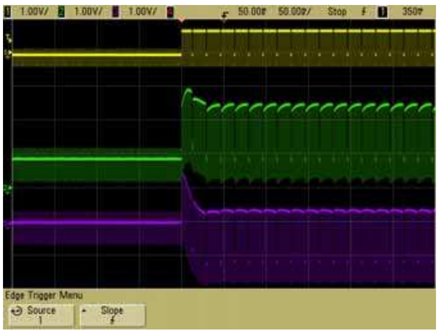
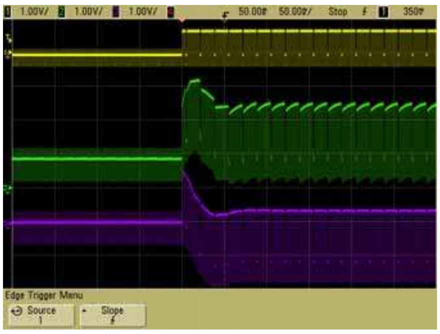
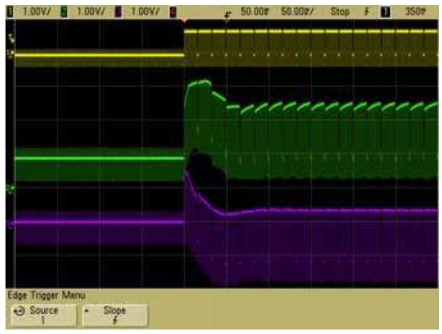
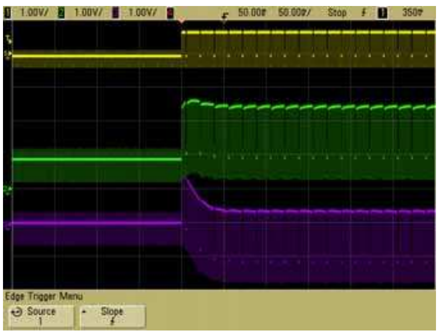
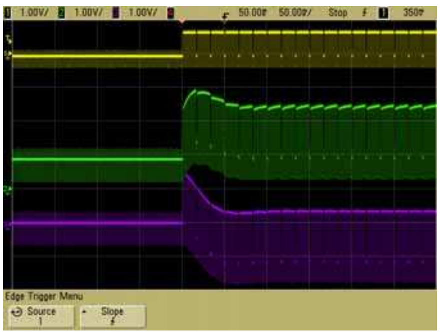
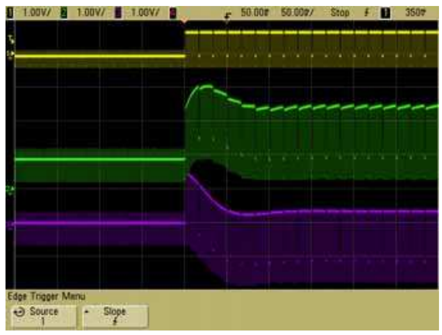
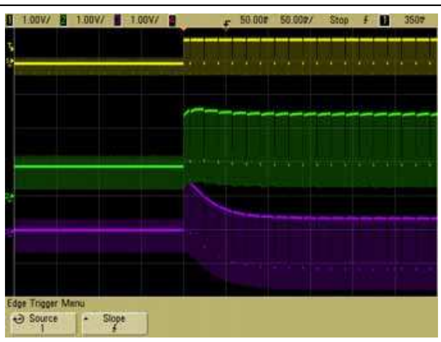
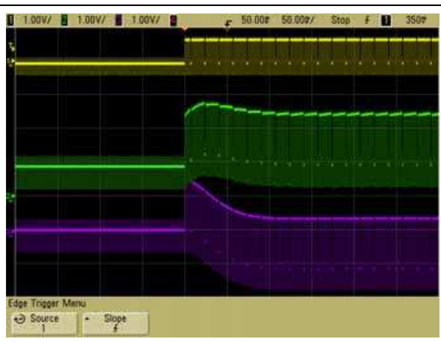
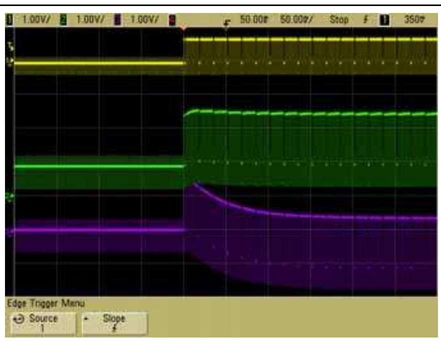
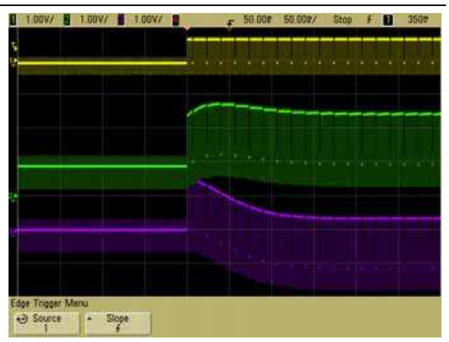
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

Input signal: White100% to Black, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

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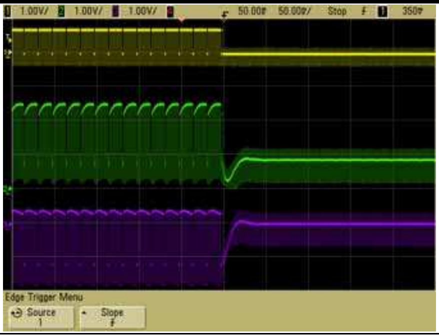
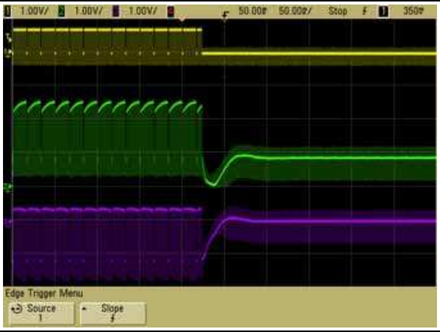
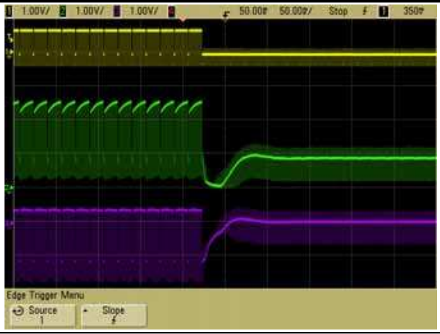
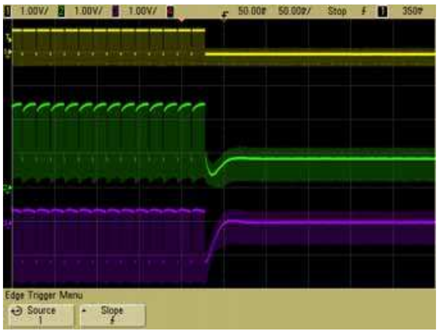
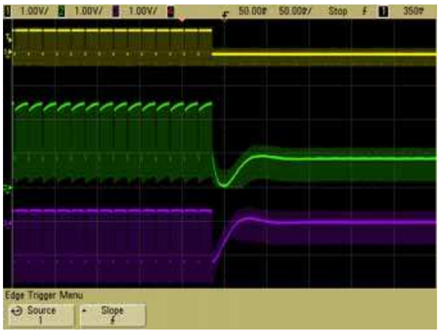
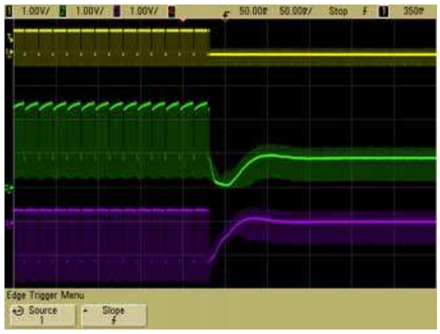
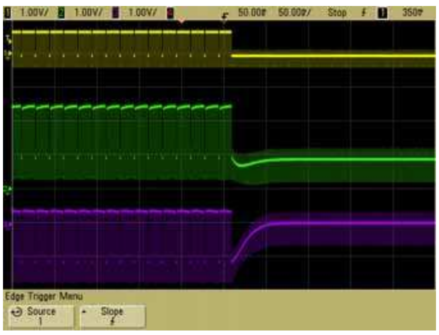
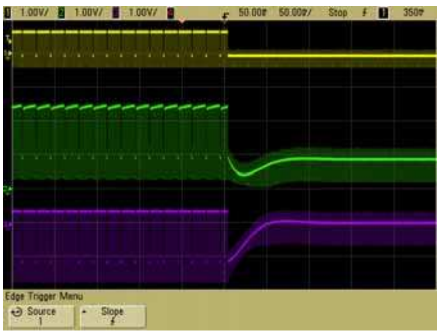
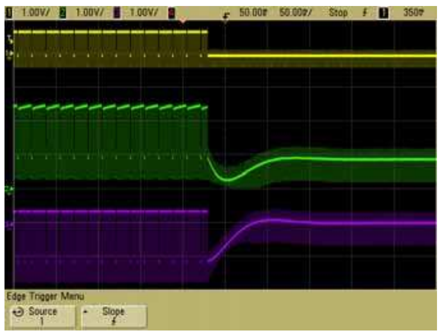
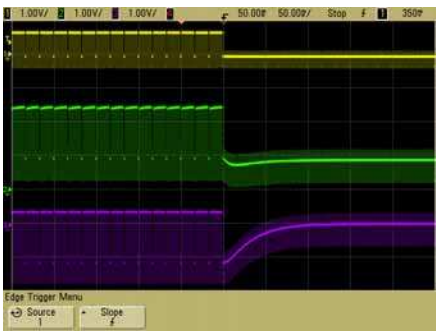
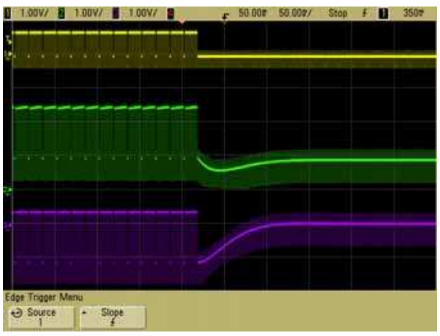
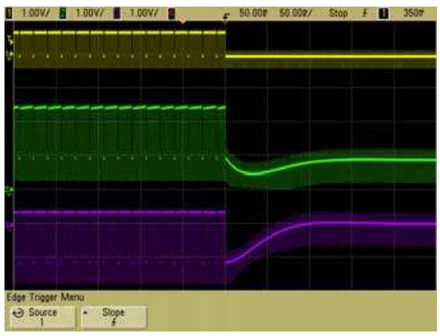
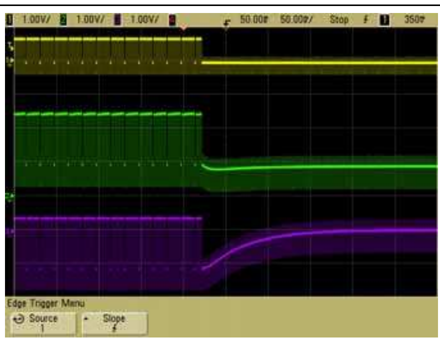
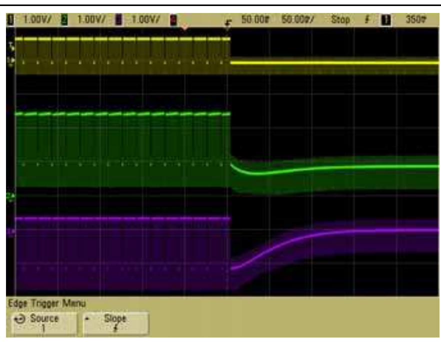
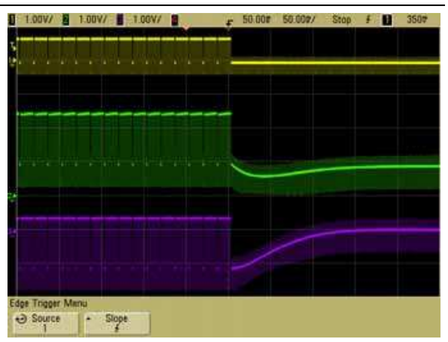
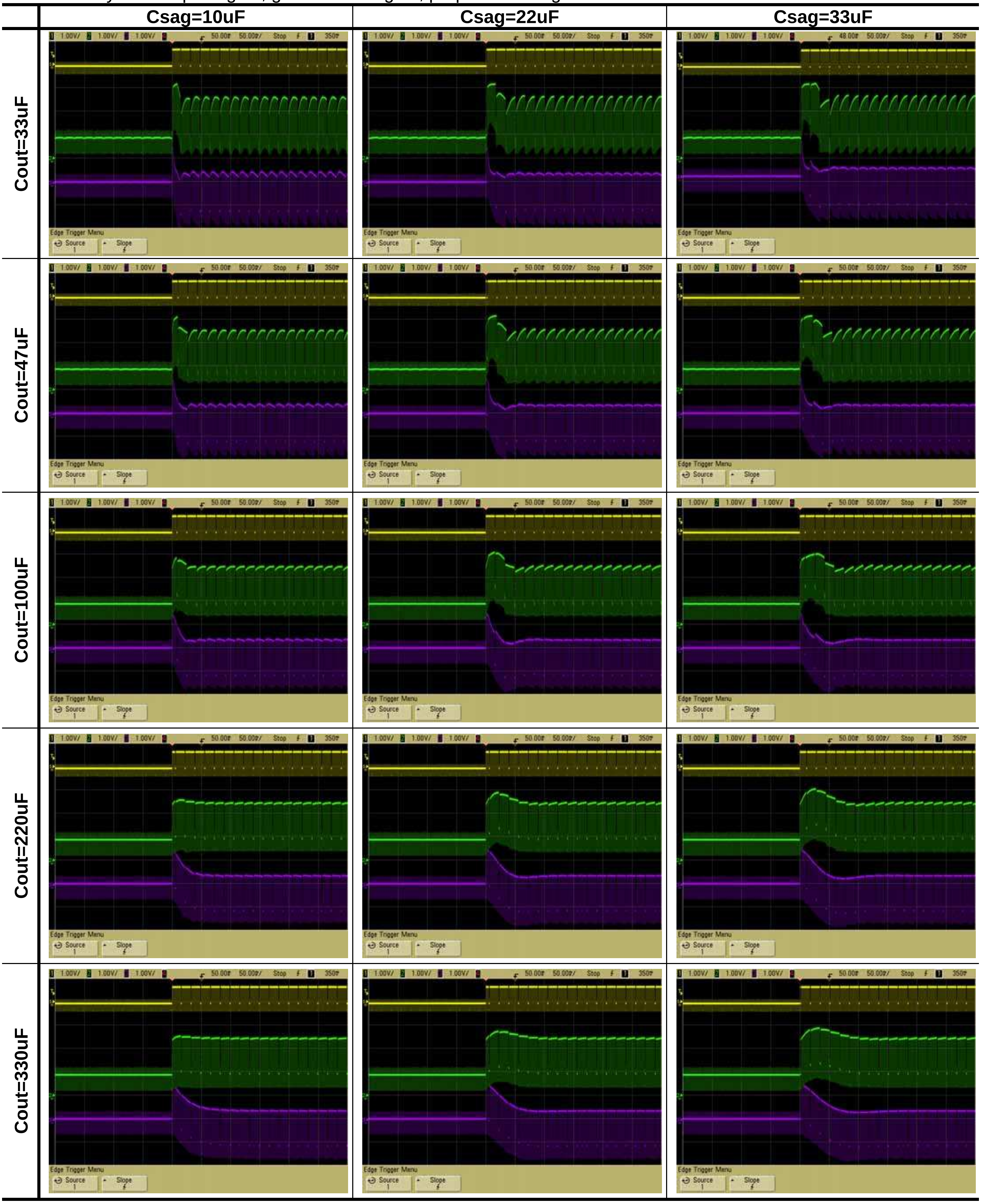
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >
Input signal: Black to White100%, resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: White100% to Black, resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

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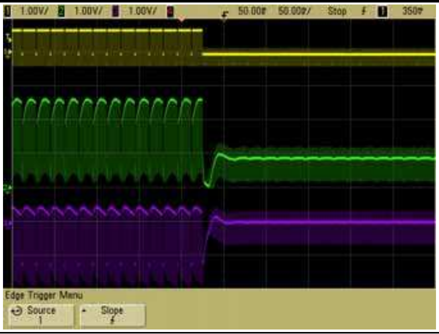
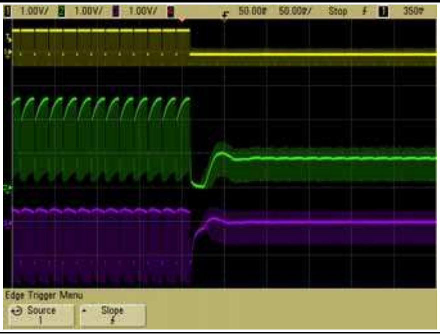
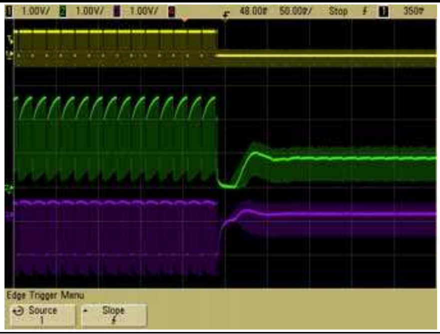
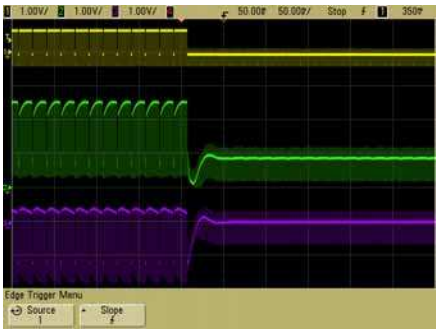
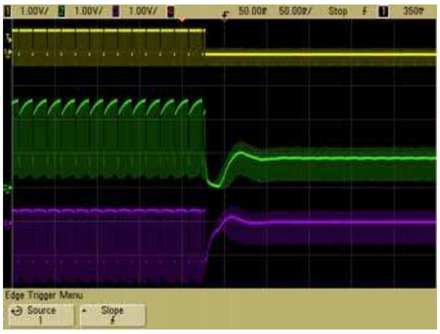
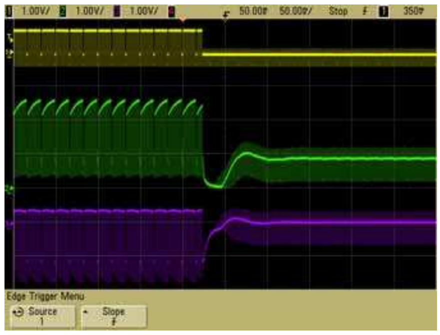
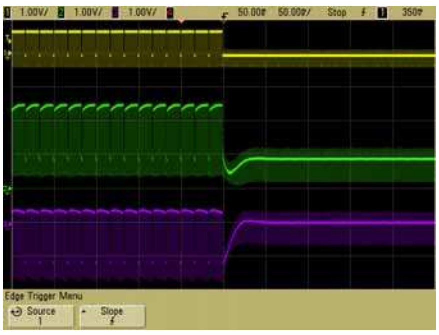
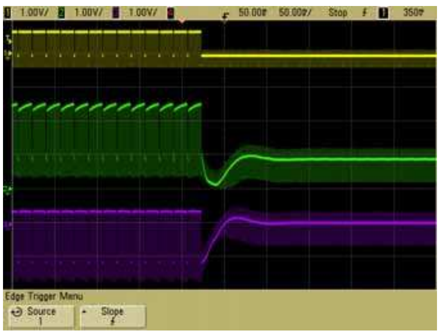
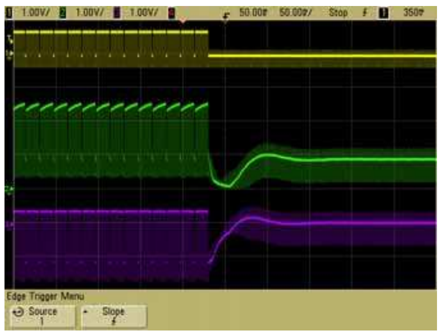
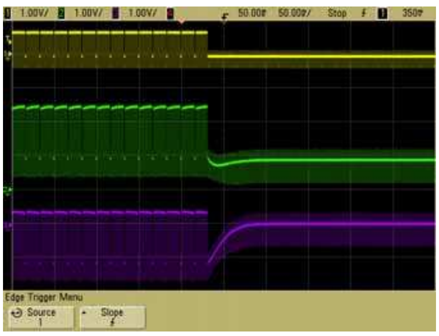
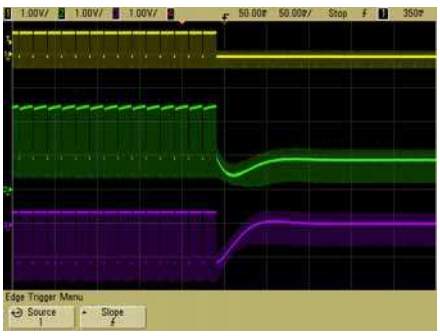
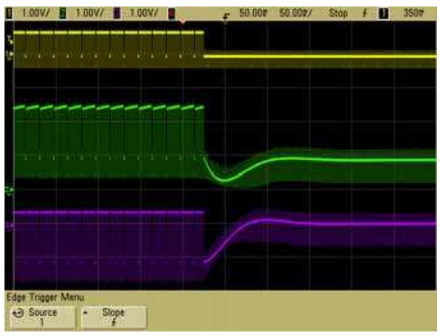
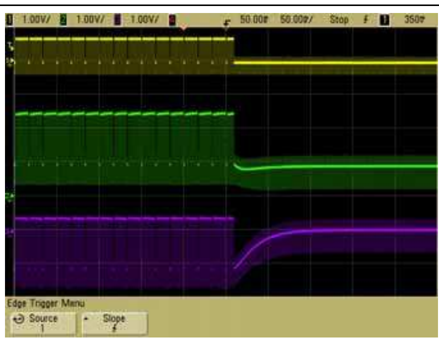
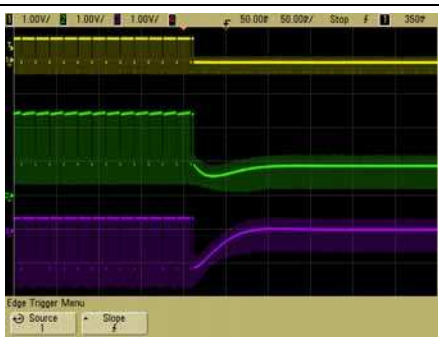
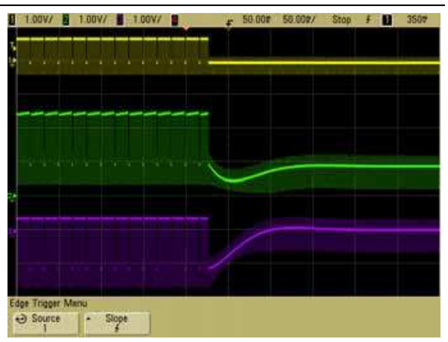
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

♦Clamp circuit

1. Operation of Sync-tip-clamp

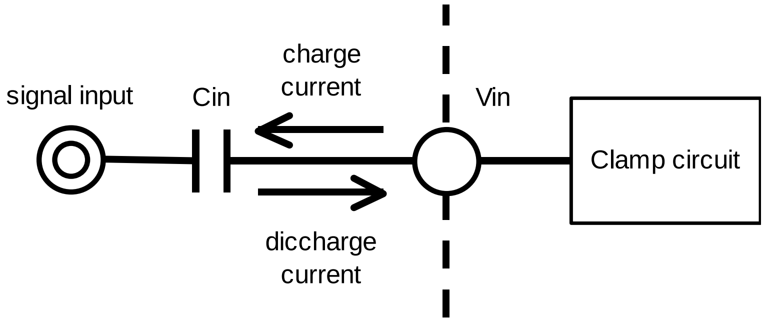
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input Cin. It is charged to the capacitor to the external input Cin at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor Cin at period other than the video signal sync tip. This is due to a small discharge current to the IC.

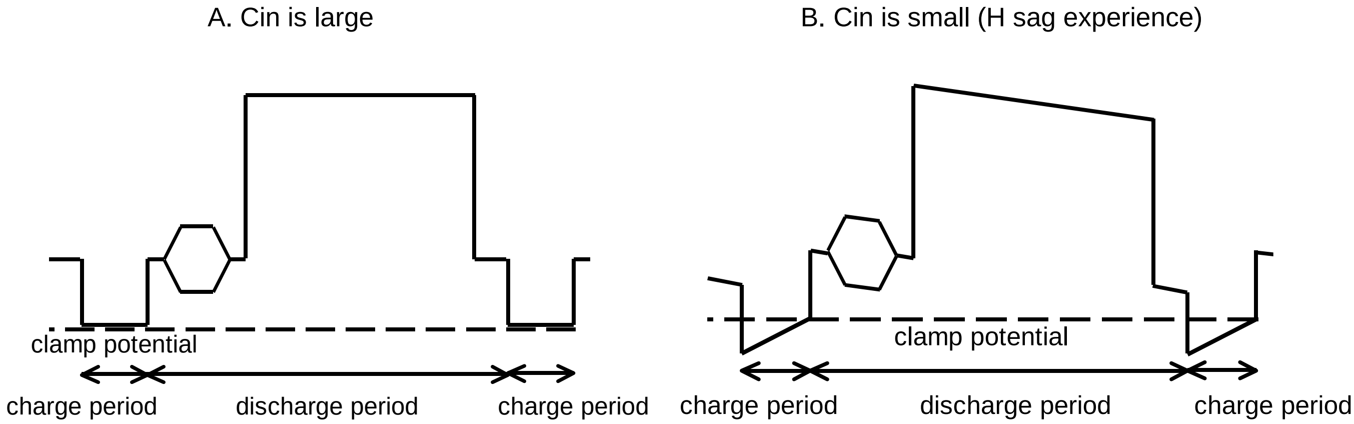
In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of Cin and discharging of Cin at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor Cin.

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1uF.



< Clamp circuit >



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

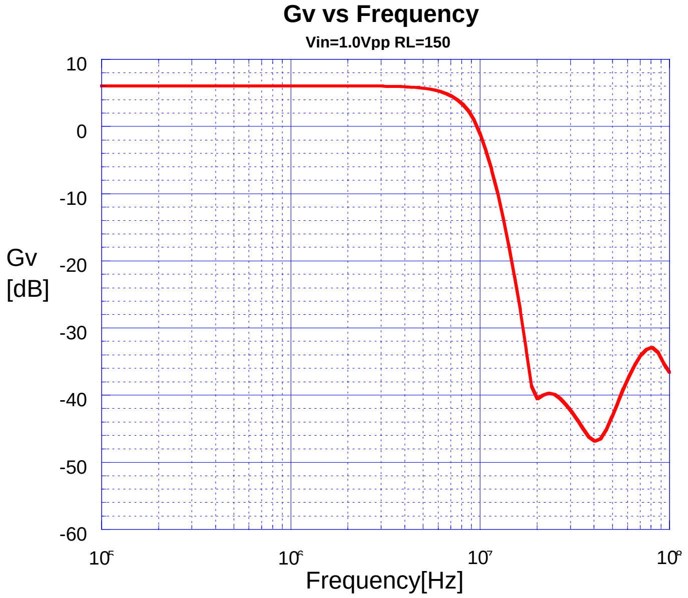
The input impedance of the charging period is a few kΩ. On the other hand, the input impedance of the discharge period is several MΩ. Because is a small discharge-current through to the IC.

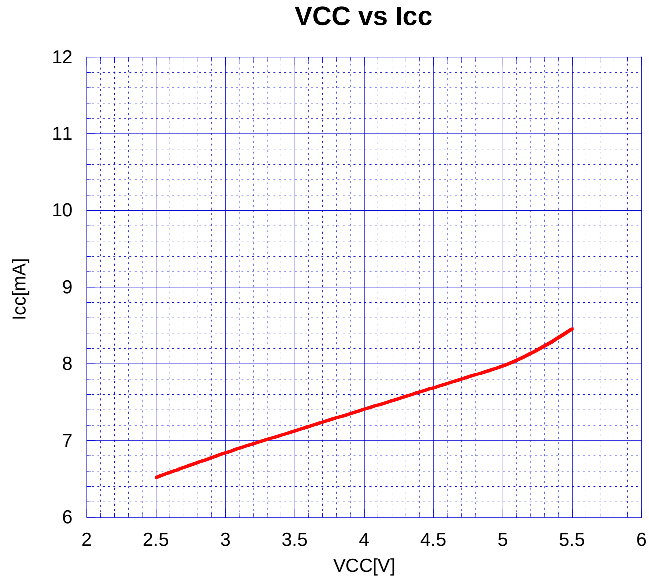
Thus the input impedance will vary depending on the operating state of the clamp circuit.

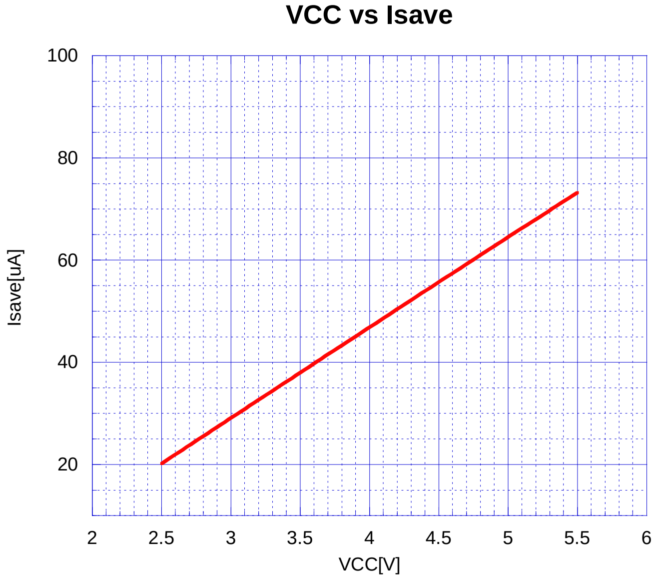
3. Impedance of signal source

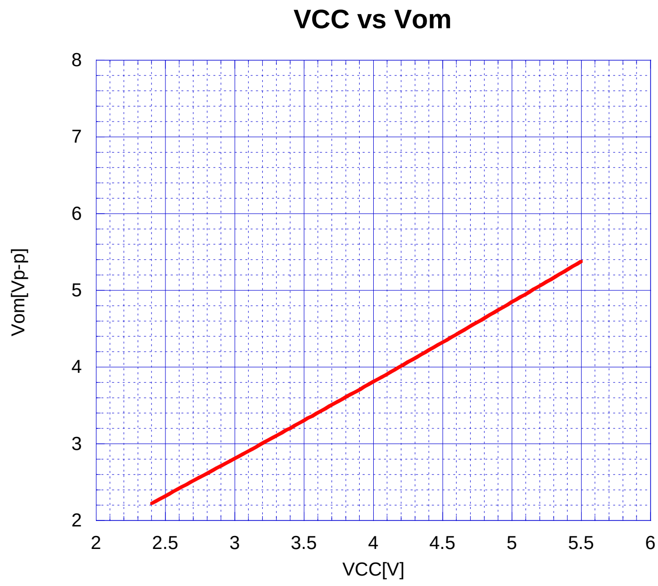
Source impedance to the input terminal, please lower than 200Ω. A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

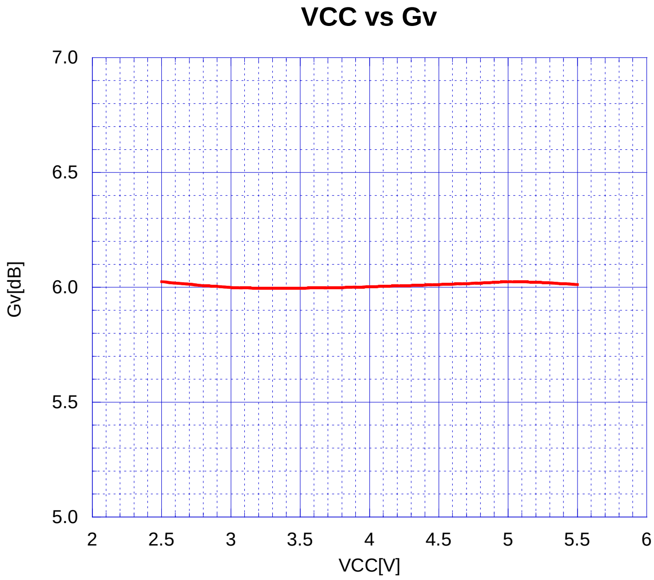
■TYPICAL CHARACTERISTICS



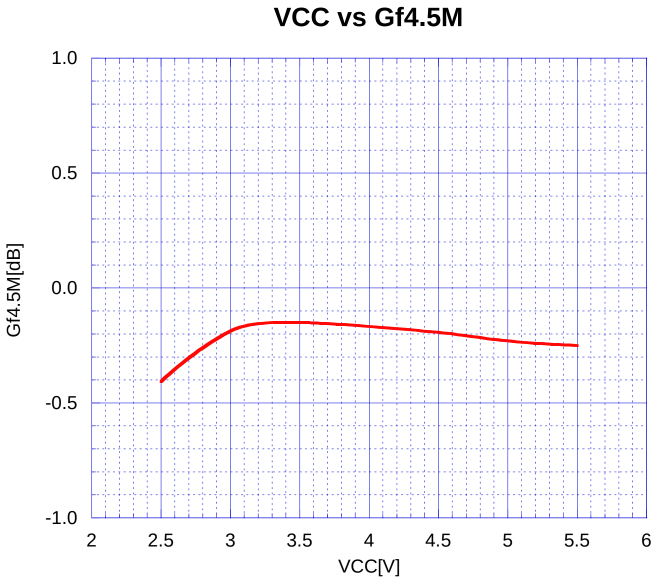


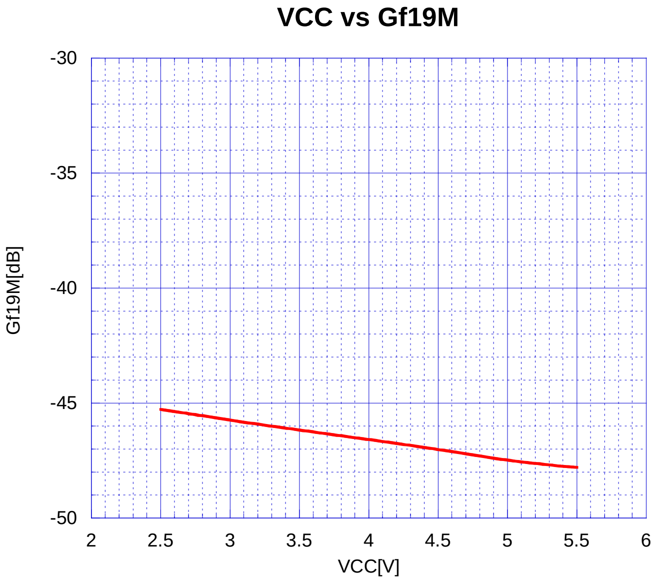


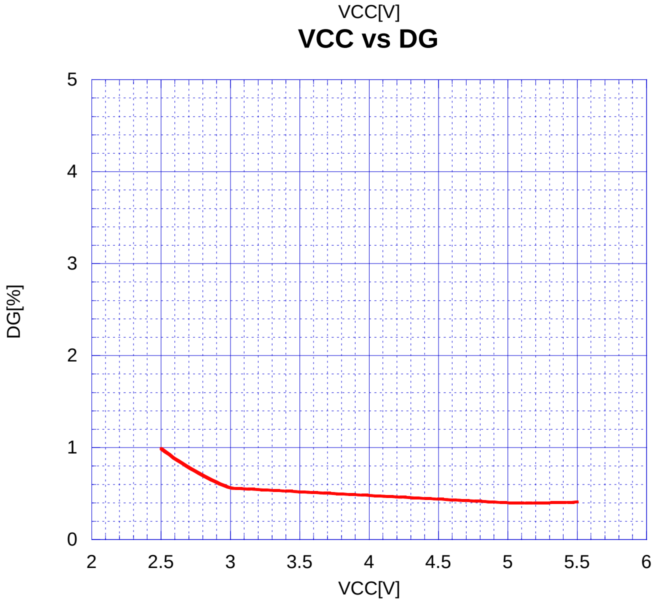


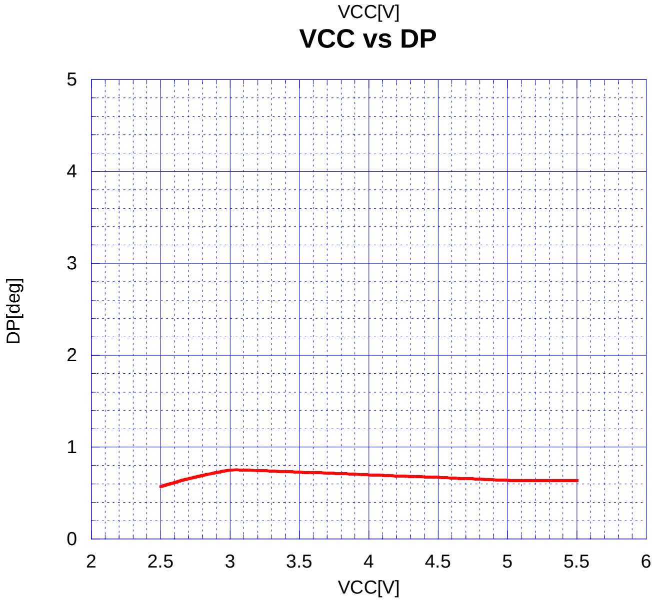


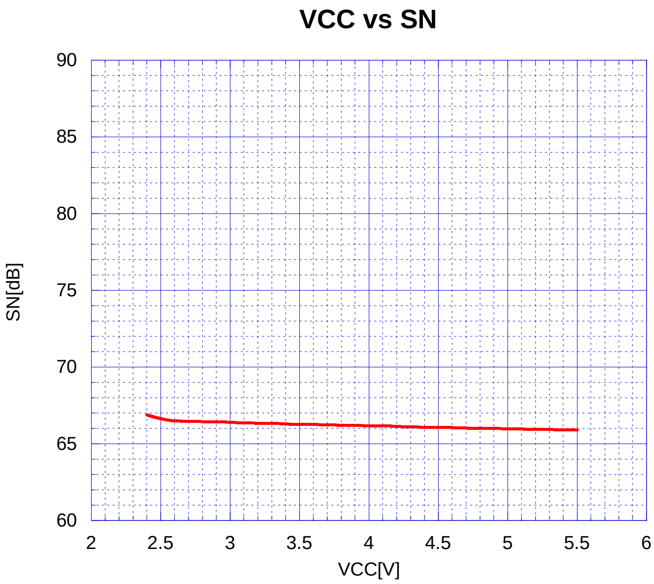
■TYPICAL CHARACTERISTICS

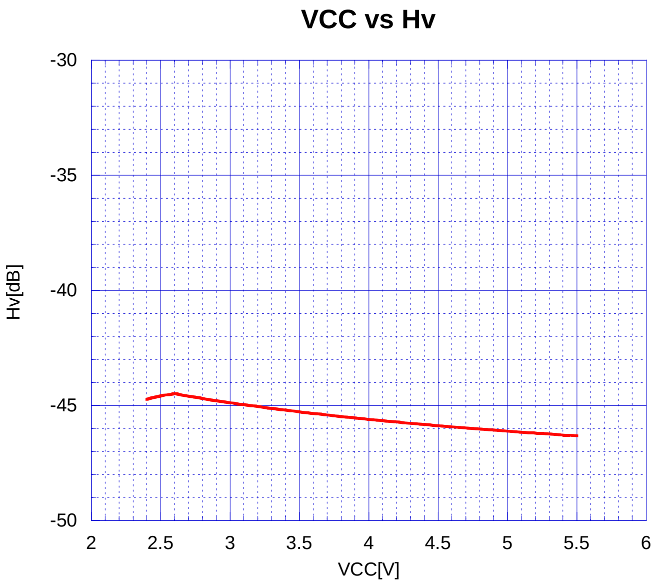












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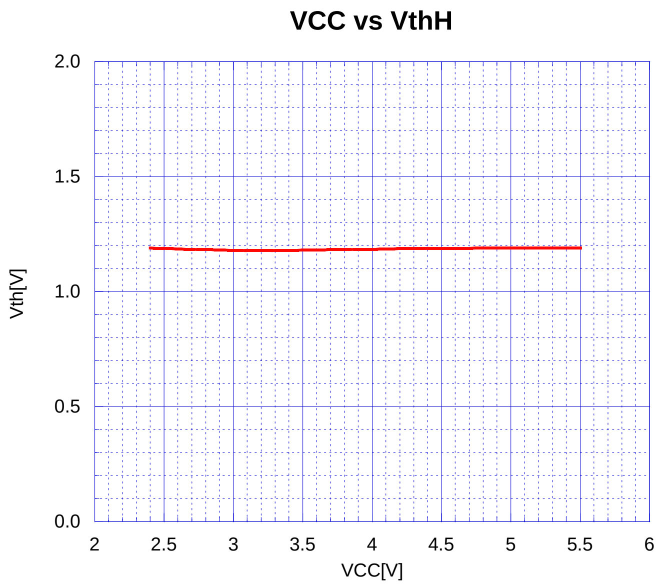

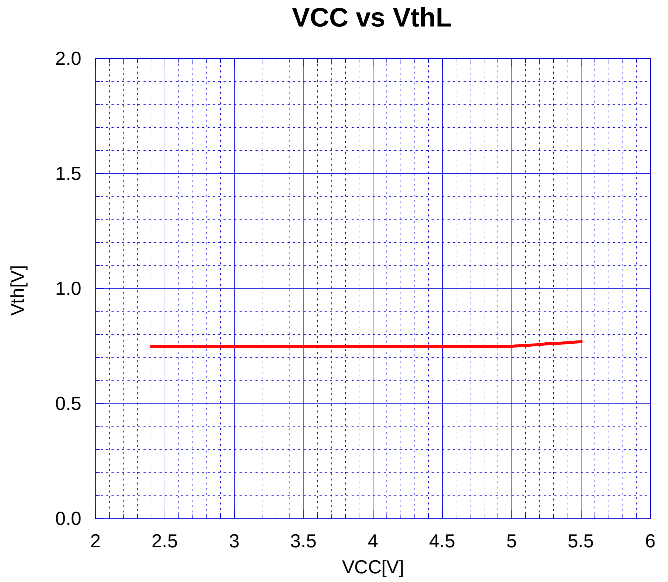

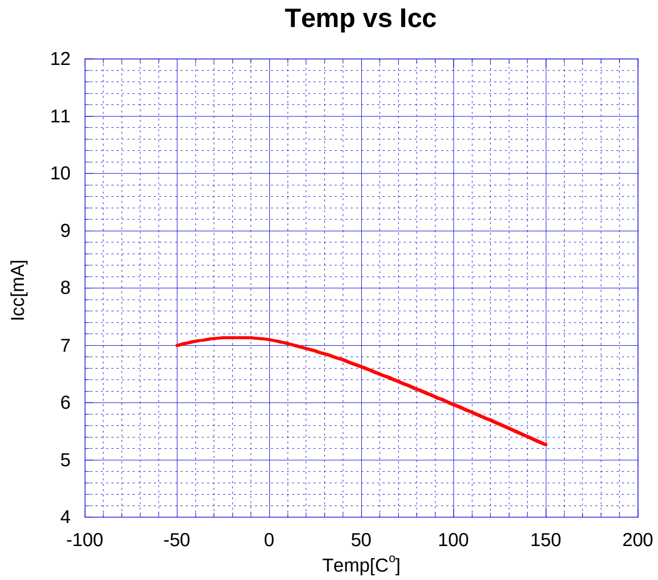

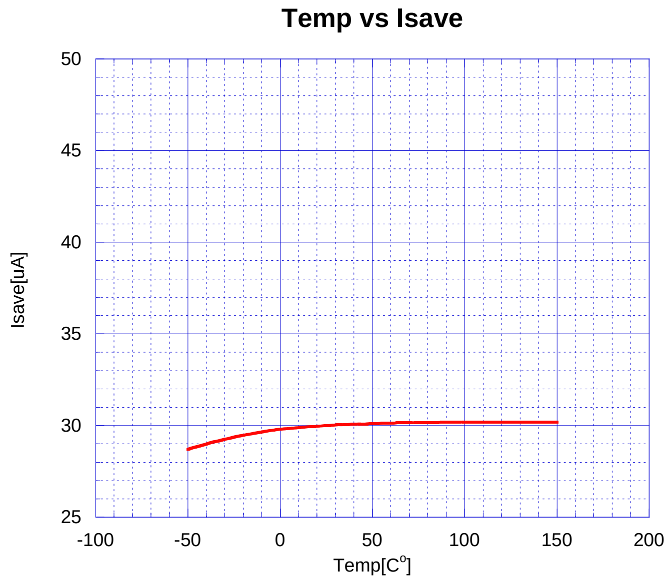

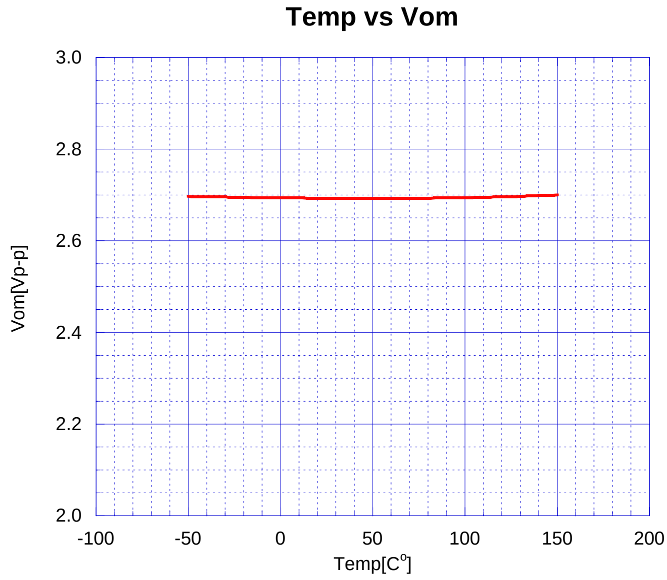

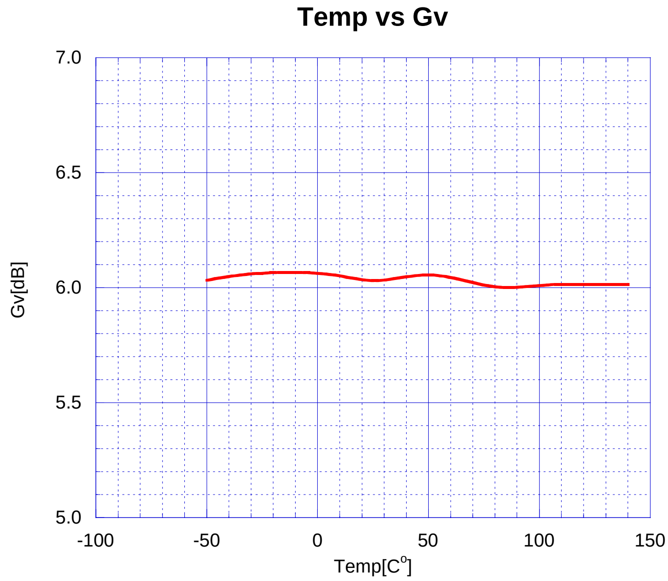

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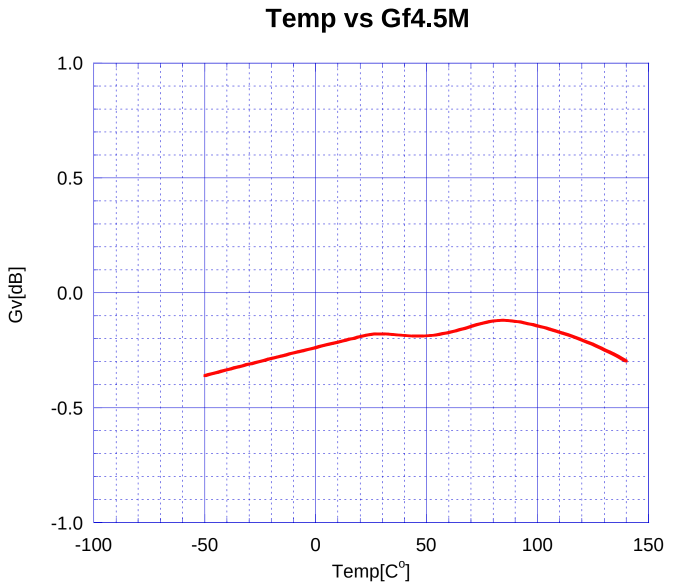

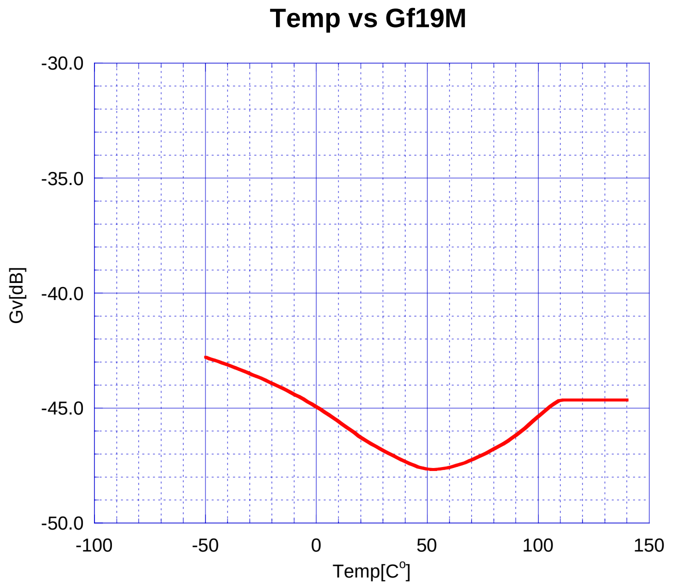

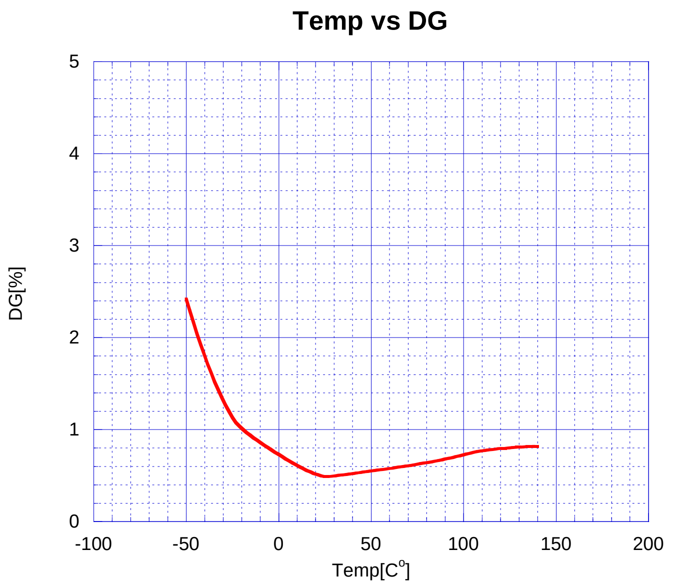

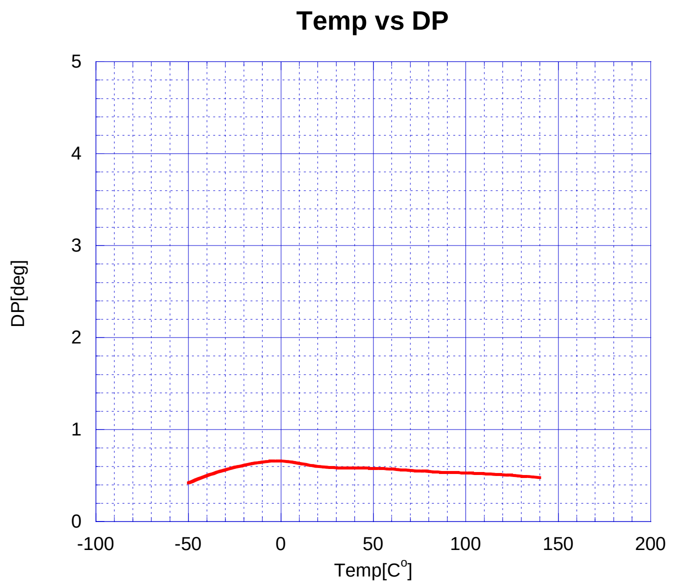

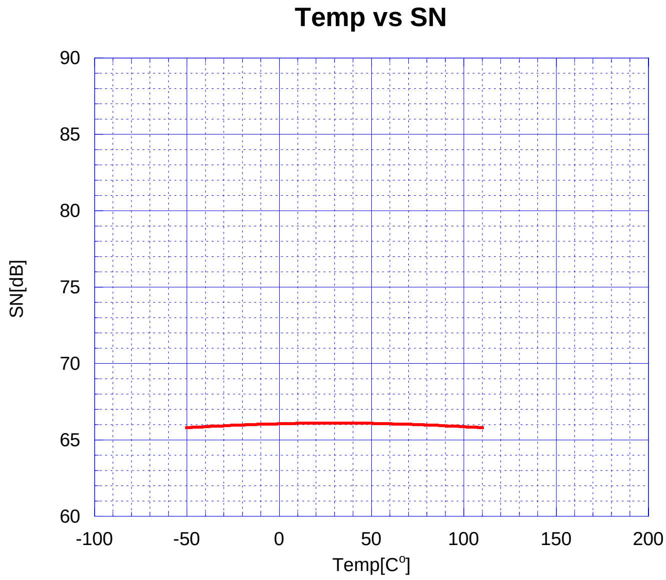

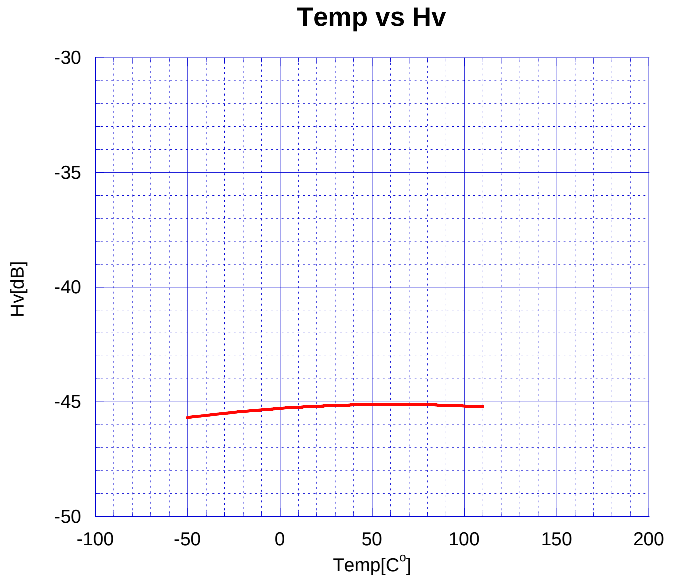

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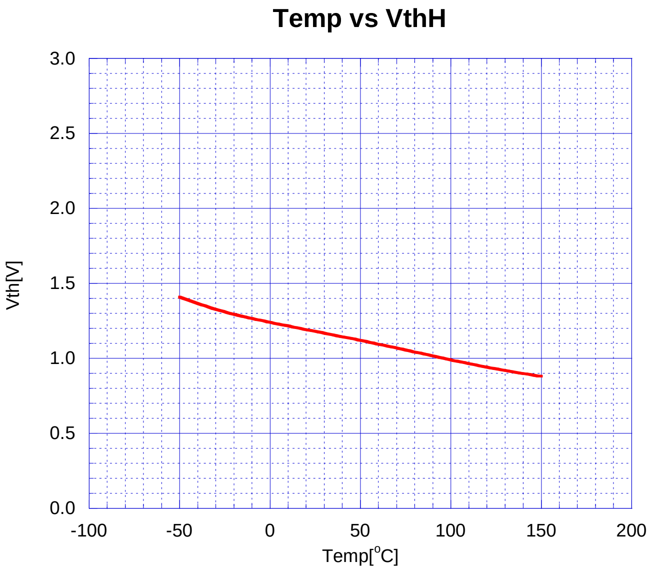

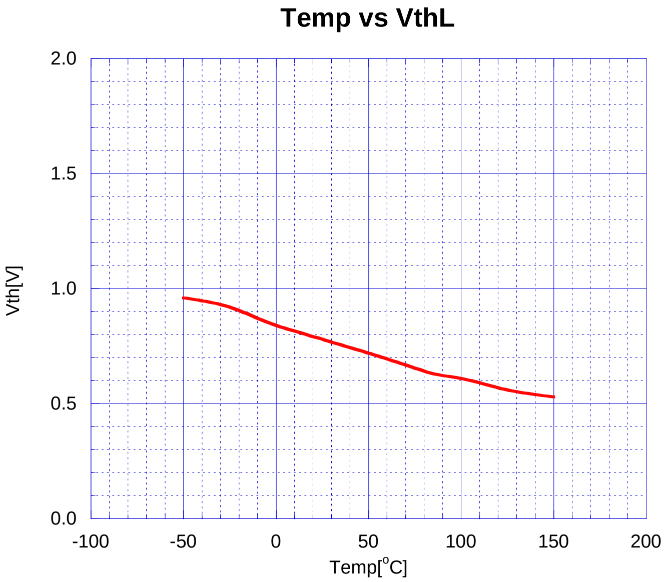

[CAUTION]
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