

30V/4A Half Bridge Driver

■ GENERAL DESCRIPTION

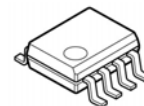
The **NJW4800** is a general purpose, half bridge power driver capable of supplying 4A current. The internal gate driver drives high-side/low-side power MOSFET; therefore, it has fast switching.

Additionally, it has protection features such as over current protection and thermal shutdown.

And in the case of failure, it can output a fault flag.

It is suitable for power switching applications of DSP/micro controller.

■ PACKAGE OUTLINE

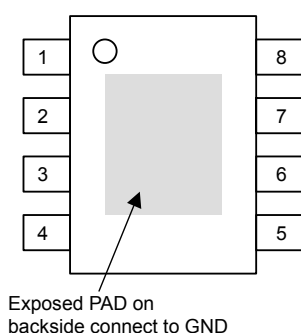


NJW4800GM1

■ FEATURES

- Output Switch Current $\pm 4A$
- Operating Voltage 7.5V to 30V
- Up to 1.2MHz Switching Frequency
- Thermal Shut Down
- Over Current Protection
- Under Voltage Lockouts
- Fault Indicator Output
- Stand-by Current $I_{QOFF} = 3\mu A$ (typ.)
- High Heat Radiation Package
- Package Outline HSOP8

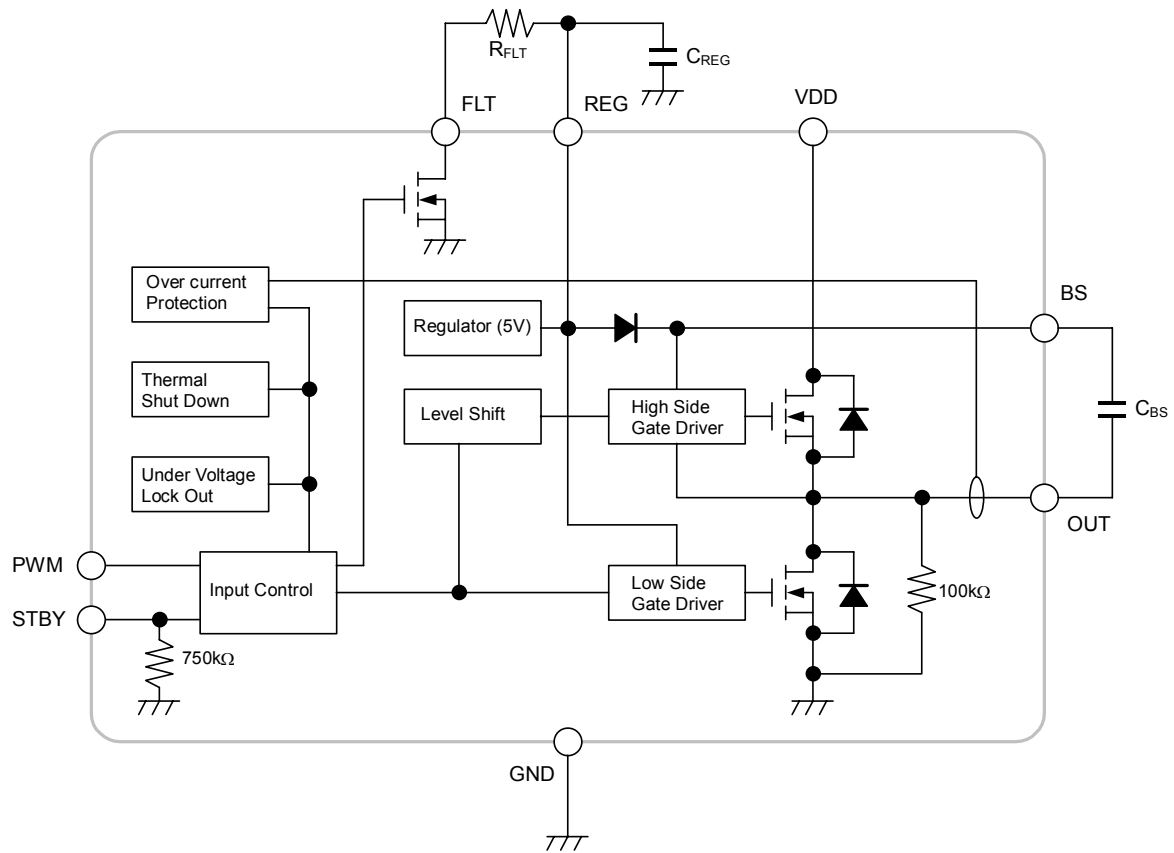
■ PIN CONFIGURATION



PIN FUNCTION

1. PWM
2. VDD
3. OUT
4. GND
5. BS
6. STBY
7. REG
8. FLT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Supply Voltage	V ⁺	35	V	VDD-GND Pin
Input Voltage	V _{STBY} V _{PWM}	-0.3 to 6	V	STBY, PWM-GND Pin
FLT Pin Voltage	V _{FLT}	-0.3 to 6	V	FLT-GND Pin
BS Pin Voltage	V _{BS}	40	V	BS-GND Pin
BS-OUT Pin Voltage	V _{BS-OUT}	-0.3 to 6	V	BS-OUT Pin
Power Dissipation	P _D	900 (*1) 3100 (*2)	W	—
Operating Junction Temperature	T _j	-40 to +150	°C	—
Operating Temperature Range	T _{opr}	-40 to +85	°C	—
Storage Temperature Range	T _{stg}	-50 to +150	°C	—

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Voltage	V _{opr}	7.5	—	30	V	VDD-GND Pin
Output Switch Current	I _{OM}	0	—	4	A	OUT Pin
Input Voltage	V _{STBY} , V _{PWM}	0	—	5.5	V	STBY, PWM-GND Pin
FLT Pin Voltage	V _{FLT}	0	—	V _{REG1}	V	FLT-GND Pin

■ THERMAL CHARACTERISTICS

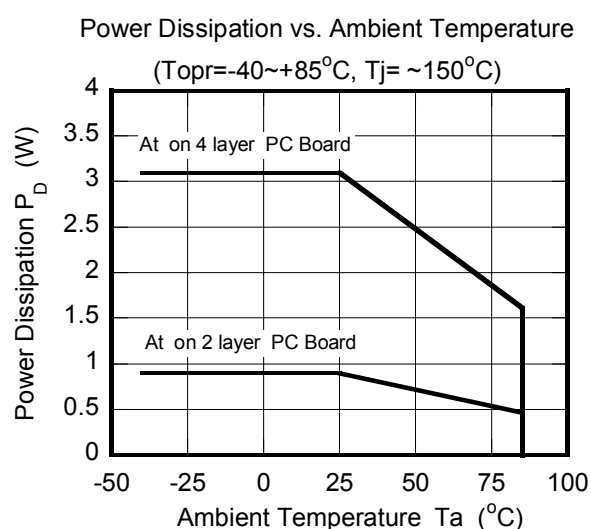
(Ta=25°C)

PARAMETER	SYMBOL	THERMAL RESISTANCE	UNIT
Junction-to-Ambient Temperature	θ _{ja}	139 (*1) 40 (*2)	°C/W
Junction-to-Case	ψ _{jt}	19 (*1) 3.7 (*2)	°C/W

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)



■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V^+=12V$, $V_{STBY}=0V$, $C_{BS}=0.1\mu F$, $C_{REG}=1\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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General Characteristics

Quiescent Current 1 (Operating)	I_{Q1}	$V_{PWM}=0V$	—	1	2	mA
Quiescent Current 2 (Switching)	I_{Q2}	$V_{PWM}=0V$ to $3V$, $f_{PWM}=1.2MHz$	—	9	14	mA
Quiescent Current 3 (Standby)	I_{QOFF}	$V_{STBY}=5.5V$, $V_{PWM}=0V$	—	3	10	μA

Output Block

High-side SW ON Resistance	R_{DSH}	$I_{OSOURCE}=1A$, $V_{BS-OUT}=5V$	—	0.25	0.45	Ω
Low-side SW ON Resistance	R_{DSL}	$I_{OSINK}=1A$	—	0.25	0.45	Ω
Over Current Limit	I_{LIMIT}	High-side and Low-side	4	5.5	7	A
Turn-on Time	t_r	$V_{PWM}=0V$ to $3V$	—	3	—	ns
Turn-off Time	t_f	$V_{PWM}=3V$ to $0V$	—	3	—	ns
Dead Time	Dt	$V_{PWM}=0V$ to $3V$	—	20	—	ns
PWM Rise Delay Time	t_{d_ON}	$V_{PWM}=0V$ to $3V$	—	60	—	ns
PWM Fall Delay Time	t_{d_OFF}	$V_{PWM}=3V$ to $0V$	—	60	—	ns
OUT Pin – VDD Pin Voltage Difference	V_{PDOV}	$V^+=5.7V$, $I_{ORH}=1A$	—	0.85	1.1	V
GND Pin – OUT Pin Voltage Difference	V_{PDGO}	$V^+=5.7V$, $I_{ORL}=1A$	—	0.85	1.1	V
Output Pull-down Resistance	R_{PD}	$V^+=5.7V$, $V_{STBY}=5.5V$	50	100	200	$k\Omega$
Output Leak Current (High Side SW OFF)	$I_{OLEAKOUT}$	$V^+=30V$, $V_{STBY}=5.5V$, $V_{OUT}=0V$	—	—	1	μA
OUT Pin Output Current (FLT Signal Output)	I_{O-FLT}	$V^+=5.7V$, $V_{OUT}=0V$	—	30	60	μA

Input Circuit Block

STBY Pin High Voltage (Standby Mode)	V_{IHSTBY}		2.4	—	5.5	V
STBY Pin Low Voltage (Operating Mode)	V_{ILSTBY}		0	—	0.8	V
STBY Pin Input Current	I_{ISTBY}	$V_{STBY}=5.5V$	4.8	7.33	14.7	μA
STBY Pull-down Resistance	R_{PD_STBY}		—	750	—	$k\Omega$
PWM Pin High Voltage	V_{IHPWM}		2.2	—	5.5	V
PWM Pin Low Voltage	V_{ILPWM}		0	—	0.9	V
PWM Pin Input Current	I_{IPWM}	$V_{PWM}=5.5V$	—	0.01	1	μA
Continuous Output High Time	t_{HPWM}	$V_{PWM}=5.5V$	140	300	—	μs

Under Voltage Lockout (UVLO) Block

UVLO Release Voltage	V_{UVLO2}	$V^+ = L \rightarrow H$	5.9	6.6	7.3	V
UVLO Operation Voltage	V_{UVLO1}	$V^+ = H \rightarrow L$	5.65	6.35	7.05	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	$V_{UVLO2}-V_{UVLO1}$	—	0.25	—	V

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V^+=12V$, $V_{STBY}=0V$, $C_{BS}=0.1\mu F$, $C_{REG}=1\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Internal Power Supply Circuit

Output Voltage 1	V_{REG1}	$I_{REG}=0mA$	4.75	5	5.25	V
Line Regulation	$\Delta V_{REG-VDD}$	$V^+=8$ to $30V$, $I_{REG}=0mA$	–	2	20	mV
Load Regulation	ΔV_{REG-IO}	$I_{REG}=0$ to $20mA$	–	20	50	mV
REG Pin Output Current	I_{OREG}	$V_{REG1}\times 0.95$, Input signal=500kHz	30	–	–	mA

Fault Function (FLT Pin)

Low Level Output Voltage	V_{LFLT}	$I_{FLT}=500\mu A$	–	0.25	0.5	V
OFF Leak Current	$I_{OLEAKFLT}$	$V_{FLT}=5.5V$	–	–	1	μA

■ PIN OPERATION TABLE

INPUT			OUTPUT			Mode
PWM	STBY	VDD	FLT	High-side SW	Low-side SW	
L	L	$V^+ \geq V_{UVLO2}$	ON	OFF	ON	Normal
H	L	$V^+ \geq V_{UVLO2}$	ON	ON (*3)	OFF	Normal
L	H	–	OFF	OFF	OFF	Stand-by
H	H	–	OFF	OFF	OFF	Stand-by
L	L	$V^+ < V_{UVLO1}$	OFF	OFF	OFF	UVLO
H	L	$V^+ < V_{UVLO1}$	OFF	OFF	OFF	UVLO

(*3): If PWM=H continues by t_{HPWM} or more, it becomes low-side SW=ON during $t_{HPWM}/128$.

INPUT		OUTPUT			Mode
T_j	I_{OUT}	FLT	High-side SW	Low-side SW	
$T_j > 150^\circ C$	–	OFF	OFF	OFF	TSD
–	$I_{OM} \geq I_{LIMIT}$	OFF	OFF	OFF	OCP

■ TIMING CHART

Fig1. Turn-on/Turn-off Time, PWM Rise/Fall Delay Time

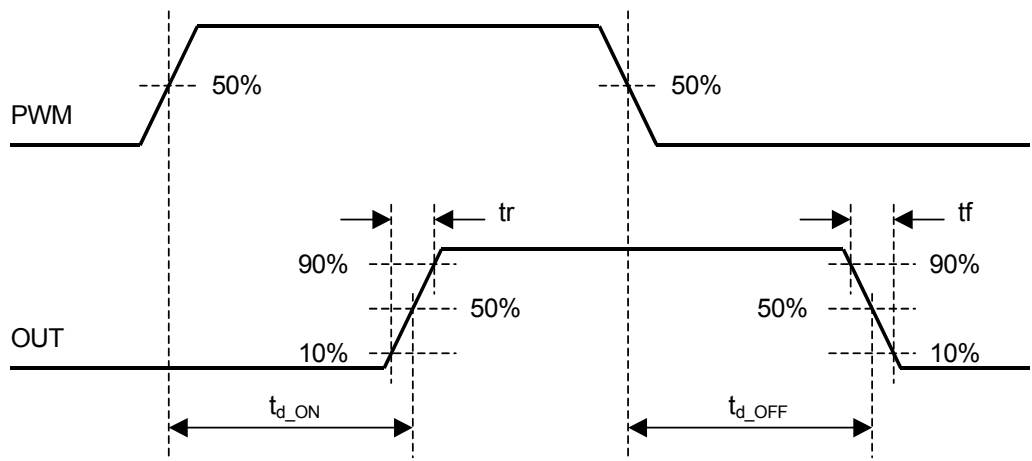


Fig2. Maximum Continuous Output Time (High-level)

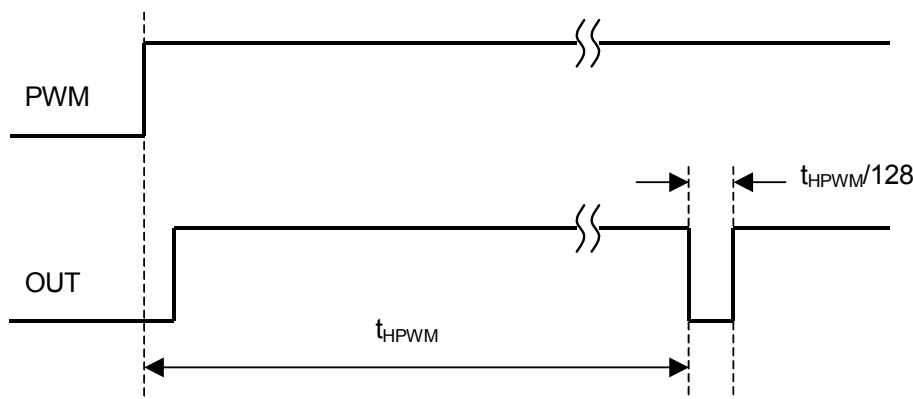
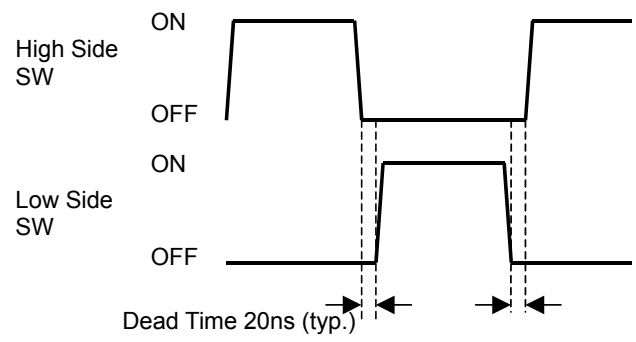
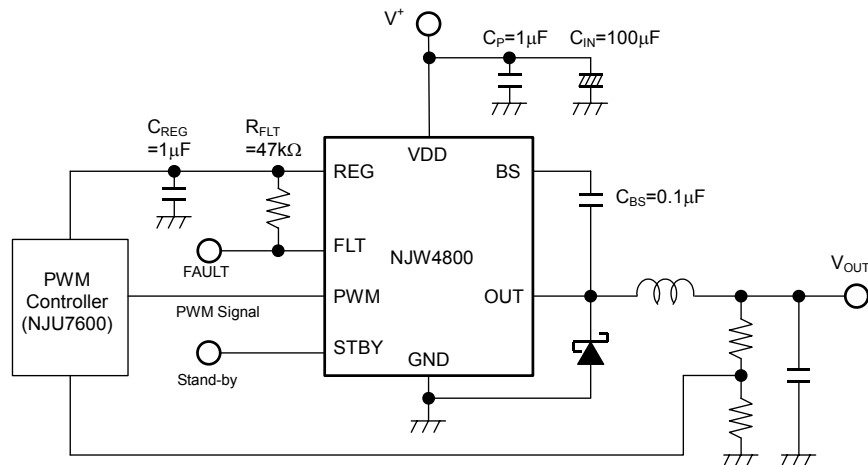


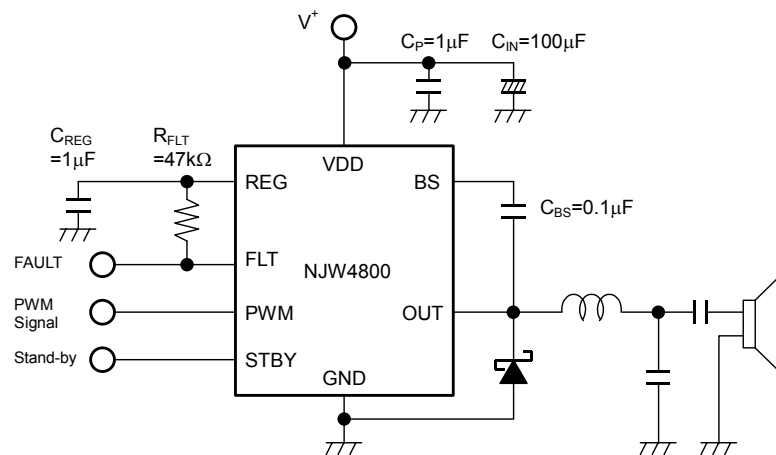
Fig3. Switching and Dead Time



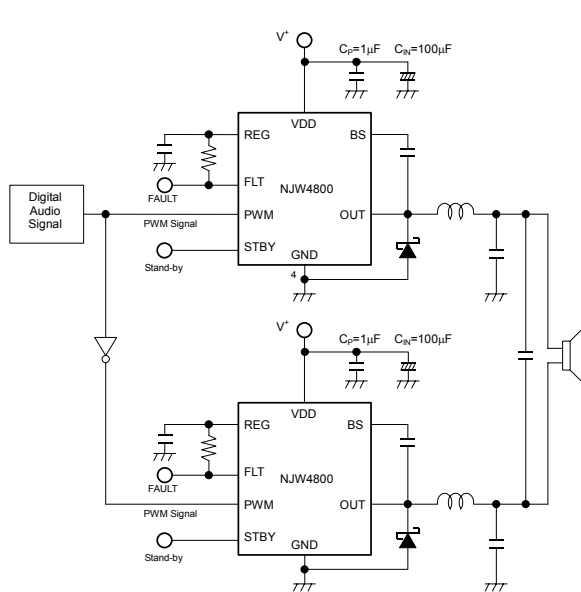
■ TYPICAL APPLICATIONS



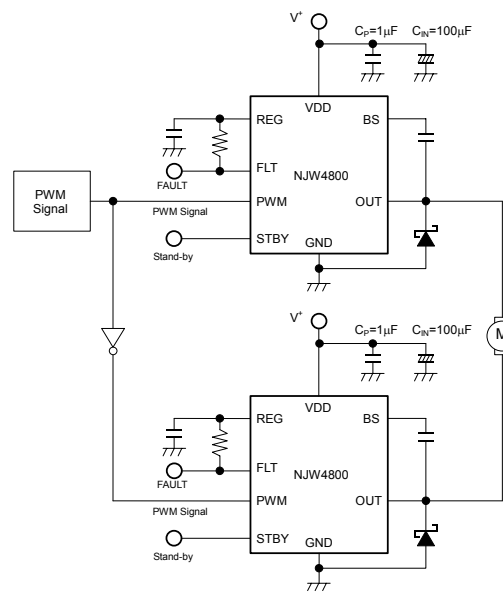
Synchronous PWM step down switching regulator



Class-D single ended audio amplifier



Class-D full bridge audio amplifier



Full bridge motor driver