

High Voltage Low current consumption Regulator

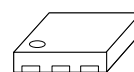
■ GENERAL DESCRIPTION

The NJW4180 is a high voltage and low current consumption linear regulator.

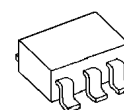
Low current consumption make the NJW4180 possible to supply 2.5 to 5.0 V regulated voltage from high voltage input.

Therefore, it is suitable for a power supply for micro controllers, battery related applications, LED and other applications where low power consumption is essential.

■ PACKAGE OUTLINE



NJW4180KG1

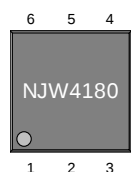


NJW4180F

■ FEATURES

- Operating Voltage Range 35V (max.)
- Low Current Consumption 9 μ A (typ.)
- MLCC correspond
- Output Current $I_O(\text{min.})=20\text{mA}$
- High Precision Output $V_O \pm 1.5\%$
- Internal Thermal Overload Protection
- Internal Over Current Protection
- Internal Reverse Current Protection
- Package Outline ESON6-G1, SOT23-5

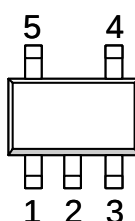
■ PIN CONNECTION



NJW4180KG1

PIN CONFIGURATION

1. N.C.
2. GND
3. N.C.
4. V_{IN}
5. N.C.
6. V_{OUT}

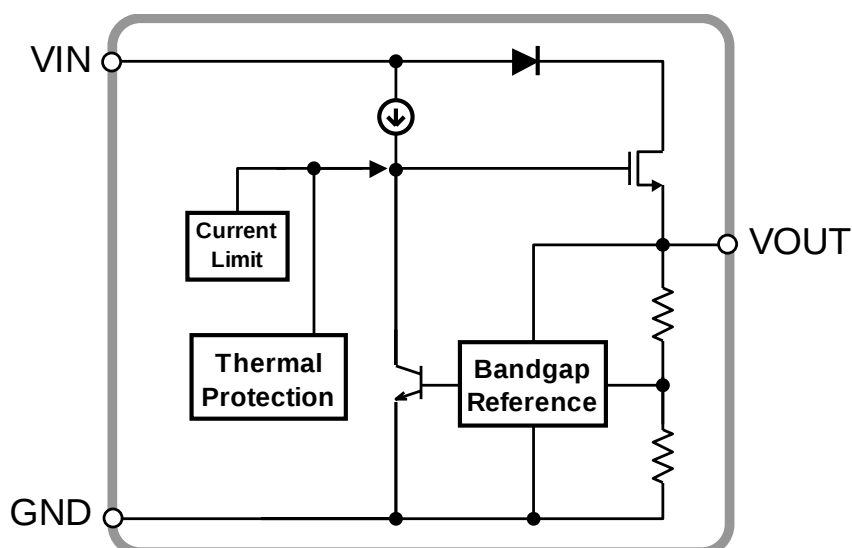


NJW4180F

PIN CONFIGURATION

1. N.C.
2. GND
3. N.C.
4. V_{OUT}
5. V_{IN}

■ BLOCK DIAGRAM



NJW4180

■ OUTPUT VOLTAGE LANK LIST

Device Name	V _{OUT}	Device Name	V _{OUT}
NJW4180F25	2.5V	NJW4180KG1-25	2.5V
NJW4180F33	3.3V	NJW4180KG1-33	3.3V
NJW4180F05	5.0V	NJW4180KG1-05	5.0V

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V _{IN}	+40	V
Output Voltage	V _{OUT}	+7	V
Power Dissipation	P _D	ESON6-G1	330 (*1)
			905 (*2)
		SOT-23-5	390 (*3)
			520 (*4)
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-50 to +125	°C

(*1): Mounted on glass epoxy board based on EIA/JEDEC STANDARD.

(101.5×114.5×1.6mm: 2Layers with Exposed Pad FR-4)

(*2): Mounted on glass epoxy board based on EIA/JEDEC STANDARD.

(101.5×114.5×1.6mm: 4Layers with Exposed Pad FR-4, Internal foil area size: 99.5×99.5mm, Applying a thermal via hole to a board based on JEDEC standard JESD51-5)

(*3): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm: 2Layers FR-4)

(*4): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm: 4Layers FR-4)

■ PROTECTION CIRCUIT

Over Current Protection

Thermal Shutdown

Reverse Current Protection

■ INPUT VOLTAGE RANG

V_O≤3V: V_{IN} = +5.5V to +35V

V_O>3V: V_{IN} = V_O+2.5V to +35V

■ ELECTRICAL CHARACTERISTICS

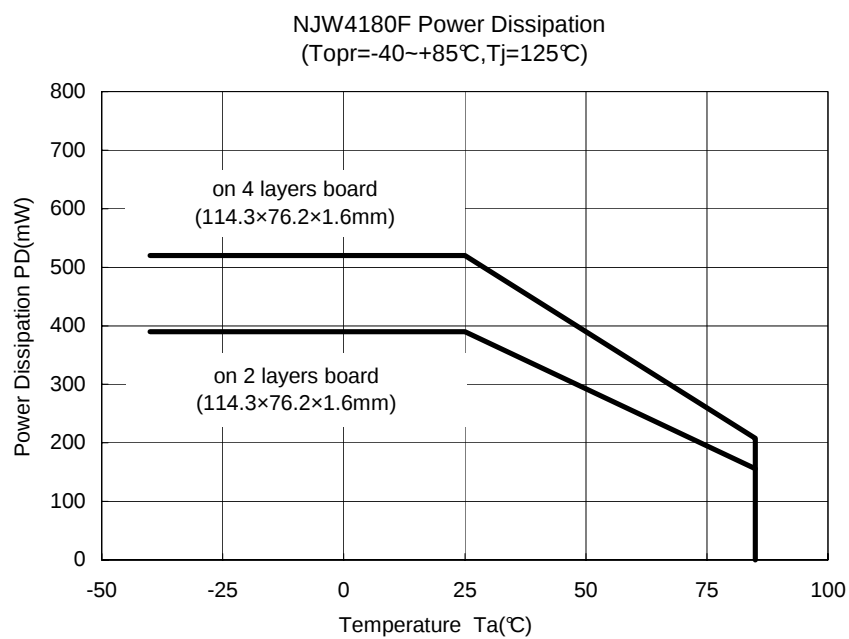
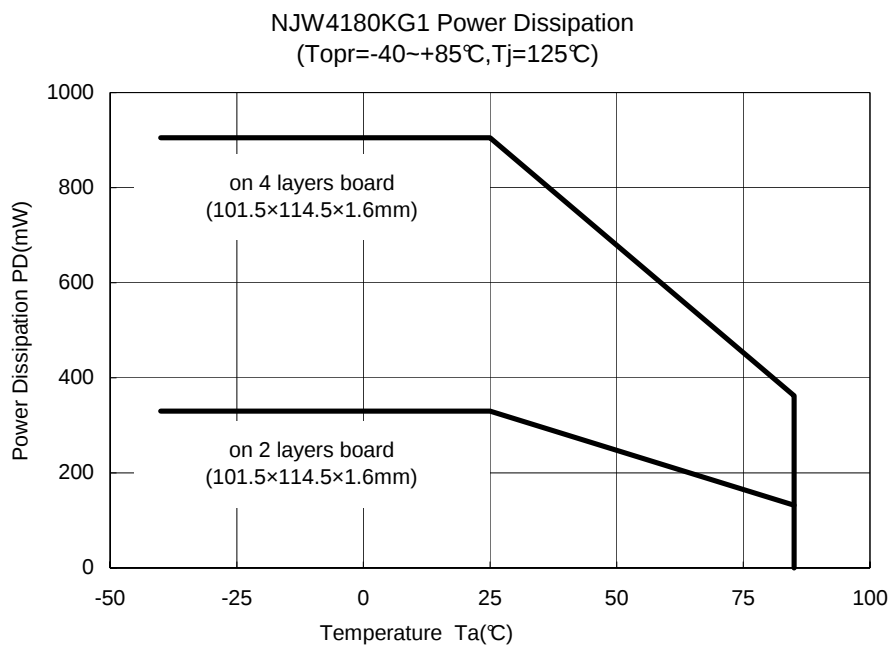
(Unless otherwise specified, $V_{IN}=V_O+2.5V$ ($V_O \leq 3V$: $V_{IN}=5.5V$), $C_{IN}=0.1\mu F$, $C_O=1\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	$I_O=10mA$	-1.5%	-	+1.5%	V
Quiescent Current	I_Q	$I_O=0mA$	-	9	15	μA
Output Current	I_O	$V_O \times 0.9$	20	30	-	mA
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 5.5V$ to $35V$, $I_O=10mA$ ($V_O \leq 3V$) $V_{IN} = V_O+2.5V$ to $35V$, $I_O=10mA$ ($V_O > 3V$)	-	0.02	0.05	%/V
Load Regulation	$\Delta V_O / \Delta I_O$	$I_O=0mA$ to $20mA$	-	0.005	0.02	%/mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T_a$	$T_a=0$ to $85^\circ C$, $I_O=10mA$	-	± 100	-	ppm/ $^\circ C$
Sink Current under Reverse Current Protection operating	$I_{REVERSE}$	$V_{IN} = 0V$, $V_O = 5V$	-	50	75	μA
Input Voltage	V_{IN}	$V_O \leq 3V$	5.5	-	35	V
		$V_O > 3V$	$V_O+2.5$	-	35	

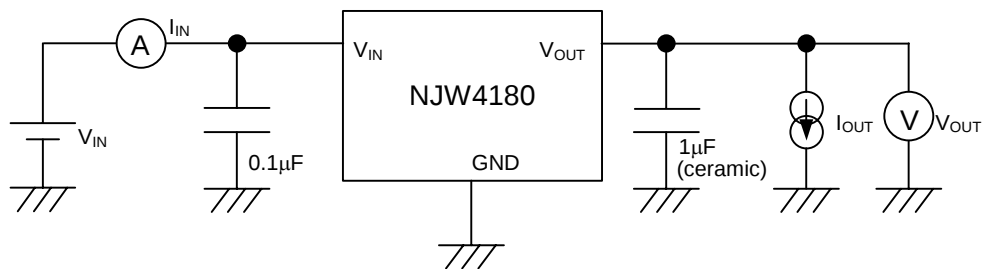
The above specification is a common specification for all output voltages.

Therefore, it may be different from the individual specification for a specific output voltage.

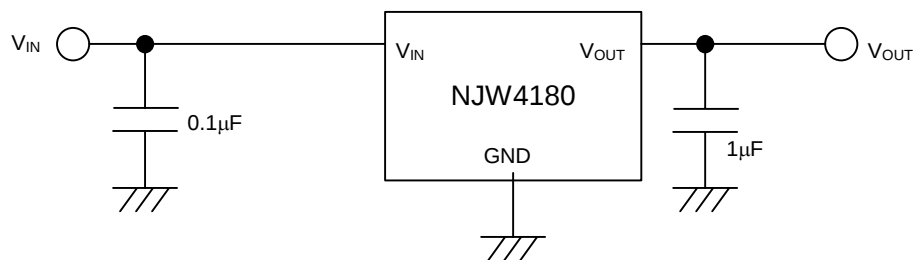
POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ TEST CIRCUIT



■ TYPICAL APPLICATION



*Input Capacitance C_{IN}

Input Capacitance (C_{IN}) is required to prevent oscillation and reduce power supply ripple for applications with high power supply impedance or a long power supply line.

Use the C_{IN} value of $0.1\mu\text{F}$ greater to avoid the problem.

C_{IN} should connect between GND and V_{IN} as short as possible.

*Output Capacitance C_O

Output capacitor (C_O) is required for a phase compensation of the internal error amplifier. The capacitance and the equivalent series resistance (ESR) influences stability of the regulator.

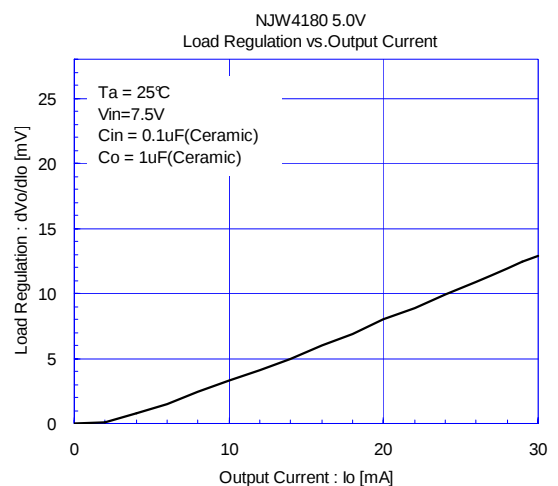
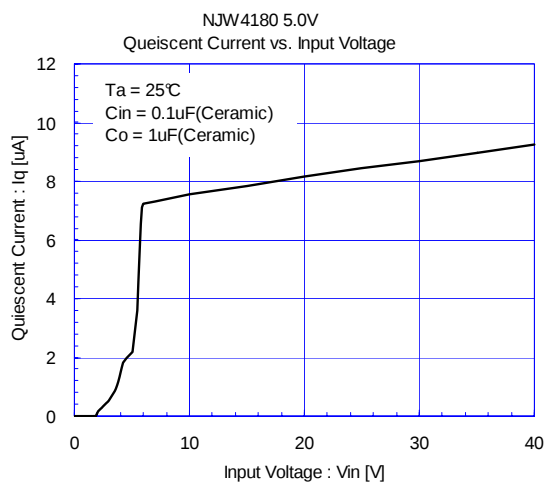
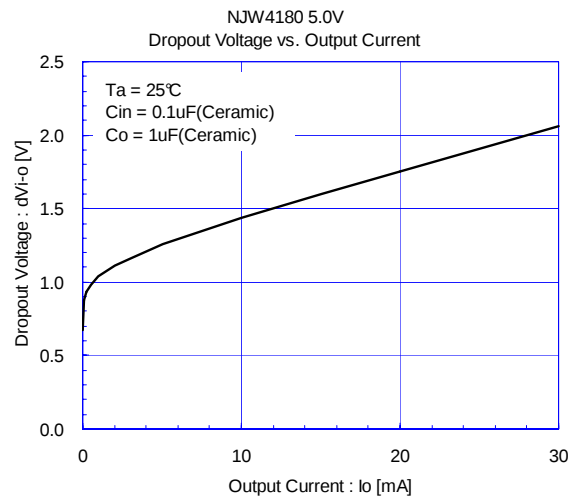
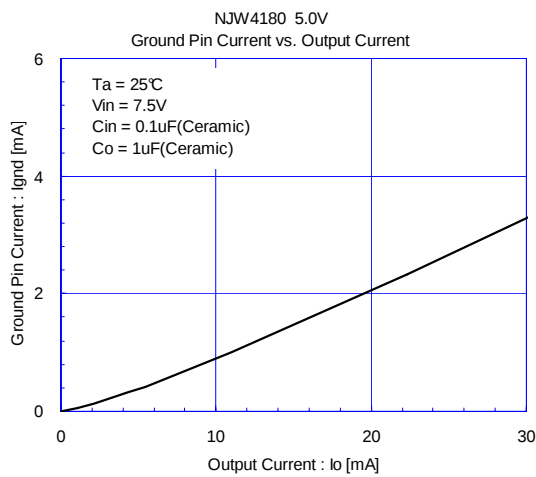
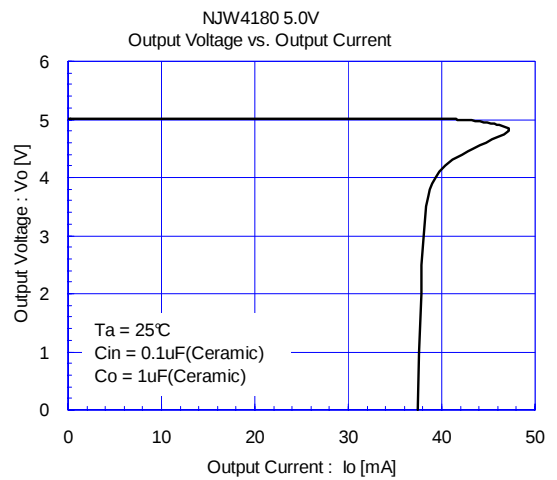
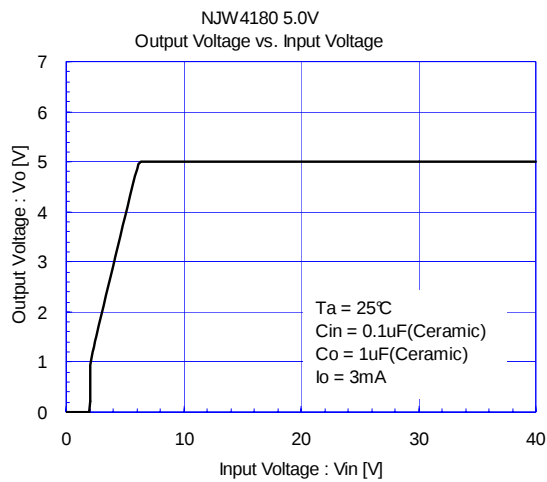
This product is designed to work with a low ESR capacitor for the C_O ; however, use of recommended capacitance or greater value is essential for stable operation.

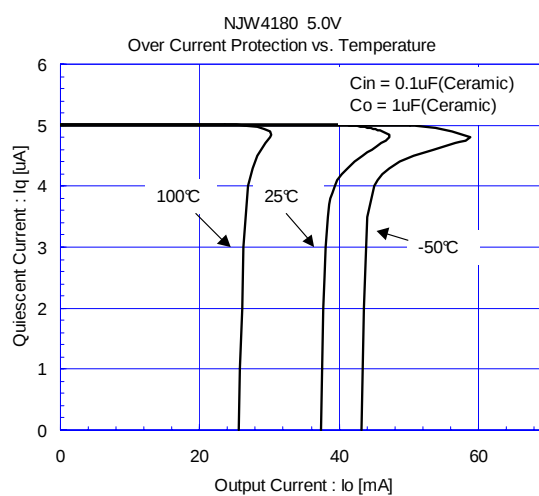
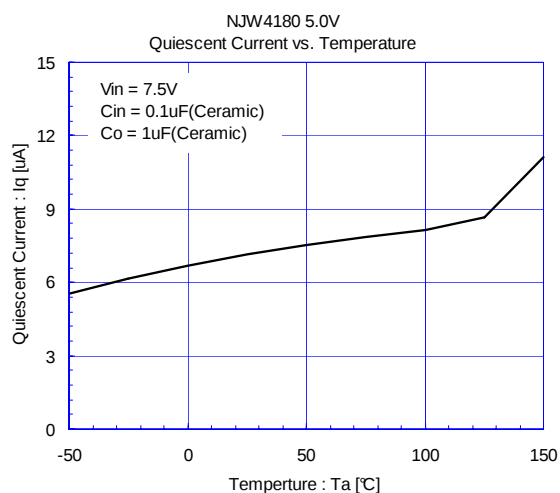
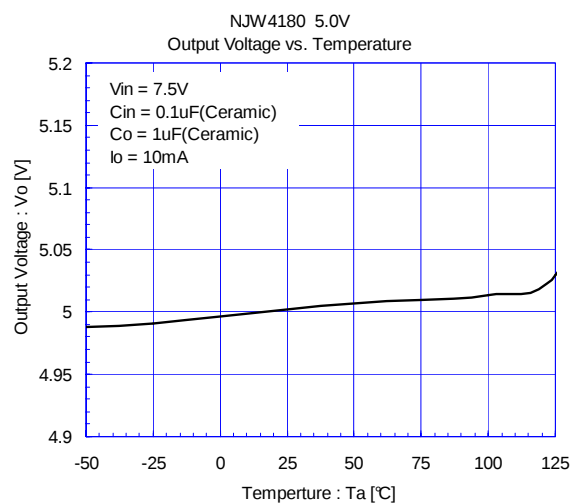
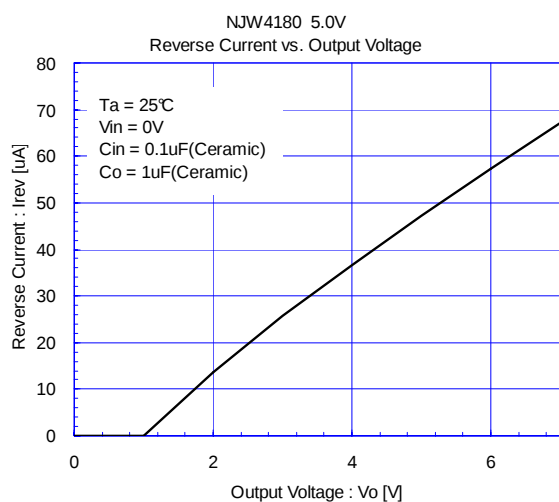
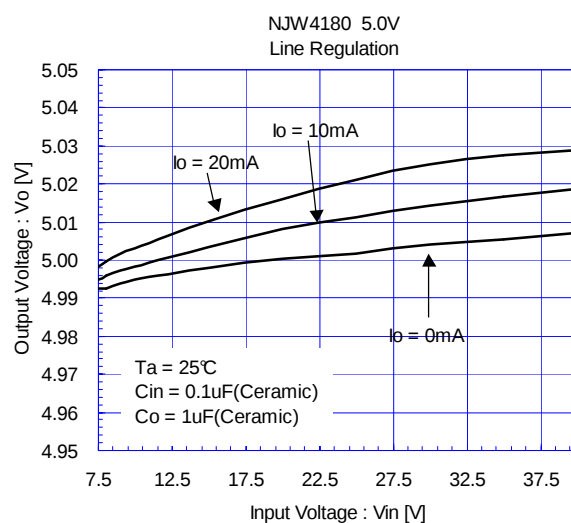
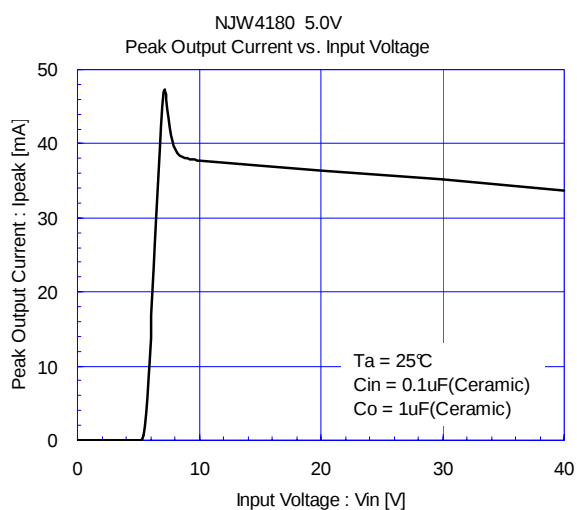
Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

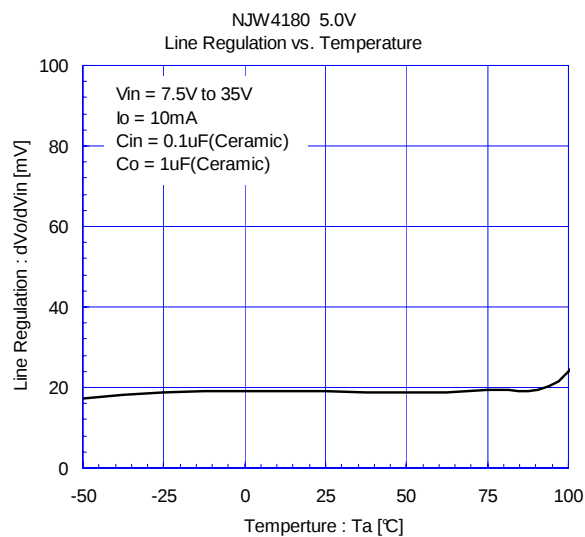
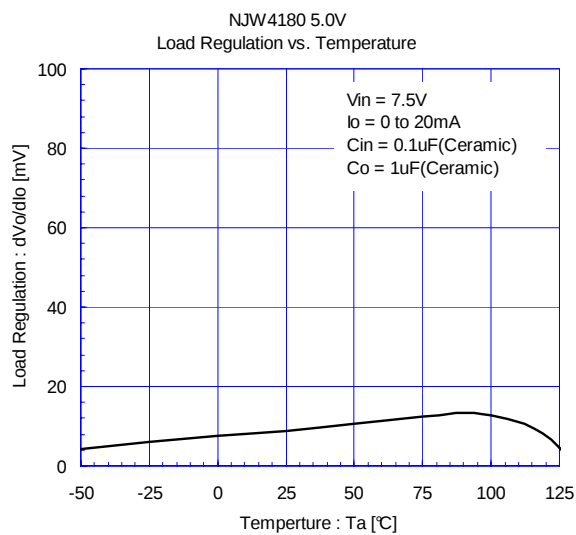
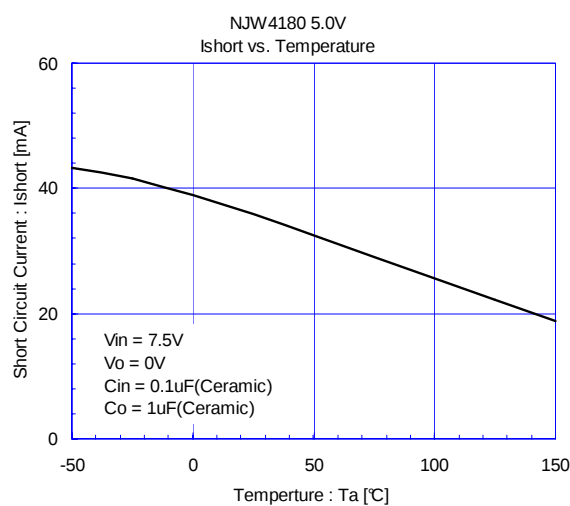
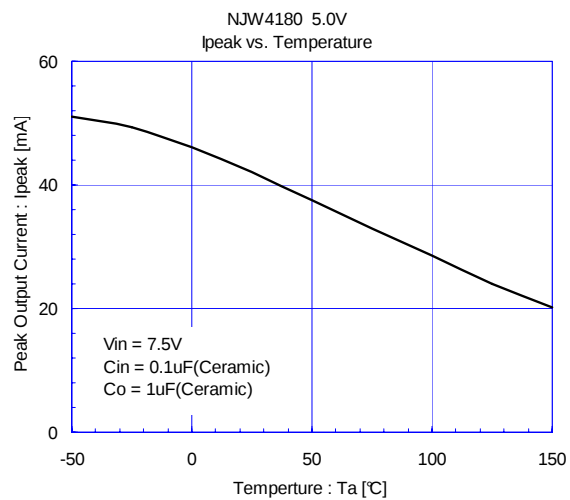
Therefore, use C_O with the recommended capacitance or greater value and connect between V_O terminal and GND terminal with minimal wiring. The recommended capacitance depends on the output voltage. Low voltage regulator requires greater value of the C_O . Thus, check the recommended capacitance for each output voltage.

Use of a greater C_O reduces output noise and ripple output, and also improves transient response of the output voltage against rapid load change.

■ TYPICAL CHARACTERISTICS







[CAUTION]

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