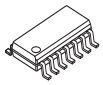
Low power quad operational amplifiers

Features

- Wide gain bandwidth:1.3MHz typ.
- Input common-mode voltage range includes ground
- Large voltage gain:100dB typ.
- Very low supply current per amplifier:300uA typ.
- Low input bias current: 20nA typ.
- Low input offset voltage: 7mV max.
- Low input offset current: 2nA typ.
- Wide power supply range:
  - Single supply: +3V to +30V
  - Dual supplies: ±1.5V to ±15V
- Internal ESD protection
  Human body model (HBM) ±2000V typ.



NJM324CG
(SOP14)

Description

The NJM324C consist of four independent, high gain, internally frequency-compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

1 Pin and schematic diagram

Figure 1. Pin connections (top view)

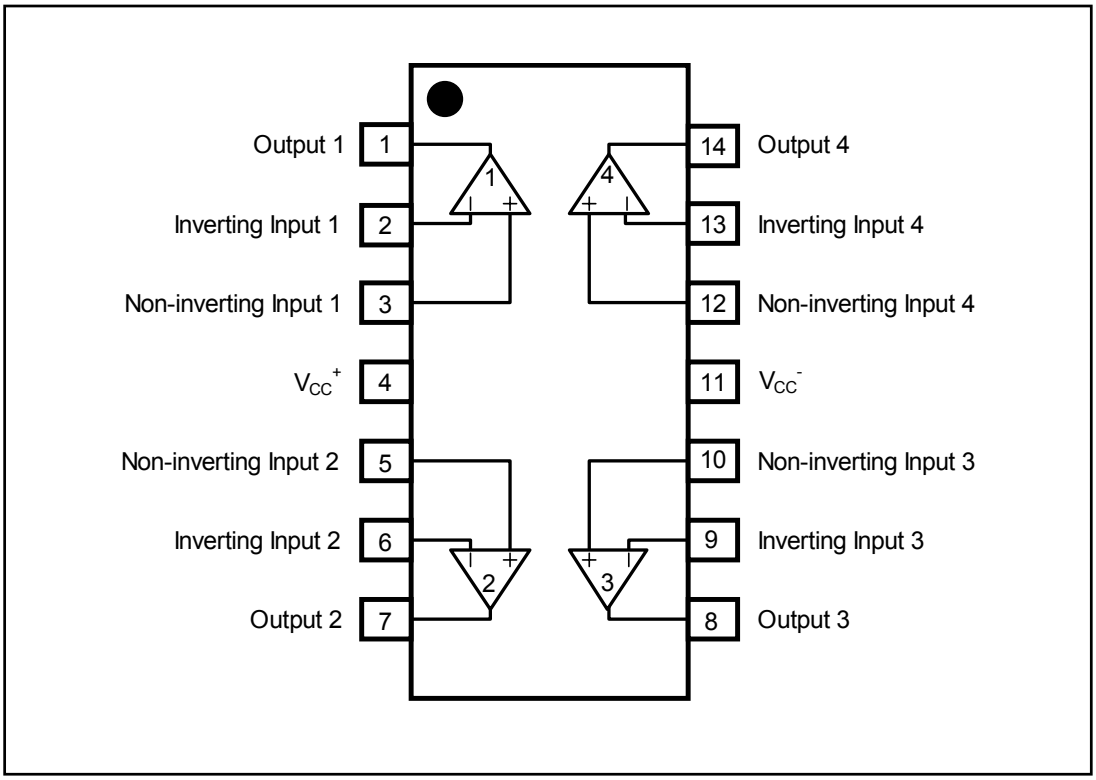
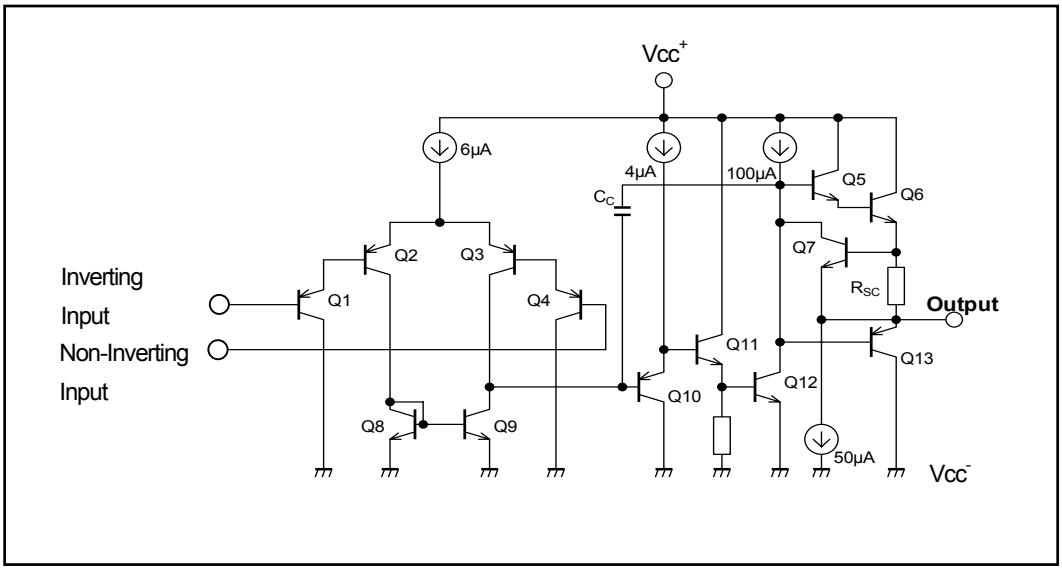


Figure 2. Schematic diagram (1/4 NJM324C)



2 Absolute maximum ratings

Table1. Absolute maximum ratings (Tamb=25°C)

Symbol	Parameter	NJM324C	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	32	V
V_{IN}	Input voltage (1)	-0.3 to 32	V
V_{ID}	Differential input voltage	±32	V
-	Output short-circuit duration (2)	Infinite	-
I_{IN}	Input current (3):Vin driven negative Input current (4):Vin driven positive above AMR value	5mA in DC or 50mA in AC (duty cycle = 10%, T=1s) 0.4	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
P_D	Power Dissipation	880(6) 1200(7)	mW
θja	Thermal resistance junction to ambient(5)	140(6) 100(7)	°C /W
ψjt	Thermal resistance junction to top surface of IC package(5)	40(6) 35(7)	°C /W

1. Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V_{CC}^+
2. Short-circuits from the output to V_{CC}^+ can cause excessive heating if V_{CC} > 15V. Destructive dissipation can result from simultaneous short circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-vase junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
4. The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400uA max (R= (Vin-32V)/400uA).
5. Short-circuit can cause excessive heating and destructive dissipation. Values are typical.
6. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting
7. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting

3. Operating conditions

Table2. Operating conditions (Tamb=25°C)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	3 to 30	V
V_{icm}	Common mode input voltage range	V_{CC}^- - 0.3 to V_{CC}^+ - 1.5	V
T_{oper}	Operating free-air temperature range	-40 to +85	°C

4. Electrical characteristics

Table3. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25°C , T_{min} = 0°C, T_{max}=70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1)				mV
	T_{amb}	-	0.5	7	
	$T_{min} < T_{amb} < T_{max}$ (5)	-	-	9	
I_{io}	Input offset current				nA
	T_{amb}	-	2	30	
	$T_{min} < T_{amb} < T_{max}$ (5)	-	-	100	
I_{ib}	Input bias current (2)				nA
	T_{amb}	-	20	150	
	$T_{min} < T_{amb} < T_{max}$ (5)	-	-	300	
A_{vd}	Large signal voltage gain				V/mV
	T_{amb}, V_{CC}^+ = +15V, RL=2kΩ, Vo=1.4V to 11.4V,	50	100	-	
	$T_{min} < T_{amb} < T_{max}$ (5)	25	-	-	
SVR	Supply voltage rejection ratio (Rs<10kΩ)				dB
	T_{amb}, V_{CC}^+ = 5V to 30V	65	110	-	
	$T_{min} < T_{amb} < T_{max}$ (5)	65	-	-	
I_{CC}	Supply current, all amp, no load				mA
	T_{amb}, V_{CC}^+ = 5V	-	1.2	2	
	T_{amb}, V_{CC}^+ = 30V	-	1.7	3	
	$T_{min} < T_{amb} < T_{max}$ (5)				mA
	V_{CC}^+ = 5V	-	-	2	
	V_{CC}^+ = 30V	-	-	3	
V_{icm}	Input common mode voltage range				V
	T_{amb}, V_{CC}^+ = +30V (3)	0	-	V_{CC}^+ - 1.5	
	$T_{min} < T_{amb} < T_{max}$ (5)	0	-	V_{CC}^+ - 2	
CMR	Common mode rejection ratio (R_S < 10kΩ)				dB
	T_{amb}	70	100	-	
	$T_{min} < T_{amb} < T_{max}$ (5)	60	-	-	
I_{source}	Output current source (V_{id} = +1V)				mA
	T_{amb}, V_{CC}^+ = 15V, V_O = +2V,	20	40	-	

Table4. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25˚C , T_{min} = 0˚C,T_{max}=70˚C (unless otherwise specified)

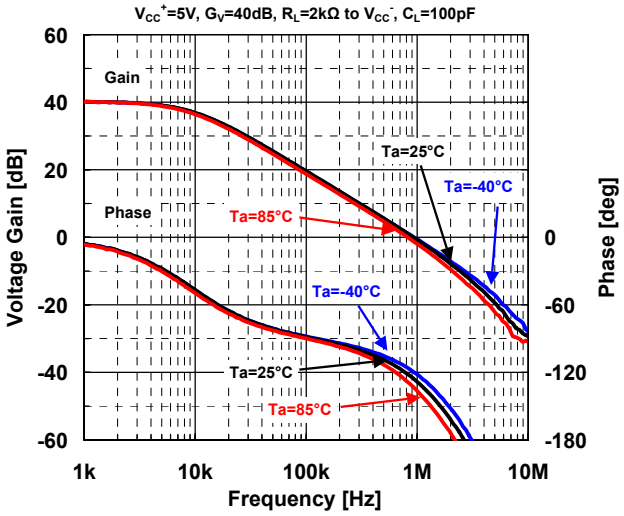
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{sink}	Output sink current (V_{id} = -1V)				
	T_{amb},V_{CC}^+ = 15V, V_o = +2V	10	20	-	mA
	T_{amb},V_{CC}^+ = 15V, V_o = +0.2V	12	50	-	uA
V_{OH}	High level output voltage				V
	T_{amb},V_{CC}^+ = 30V, RL = 2kΩ	26	27	-	
	T_{min} < T_{amb} < T_{max} (5)	26	-	-	
	T_{amb},V_{CC}^+ = 30V,RL = 10kΩ	27	28	-	
	T_{min} < T_{amb} < T_{max} (5)	27	-	-	
	T_{amb},V_{CC}^+ = 5V, RL = 2kΩ	3.5	-	-	
	T_{min} < T_{amb} < T_{max} (5)	3	-	-	
V_{OL}	Low level output voltage				mV
	T_{amb},RL = 10kΩ	-	5	20	
	T_{min} < T_{amb} < T_{max} (5)	-	-	20	
SR	Slew rate T_{amb},V_{CC}^+ = 15V, V_i=0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain	-	0.6	-	V/μs
GBP	Gain bandwidth product T_{amb},V_{CC}^+ = 30V, f = 100kHz, V_{in}=10mV, R_L = 2kΩ, C_L = 100pF	-	1.3	-	MHz
THD	Total harmonic distortion T_{amb},f = 1kHz, A_V=20dB, R_L = 2kΩ, V_O = $2V_{pp}$, C_L = 100pF, V_{CC}^+ = 30V	-	0.015	-	%
e_n	Equivalent input noise voltage T_{amb},f = 1kHz, R_S=100Ω, V_{CC}^+ = 30V	-	30	-	nV/√Hz
DV_{io}	Input offset voltage drift T_{min} < T_{amb} < T_{max} (5)	-	7	30	μV/°C
DI_{io}	Input offset current drift T_{min} < T_{amb} < T_{max} (5)	-	10	200	pA/°C
V_{O1}/V_{O2}	Channel separation (4) T_{amb},1kHz < f < 20kHz	-	120	-	dB

1. V_O = 1.4V, R_S=0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V.
2. The direction of the input current is out of the IC.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of the external components, ensure that stray capacitance between these external parts dose not cause coupling. Coupling can be detected because this type of capacitance increases at higher frequencies.
5. This parameter is not 100% test.

■ TYPICAL CHARACTERISTICS

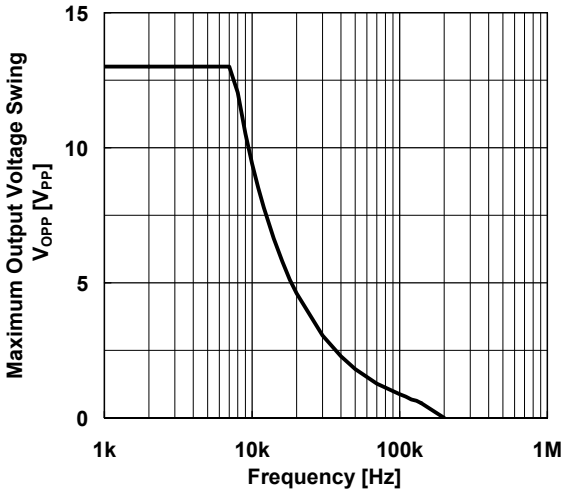
Gain/Phase vs. Frequency

V_{CC}^+=5V, G_V=40dB, R_L=2kΩ to V_{CC}^-, C_L=100pF



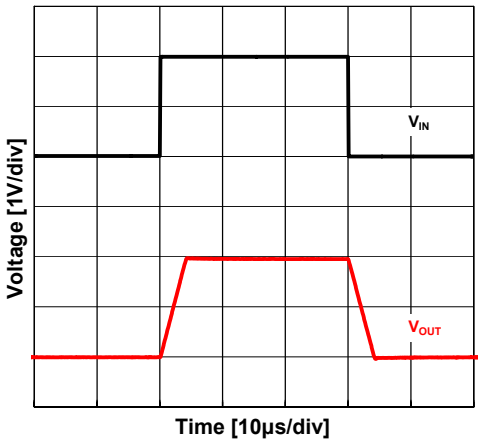
Maximum Output Voltage Swing vs. Frequency

V_{CC}^+=15V, Ta=25°C



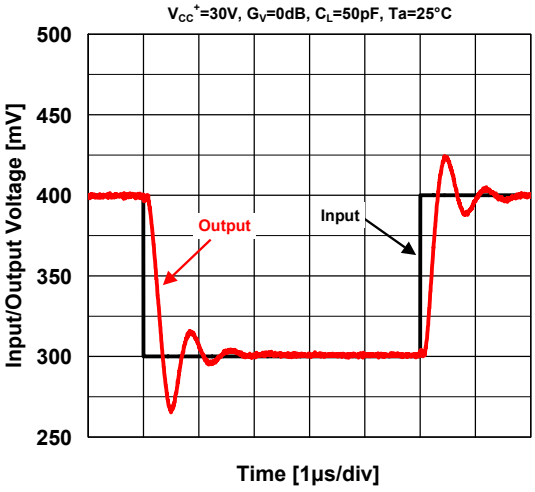
Pulse Response

V_{CC}^+=15V, R_L=2kΩ, C_L=100pF, Ta=25°C



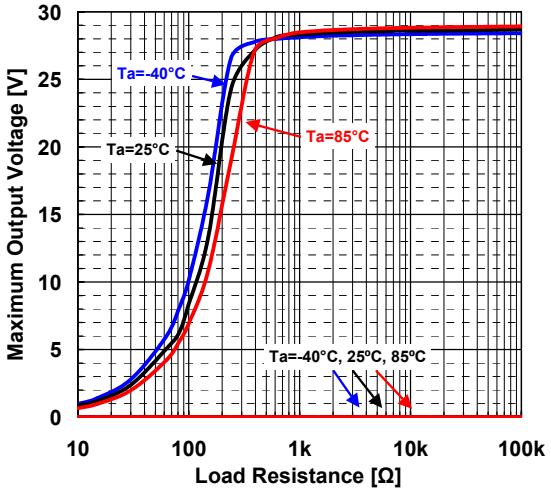
Small signal Pulse Response

V_{CC}^+=30V, G_V=0dB, C_L=50pF, Ta=25°C



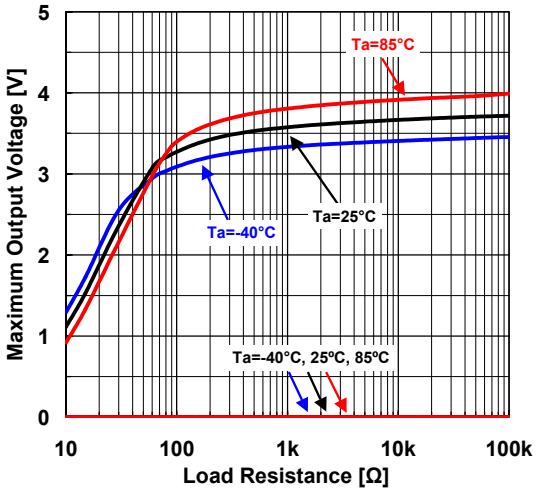
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=30V, R_L to V_{CC}^-



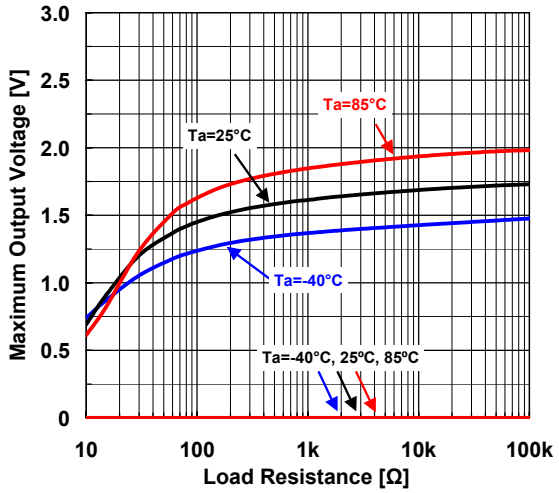
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=5V, R_L to V_{CC}^-

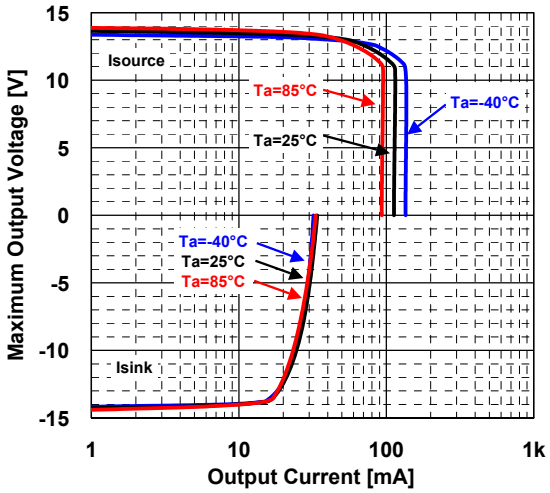


■ TYPICAL CHARACTERISTICS

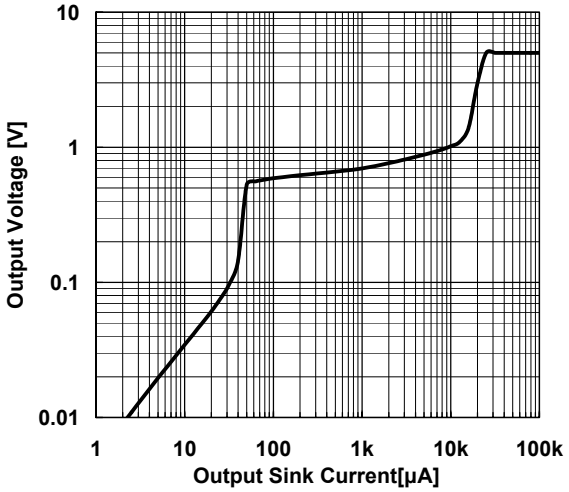
Maximum Output Voltage vs. Load Resistance



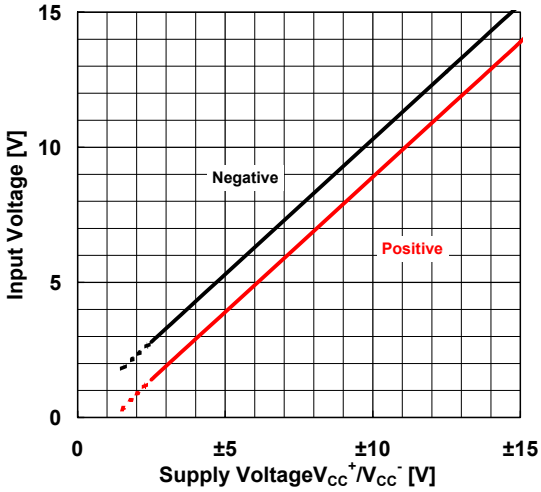
Maximum Output Voltage vs. Output Current



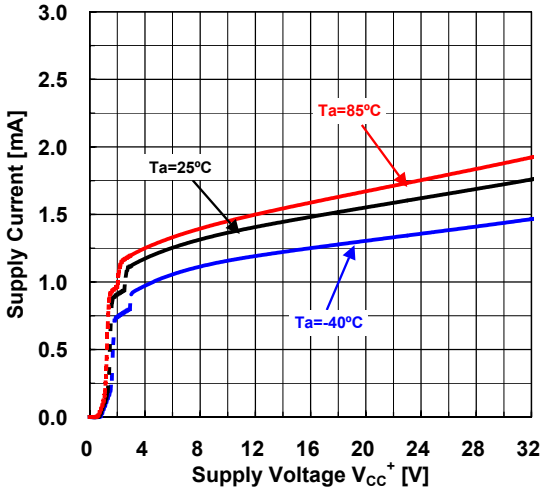
Output Voltage vs. Output Sink Current



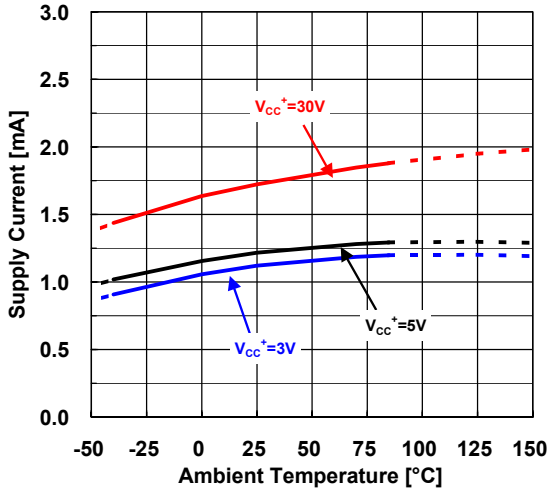
Input Voltage Range vs. Supply Voltage



Supply Current vs. Supply Voltage

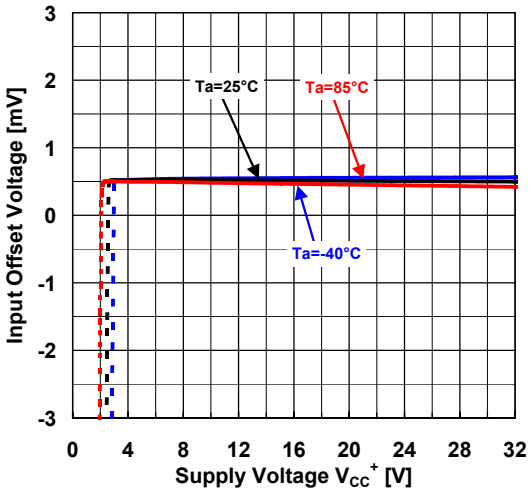


Supply Current vs. Temperature

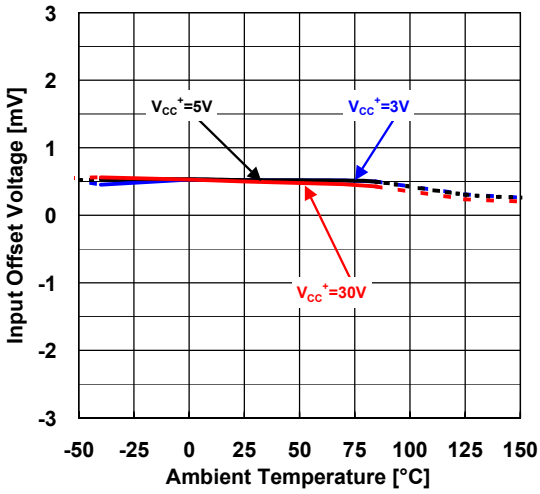


■ TYPICAL CHARACTERISTICS

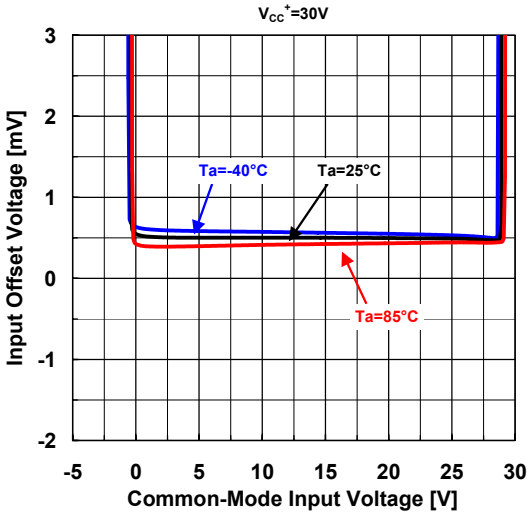
Input Offset Voltage vs. Supply Voltage



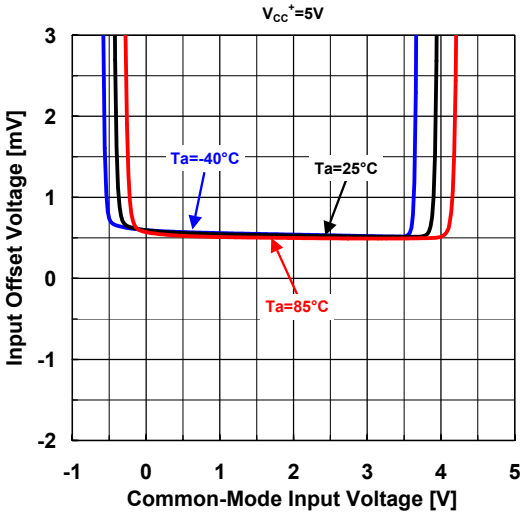
Input Offset Voltage vs. Temperature



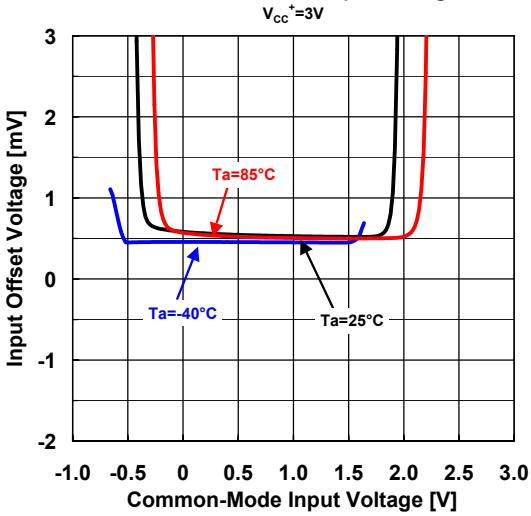
Input Offset Voltage vs. Common-Mode Input Voltage



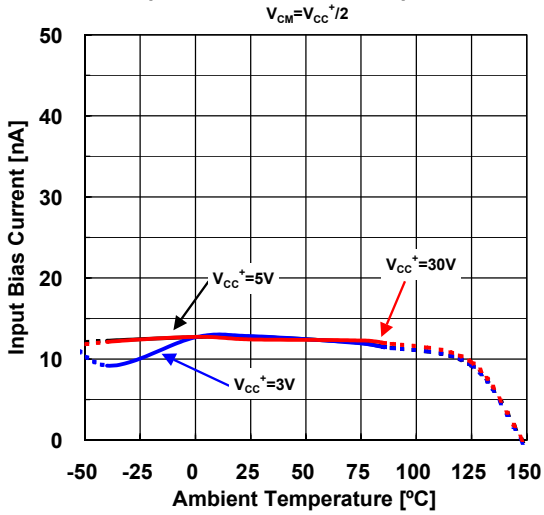
Input Offset Voltage vs. Common-Mode Input Voltage



Input Offset Voltage vs. Common-Mode Input Voltage



Input Bias Current vs. Temperature



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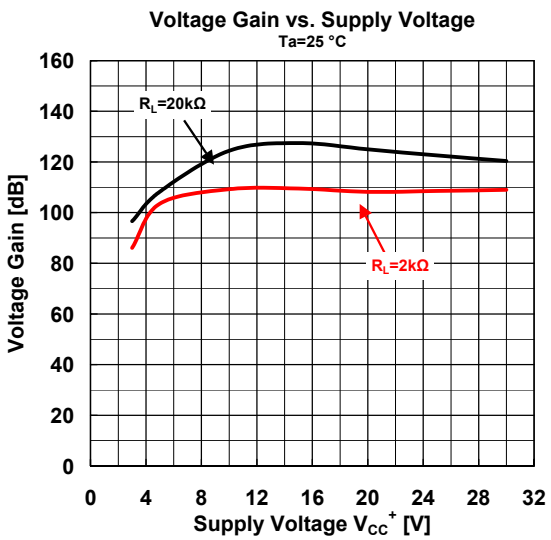
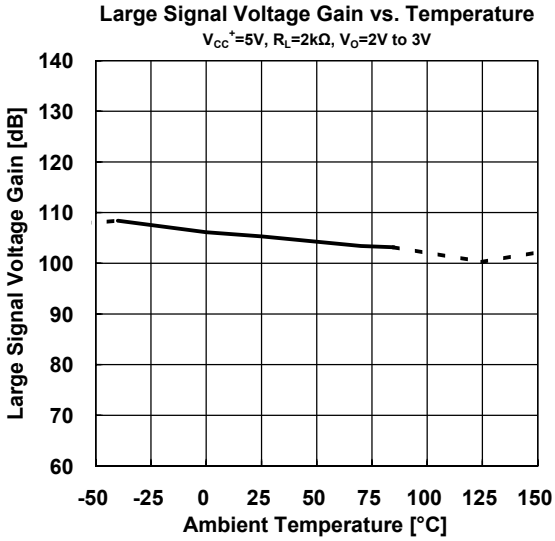
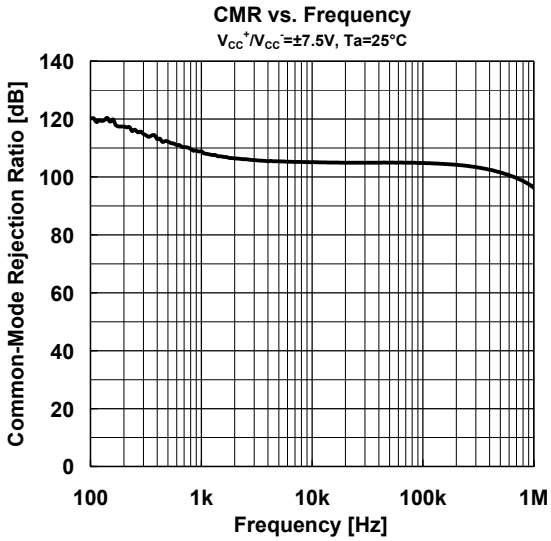
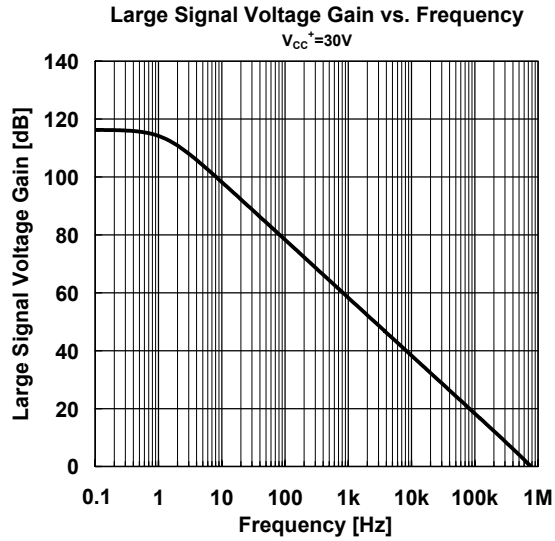
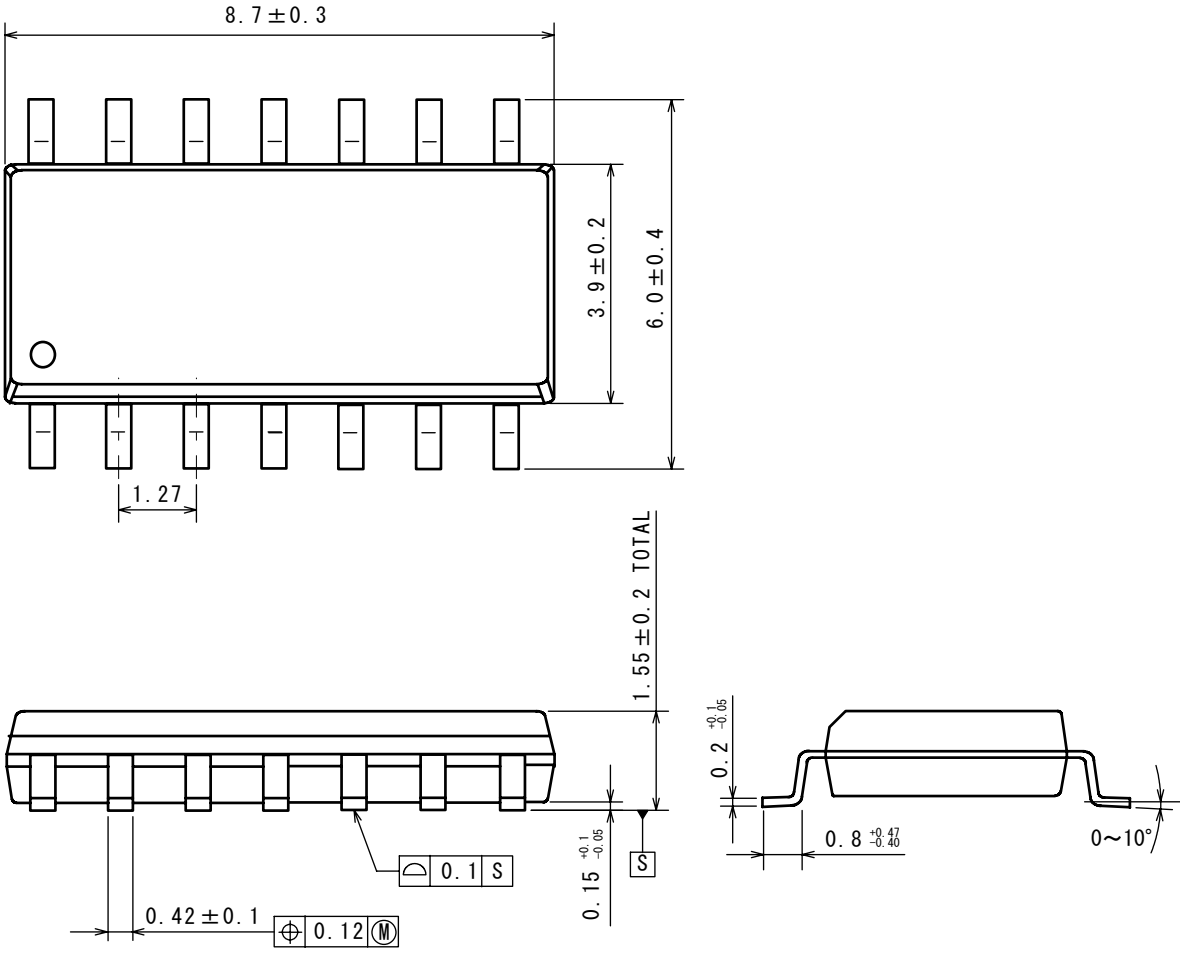








■PACKAGE OUTLINE UNIT : mm



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