

Features

- Low On-Resistance
- On-Resistance Matching Between Channels, 0.2Ω typ
- On-Resistance Flatness, <math><2\Omega</math> typ
- Low Off-Channel Leakage, <math><100\text{pA}</math> @ +25°C
- TTL/CMOS Logic Compatible
- GND-to-V+ Analog Signal Dynamic Range
- Low Power Consumption (<math><12\mu\text{W}</math>)
- Low Crosstalk: -86dB @ 1MHz
- Low Off-Isolation: -58dB @ 1 MHz
- Wide Bandwidth: > 100 MHz
- Small QSOP-16 Package Saves Board Area

Applications

- Instrumentation, ATE
- Sample-and-Holds
- Audio Switching and Routing
- Telecommunication Systems
- PBX, PABX
- Battery-Powered Systems

Description

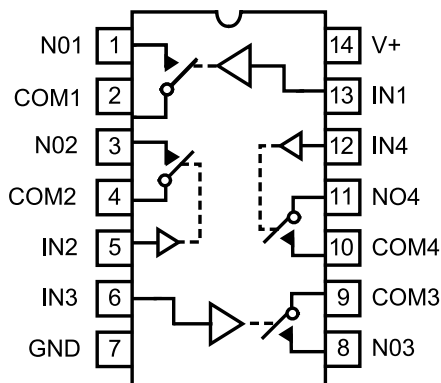
The PS4066/PS4066A are improved SPST CMOS analog switches ideal for low-distortion audio switching. These high precision, medium voltage switches were designed to operate with single-supplies from +3V to 16V. They are fully specified with +12V, +5V, and +3V supplies. The PS4066/PS4066A has four normally open (NO) switches. Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

With +12V power supply, the PS4066/PS4066A guarantee <math><45\Omega</math> on-resistance. On-resistance matching between channels is within 2Ω (PS4066). On-resistance flatness is less than 4Ω (PS4066A) over the specified range. The PS4066A guarantees low leakage currents (<math><100\text{pA}</math> @ 25°C, <math><6\text{nA}</math> @ +85°C) and fast switching speeds ($t_{\text{ON}} < 175\text{ns}</math>). ESD sensitivity rating is >2,000V per MIL-STD 883, Method 3015.7$

Both devices are available in PDIP-14, narrow-body SOIC-14, and QSOP-16 packages. Available temperature ranges are: commercial (0°C to 70°C), and industrial (-40°C to +85°C).

For operation below 5V, the PI5A101/PI5A391/PI5A392 are also recommended.

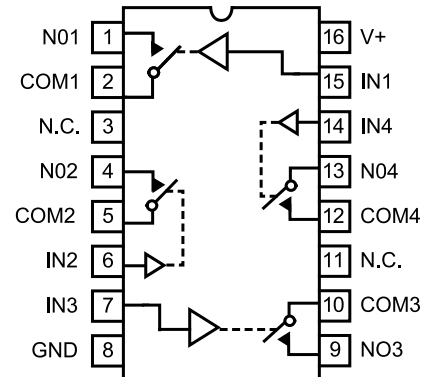
Functional Diagrams, Pin Configurations, and Truth Table



Top View
PDIP/SO

Logic	Switch
0	OFF
1	ON

N.C. = No Internal Connection
Switches shown for logic "0" input



Top View
QSOP

Absolute Maximum Ratings

Voltages Referenced to GND

V+ -0.3V to +17V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) -2V to (V+) +2V
or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA

ESD per Method 3015.7 >2000V

Thermal Information

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 10.5mW/°C above +70°C) 800mW

SO and QSOP (derate 8.7mW/°C above +70°C) 650mW

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note

Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +12V Supply

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}		Full	0		V+	V
On Resistance	R _{ON}	V+ = 12V, I _{COM} = 2mA, V _{NO} = 10V	25		12	45	Ω
			Full			55	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V+ = 12V, I _{COM} = 2mA V _{NO} = 10V	25		0.5 0.5	4 2	Ω
			Full			6	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}	V+ = 12V, I _{COM} = 2mA, V _{NO} = 10V, 5V, 1V	25		2	4	Ω
			Full			6	
NO or NC Off Leakage Current ⁽⁶⁾	I _{NO(OFF)} OR I _{NC(OFF)}	V+ = 12V, V _{COM} = 0V, V _{NO} = 10V	25		-1 -0.1	1 0.1	nA
			Full		-6	6	
COM Off Leakage Current ⁽⁶⁾	I _{COM(OFF)}	V+ = 12V, V _{COM} = 0V, V _{NO} = 10V	25		-1 -0.1	1 0.1	nA
			Full		-6	6	
COM On Leakage Current ⁽⁶⁾	I _{COM(ON)}	V+ = 12V, V _{COM} = 10V, V _{NO} = 10V	25		-2 -0.2	2 0.2	nA
			Full		-12	12	

Electrical Specifications - Single +12V Supply (continued)
($V_+ = 12V \pm 10\%$, $GND = 0V$, $V_{INH} = 4V$, $V_{INL} = 0.8V$)

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units	
Logic Input								
Input Current with Input Voltage High	I_{INH}	$I_N = 5V$, all others = 0.8V	Full	-0.5	0.005	0.5	μA	
Input Current with Input Voltage Low	I_{INL}	$I_N = 0.8V$, all others = 5V		-0.5	0.005	0.5		
Dynamic								
Turn-On Time	t_{ON}	$V_{COM} = 10V$, Figure 2	25		45	100	ns	
			Full			150		
Turn-Off Time	t_{OFF}		25		17	75		
			Full			100		
On-Channel Bandwidth	BW	Signal = 0dbm Figure 4, 50 Ω in and out	25		100		MHz	
Charge Injection ⁽³⁾	Q	$C_L = 1nF$, $V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, Figure 3			2	10	pC	
Off Isolation	OIRR	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1$ MHz, Figure 4			-58		dB	
Crosstalk ⁽⁸⁾	X_{TALK}	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1$ MHz, Figure 5			-86			
NO Capacitance	$C_{(OFF)}$	$f = 1$ MHz, Figure 6			9		pF	
COM Off Capacitance		$f = 1$ MHz, Figure 6			9			
COM On Capacitance	$C_{COM(ON)}$	$f = 1$ MHz, Figure 7			22			
Supply								
Positive Supply Current	I_+	$V_{IN} = 0V$ or V_+ , all channels on or off		Full	-1	0.001	1	μA
Total Harmonic Distortion	THD				0.03		%	

Notes:

- The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- Guaranteed by design
- $\Delta R_{ON} = \Delta R_{ON} \text{ max} - \Delta R_{ON} \text{ min}$
- Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
- Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
- Off Isolation = $20 \log_{10} [V_{COM} / (V_{NO} \text{ or } V_{NO})]$, V_{COM} = Output, V_{NC} / V_{NO} = input to off switch
- Between any two switches.

Electrical Specifications - Single +5V Supply

(V+ = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}		Full	0		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, I _{COM} = -1mA, V _{NO} = 3.5V	25		22	75	Ω
			Full			100	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V+ = 5V, I _{COM} = -1mA, V _{NO} = 3V	25		0.3	4	
			Full			12	
On-Resistance Flatness ^(3,5)	R _{FLAT(ON)}	V+ = 5V, I _{COM} = -1mA, V _{NO} = 1V, 3V	25		4	6	
			Full			8	
NO Off Leakage Current ⁽⁹⁾	I _{NO(OFF)}	V+ = 5.5V, V _{COM} = 0V, V _{NO} = 4.5V	25		-1 -0.1	1 0.1	nA
			Full			6	
COM Off Leakage Current ⁽⁹⁾	I _{COM(OFF)}	V+ = 5.5V, V _{COM} = 0V, V _{NO} = 4.5V	25		-1 -0.1	1 0.1	
			Full			6	
COM On Leakage Current ⁽⁶⁾	I _{COM(ON)}	V+ = 5.5V, V _{COM} = 5V V _{NO} = 4.5V	25		-2 -0.2	2 0.2	
			Full			12	
Dynamic							
Turn-On Time	t _{ON}	V _{NO} = 3V	25		65	125	ns
			Full			175	
Turn-Off Time	t _{OFF}		25		30	75	
			Full			125	
On-Channel Bandwidth	BW	Signal = 0dBm, 50Ω in and out Figure 4	25		100		MHz
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 3	25		1	10	pC
Supply							
Positive Supply Current	I+	V+ = 5.5V, V _{IN} = 0V or V+, all channels on or off	Full		-1	1	μA

Electrical Specifications - Single +3V Supply

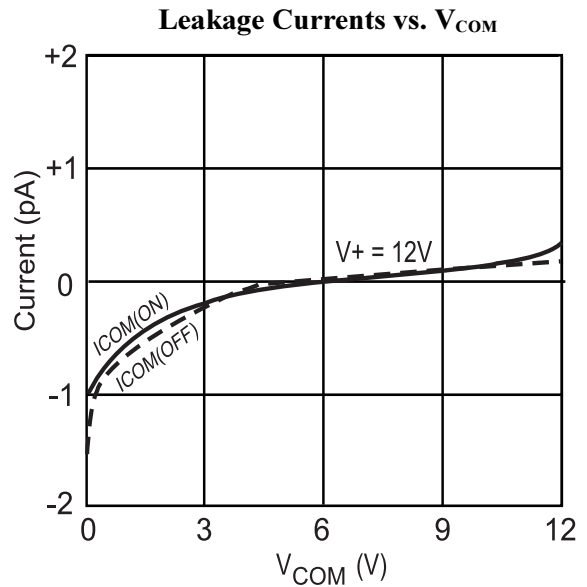
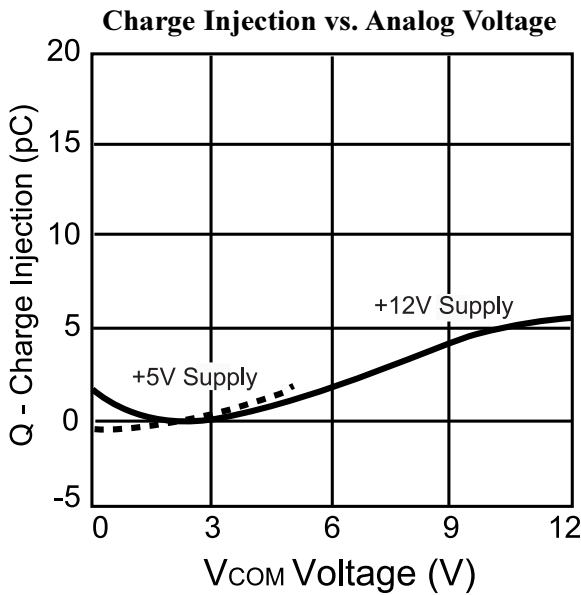
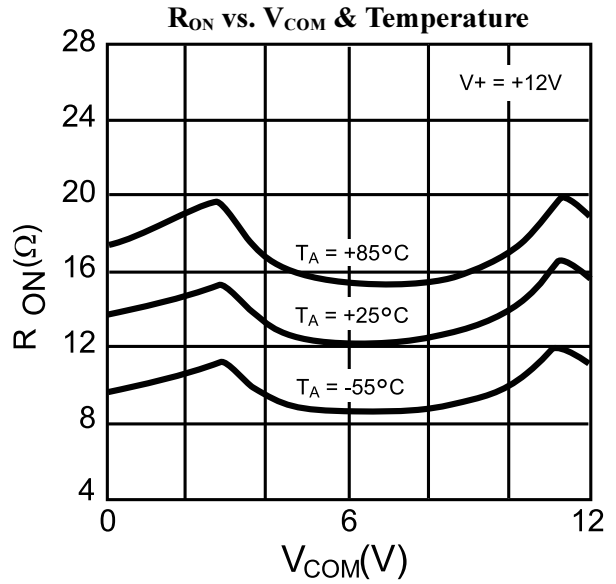
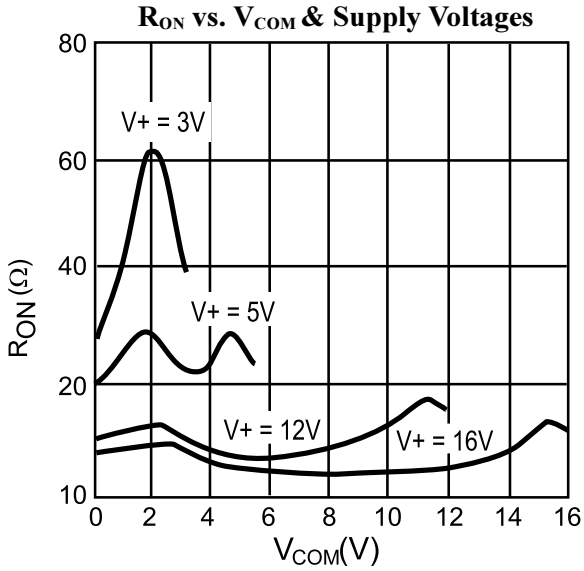
(V+ = +2.7V to 3.3V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp°C	Min. ⁽¹⁾	Typ ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V+	V
Channel On-Resistance	R _{ON}	V+ = 3V, I _{COM} = -1mA, V _{NO} = 1.5V	25			170	Ω
			Full			225	
Dynamic							
Turn-On-Time ⁽³⁾	t _{ON}	V+ = 3V, V _{NO} = 1.5V	25		80	185	ns
			Full			230	
Turn-Off-Time ⁽³⁾	t _{OFF}	V+ = 3V, V _{NO} = 1.5V	25		40	150	
			Full			200	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0V	25		2	10	pC
Supply							
Positive Supply Current	I+	V+ = 3.3V, V _{IN} = 0V or V+, all channels on or off	Full	-1	0.001	1	μA

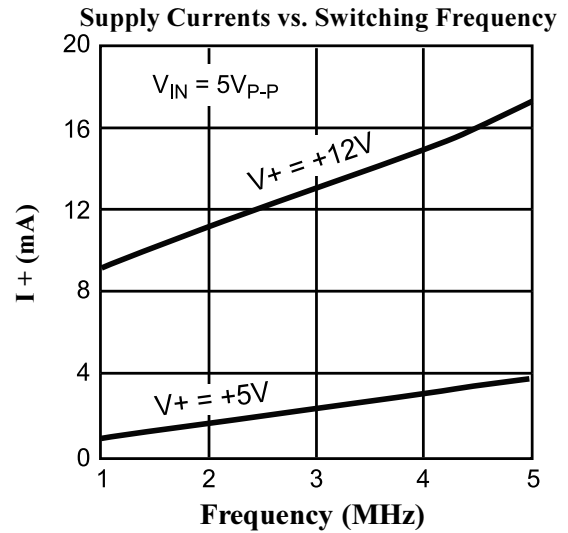
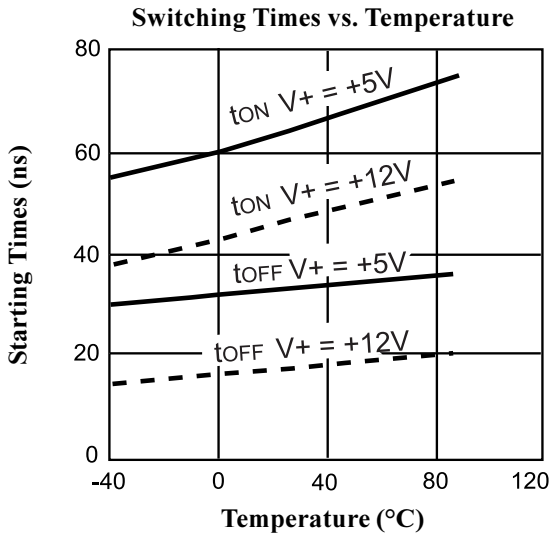
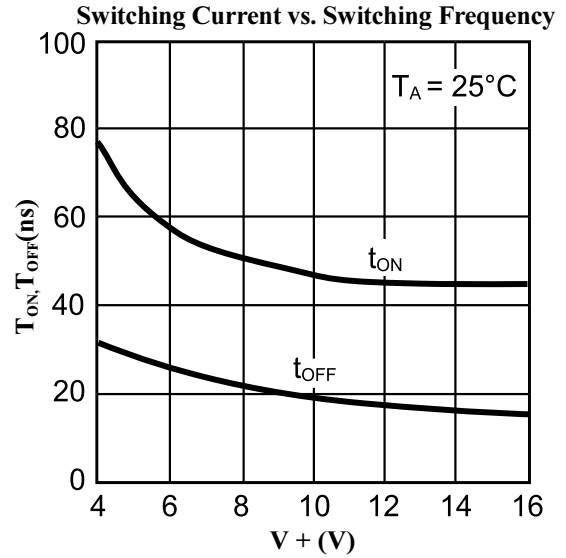
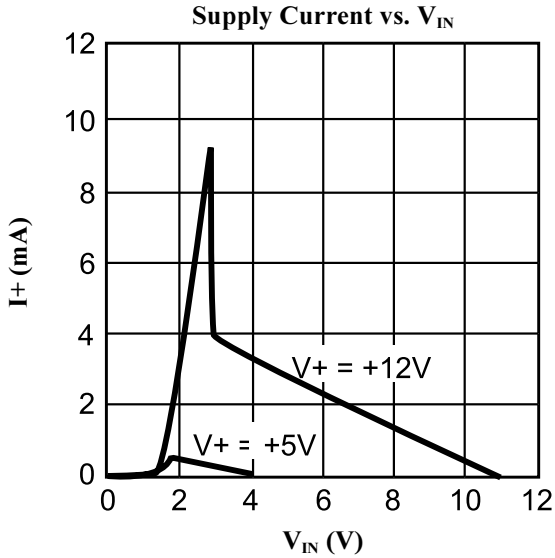
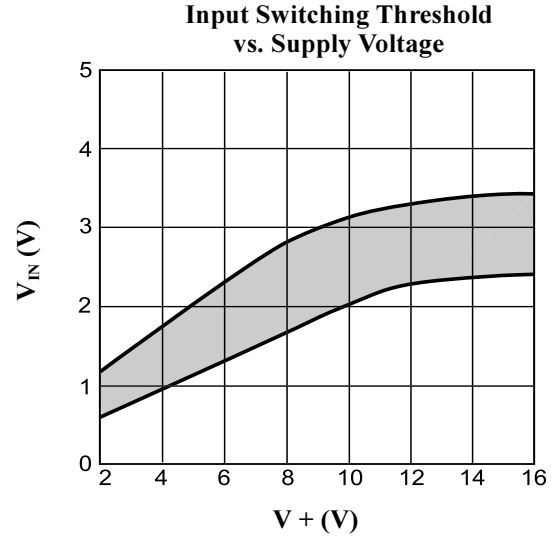
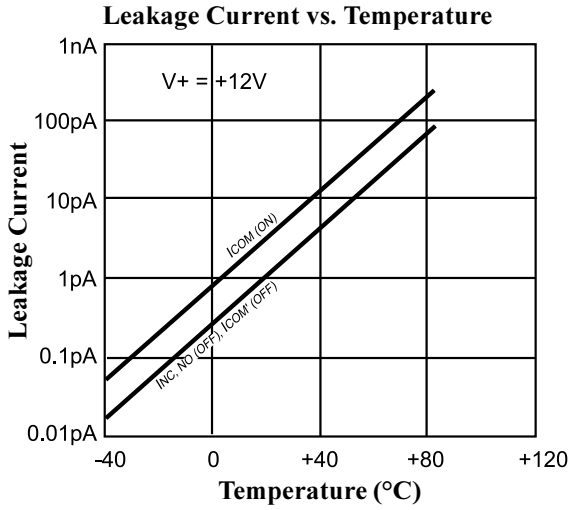
Notes:

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3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON \text{ max}} - \Delta R_{ON \text{ min}}$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Off Isolation = $20 \log_{10} [V_{COM} / (V_{NO} \text{ or } V_{NO})]$, V_{COM} = Output, V_{NC} / V_{NO} = input to off switch
8. Between any two switches.

Typical Operating Characteristics (TA = +25°C, unless otherwise noted)



Typical Operating Characteristics (TA = +25°C, unless otherwise noted)



Pin Description

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, and then the logic inputs. If power-supply sequencing is not possible, add a small signal diode or current limiting resistor in series with the supply pin for overvoltage protection (Figure 1). Adding a diode reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

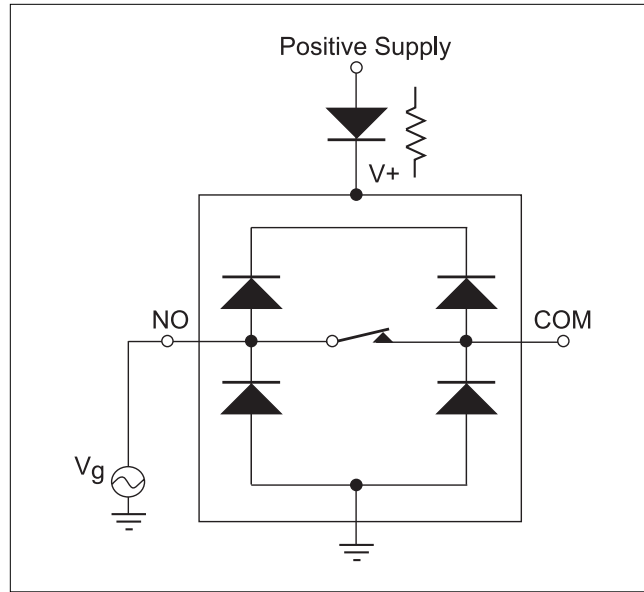


Figure 1. Overvoltage protection is accomplished using an external blocking diode or a current limiting resistor .

Test Circuits/Timing Diagrams

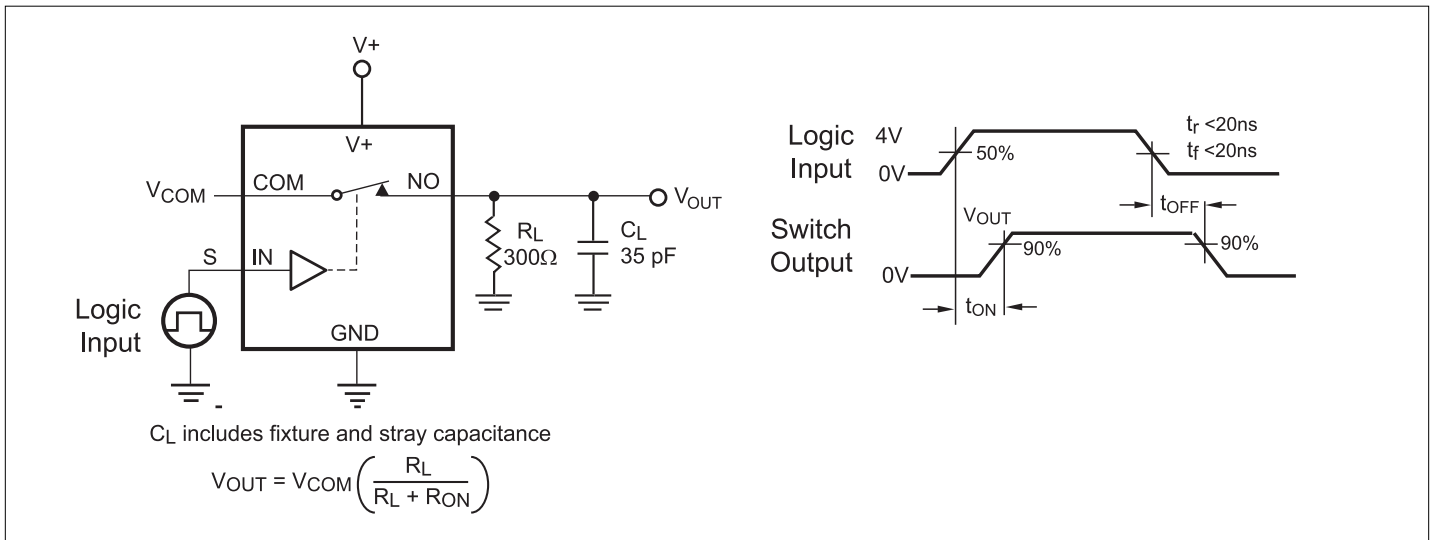


Figure 2. Switching Times

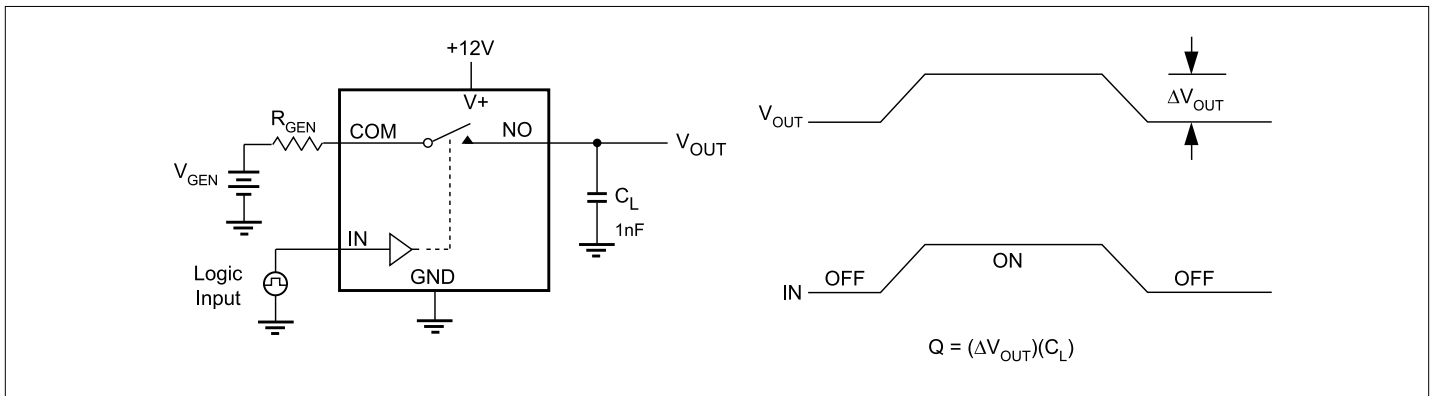


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

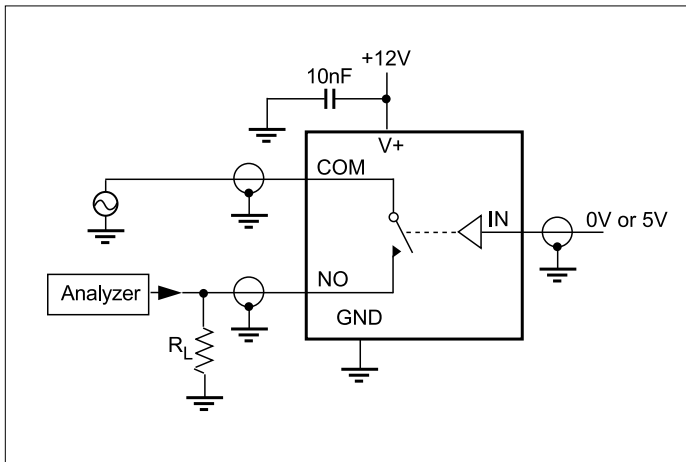


Figure 4. Off Isolation, BW

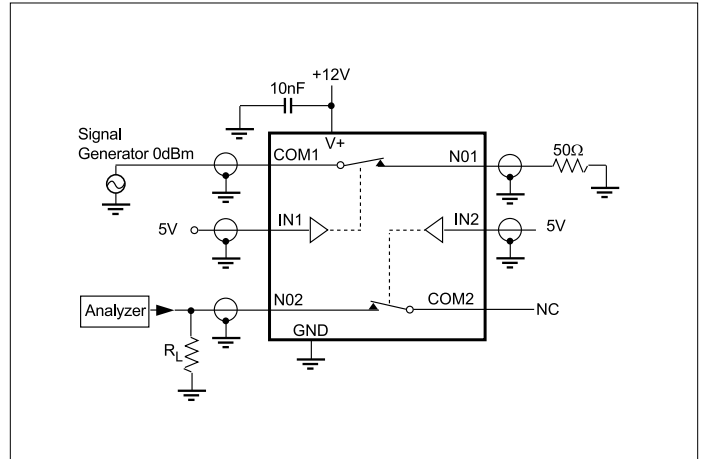


Figure 5. Crosstalk

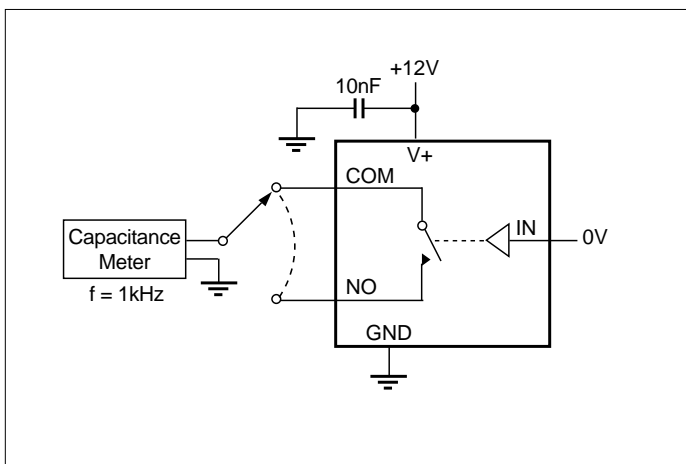


Figure 6. Channel-Off Capacitance

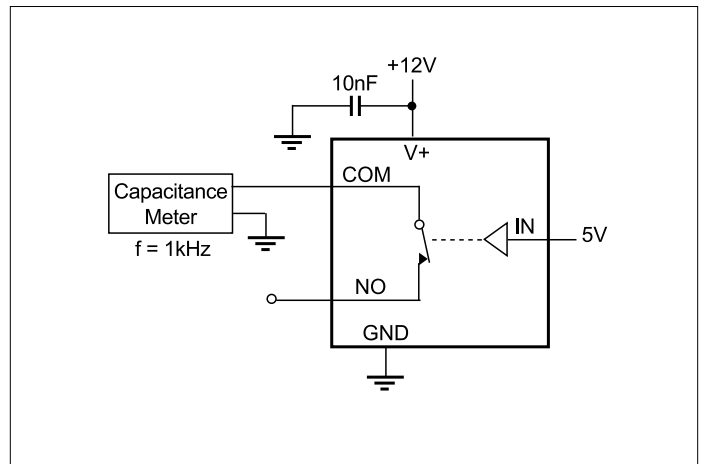


Figure 7. Channel-On Capacitance

Ordering Information

Part Number	Temperature - Range	Package
PS4066CPD	0°C to + 70°C	14 Plastic DIP
PS4066CSD	0°C to + 70°C	14 Narrow SO
PS4066CEE	0°C to + 70°C	16 QSOP
PS4066EPD	-40°C to + 85°C	14 Plastic DIP
PS4066ESD	-40°C to + 85°C	14 Narrow SO
PS4066ACPD	0°C to + 70°C	14 Plastic DIP
PS4066ACSD	0°C to + 70°C	14 Narrow SO
PS4066ACEE	0°C to + 70°C	16 QSOP
PS4066AEPD	-40°C to + 85°C	14 Plastic DIP
PS4066AESD	-40°C to + 85°C	14 Narrow SO
PS4066AEED	-40°C to + 85°C	16 QSOP