PI5USB2543

USB Power Switch with Pericom's FAST Charger Circuitry for DCP, CDP, and 2A iPad support

Features

- USB charger controller that supports SDP, DCP and CDP per USB BC 1.0, 1.1, and 1.2 specfication
  - DCP (Dedicated charger port) is used when enumeration is not available
  - CDP (Charging downstream port) is used when enumeration is available and FAST charging is requested
  - SDP (Standard downstream port) is used for systems with standard USB host ports
- Support for YD/T-1591(Chinese Telecom Standard)
- Support for non-standard charging such as Apple-1A and Apple-2A
- Integrated 85mΩ MOSFET with thermal and Short-circuit protection
- Adjustable Current Limit from 1.1A to 2.8A
- Single Power Supply, 5V +/-5%
- Fast response time for over-current detection, 4us (typ)
- De-glitched Fault Report ($\overline{\text{FAULT}}$)
- Integrated ESD protection up to +/- 4kV contact on pins 10 and 11 per IEC61000-4-2 spec
- Reverse Current Blocking and over-voltage on Vbus path
- Detects when device is plugged in or out when in "DCP/ AutoDetect" mode and provides output signal (PE/)
- Mouse/Keyboard wake-up support (see truth table)
- UL certified, E352621 (2012-02-17)

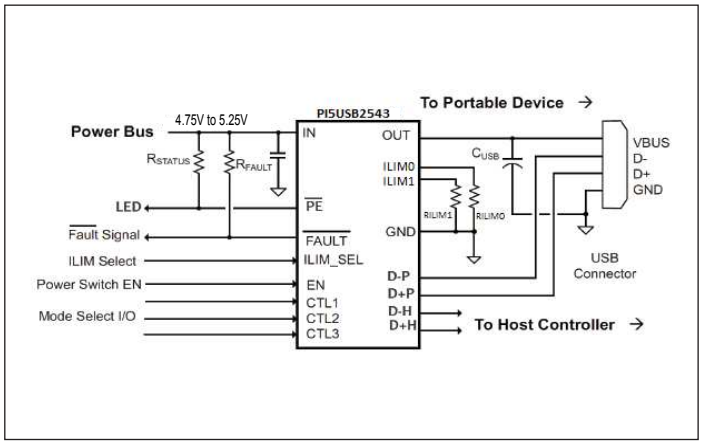
Description

Type A USB connectors are found in 100% of PCs as well as in wall chargers that are shipped with all of the latest popular hand-held devices that require charging. All of the connectors physically look the same, however, their behavior is different. When a user tries to connect an iPAD into a notebook USB port vs. a USB charger that came with the iPAD, one can instantly observe a different behavior. This is because the communication protocol of a standard PC USB port vs. a dedicated Apple-iPAD USB port is different and it is this communication that enables the iPAD to charge efficiently. The same can be seen by other popular phones and tablets.

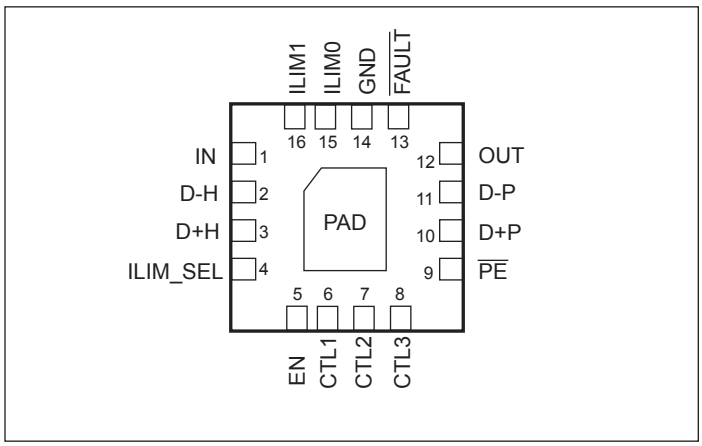
There are Apple-1A modes of communication, Apple-2A modes of communication, communication described by the Chinese Telecom standard, YD/T-1591, and communication described by the USB Battery Charging Spec. In order to support all popular phones, all communication protocols must be supported.

Pericom's PI5USB2543 is able to offer anybody designing a USB port meant to charge external devices with all communication protocols in a single IC. The PI5USB2543 can detect the communication language required and then automatically enable charging to occur with different external USB devices.

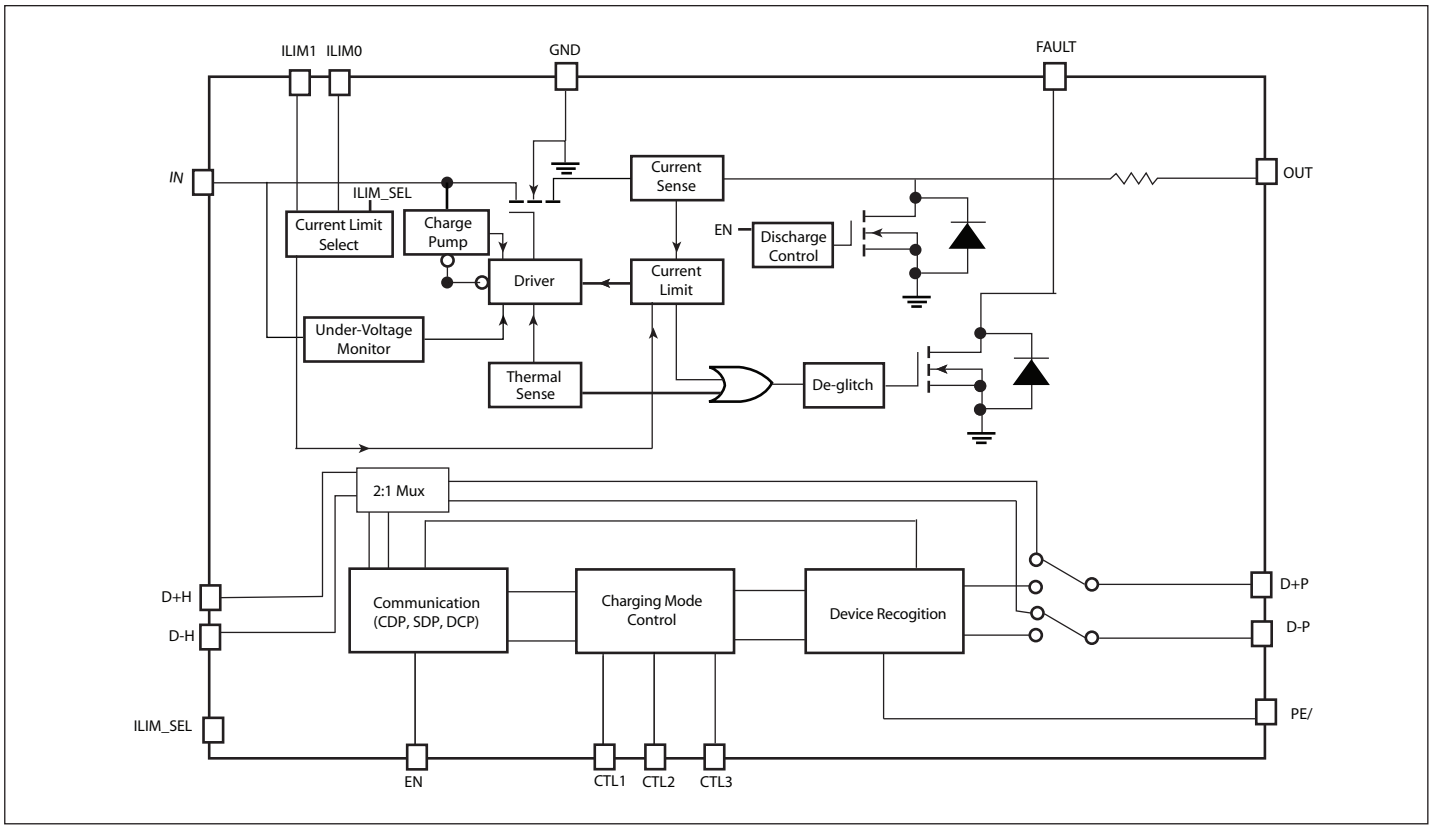
Reference Diagram



Pin Diagram: (Top View)



Block Diagram



Pin Description

Pin No.	Pin Name	I/O Type	Description
1	IN	Power Input	5V Input Voltage: connect a 0.1µF or greater ceramic capacitor from IN to GND as close to the IC as possible
2	D-H	I/O	D-data line to USB host controller
3	D+H	I/O	D+data line to USB host controller
4	ILIM_SEL	I	Control input signal used to dynamically change power switch current-limit threshold: Logic Low selects ILIM0, logic High selects ILIM1 this pin has an internal pull-down
5	EN	I	Control input for turning entire IC on/off (including the Power switch), Logic High configures charger controller into normal operation, Logic Low turns the IC off, which will put the USB signal path into High-Z and the power switch will shut off the OUT pin and the OUT cap will be discharged by the Pericom IC.
6	CTL1	I	Control input for controlling charging mode, See truth table
7	CTL2	I	Control input for controlling charging mode, See truth table
8	CTL3	I	Control input for controlling charging mode, See truth table
9	PE/	O	Open drain output telling system when device is connected
10	D+P	I/O	D+ data line to external USB Port

Pin Description (Cont..)

Pin No.	Pin Name	I/O Type	Description
11	D-P	I/O	D- data line to external USB Port
12	OUT	Power Output	Power-Switch Output
13	$\overline{\text{FAULT}}$	O	Active-low open drain output, asserted during over temperature, low VOUT or reverse voltage conditions
14	GND	Ground	Ground connection : should be connected externally to POWERPAD
15	ILIM0	I	External Resistor used to set current limit threshold when ILIM_SEL logic Low 16K≤ RILIM ≤ 50K
16	ILIM1	I	External Resistor used to set current limit threshold when ILIM_SEL logic High; 16K≤ RILIM ≤ 50K
NA	Center Pad	Ground	Internally connected to GND: Used to heat-sink the part to the circuit board-traces. Should be connected to GND pin

System State	CTL1	CTL2	CTL3	Mode
S4/S5	0	0	0	IC power down with all I/O's High-z
S4/S5	0	0	1	DCP/Auto detect w/ USB/Keyboard pass through disabled
S3	0	1	0	D+/- pass through mode (D+/-P connects to D+/-H)
S3	0	1	1	DCP/Auto detect w/ USB/Keyboard pass through enabled
Test mode	1	0	0	DCP, BC Specification 1.1 only
Test Mode	1	0	1	DCP, Apple 1A only
S0	1	1	0	SDP enabled
S0	1	1	1	CDP or SDP (if device does not support CDP) enabled

7.1 Plug in Detection

During PowerNAP mode (charing when system is in S3/S4/S5), Pericom can detect when an external device is connected or not. This feature can help save system power when nothing is connected externally. Using Pericom's PE/ open drain output flag, the system could disable higher current supplies when no external device is connected. Once an external device is connected, Pericom's PE/ output flag can inform the system and then in-turn, the system could enable the higher current power supply to enable charging.

Next, the Pericom device will detect what type of device is plugged in (BC1.0 device vs. BC1.1 vs. BC1.2 device vs. Apple device vs. YD/T 1591) and then we will automatically switch to required communication mode to properly communicate with the device to initiate charging. Finally Pericom will continue to monitor Vbus for over current scenarios and over temperature scenarios and at the same time we will also detect D+/D- load for plug-out detection. Please note, Plug in detection ONLY works when device is in sleep and charge mode.

7.2 Plug out Detection

Once plug-out is detected, then PE/ will once again be pulled high (through external pull-up) and current sensing will resume to determine if a device is plugged in or not. When plug-out detection is not working, PE/ is always pulled high through external pull-up. Plug-out will not work if sleep and charge is not enabled.

7.3 Mouse/Keyboard pass through mode

Since USB1.1 devices do no integrate charging protocols, there is no special charging mode required to support charging the device. Therefore, if a USB Low-Speed external device is detected, then Pericom's solution will simply connect D+/- from the USB connector directly to the USB host controller. The detection process for mouse/keyboard will occur ~1.8 seconds after the Pericom solution enters DCP/auto detect with USB/keyboard pass through enabled mode, which is when CTL1 = 0, CTL2 = 1, and CTL3 = 1. If a low speed device is detected as "attached" at that point, then the pass through mode will be enabled and D+/-P will connect to D+/-H. If the mouse/keyboard is disconnected, while the Pericom's PI5USB2543 remains in the 011 mode, the device will enter auto-charging mode and will enable the PE/ output pin to detect if an external device is connected or not.

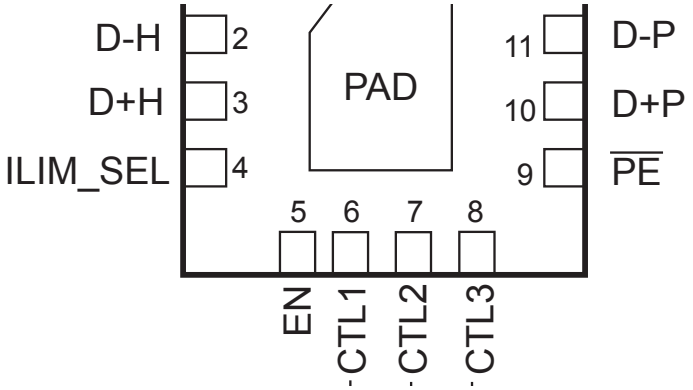
Only in auto-charging mode does Pericom ensure all external battery powered devices will succesfully charge.

7.3.1 System wake-up via external mouse or keyboard

Today's systems are enabled to wake up from S3 mode if a pre-enumerated mouse/keyboard has activity (movement or key-pressed). In order for the system to continue supporting this feature, the USB host controller must be able to communicate with the external device in S3 mode.

Therefore, if a mouse/keyboard is detected (via the USB low speed pass through feature), Pericom's PI5USB2543 will enable the communication between device and controller. Our device will automatically pass the signals through with minimal degradation.

7.4 Recommended Part Configuration



With the above design,

- In S0 mode, setting will be (CTL1,2,3) 1, 1, 1: CDP mode enabled
- In S3 mode, setting will be (CTL1,2,3) 0, 1, 1: DCP with mouse/keyboard pass through enabled
- In S4/S5 mode, setting will be (CTL1,2,3) 0, 0, 1: DCP with mouse/keyboard pass through disabled
- If customer wants to disable charging (perhaps battery power is too low), then CTL3 should be connected to logic Low.
  - In S0 mode, setting will be (CTL1,2,3) 110: normal charging (SDP)
  - In S3 mode, setting will be (CTL1,2,3) 010: Charging is bypassed
  - In S4/S5 mode, setting will be (CTL1,2,3) 000: USB port is completely disabled

7.5 CDP mode description

When PI5USB2543 is configured into CDP mode (see truth table to understand how to configure into CDP mode), D+/-H is connected to D+/-P, allowing communication/enumeration to occur between USB host controller and USB device. The Pericom device will continue to monitor D+ for primary detection and then respond with an acknowledgement on D- (with proper timing) to initiate CDP charging to occur. For secondary detection per the Battery Charger 1.2 spec, Pericom will allow the GND signal from 15Kohm pull-down in the USB controller pass through to the port. Therefore when the cell phone sends 0.6V signal on D-, it will see a GND signal on D+, which will provide a VALID response for CDP, secondary detection.

Once CDP communication has been initiated by external device, the Pericom IC will provide the acknowledge command without affecting USB signal integrity. This acknowledge command will let the external device know that the USB port (Charging downstream port) can support a minimum of 1.5A (per the USB1.2 battery charging spec). The user can set two current limit values, and then by using ILIM_SEL, the user can switch between which limit they would like to use.

Charging Downstream Port (CDP) is the communication protocol found in high charging PCs. These connectors allow USB data to be transferred between the CDP and the external device as well as allow charging to occur up to a max of 1.5A. The actual current draw is managed by the external device, the CDP only limits the max current draw from 1.5A. The communication protocol of CDP is described in the USB Battery Charging Spec revision 1.2. Pericom is able to support this communication.

SDP

Standard Downstream Port (SDP) is the communication protocol found in traditional USB connectors in PCs. These connectors allow USB data to be transferred between the SDP and the external device as well as allow charging to occur up to a max of 500mA. The communication protocol of SDP is described in the USB2.0 and USB3.0 specifications from the USB organization.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +6.0V
DC Input Voltage	-0.5V to V_{DD}+0.5V
DC Output Current	120mA

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40	+25	+85	°C
IN Power Supply Voltage (measured in respect to GND)	+4.75	+5	+5.25	V

Electrical Characteristics (Ambient Temperature -40 to +85°C)

Symbol	Parameter	Conditions			Min	Typ (1)	Max	Unit
V_{IN}	Operating Voltage				4.75		5.25	V
I_{DD}	Supply Current	V_{IN} = 5.25V, V_{EN} = 5V	DCP mode enabled	External device connected		330		µA
				External device not connected		154		
			SDP mode enabled			173		
			CDP mode enabled			215	250	
I_{DDQ}	Quiescent Supply Current	Power Down Mode enabled, V_{IN} = 5.25V, V_{EN} = 0V, CTLx = 0V, ILIM_SEL = High				19		
V_{IH}	Input High Voltage	CTL1, CTL2, CTL3, EN			1.4			V
V_{IL}	Input Low Voltage	CTL1, CTL2, CTL3, EN					0.4	
V_{IH}	Input High Voltage	ILIM_SEL			2.4			V
V_{IL}	Input Low Voltage	ILIM_SEL					0.6	
R_{ON}	Switch On-Resistance for USB 2.0 HS signal (From D+/-H to D+/-P)	V_{IN} = 5V., -0.4V < $V_{INPUT(on\ D+/-\ path)}$ < +0.4V, $I_{INPUT(on\ D+/-\ path)}$ = +30mA				2.5	4	Ω
R_{ON}	Switch On-Resistance for USB 2.0 FS signal (From D+/-H to D+/-P)	V_{IN} = 5V, 0V < V_{INPUT} < 3.3V I_{INPUT} = -15mA				3.5	6	
R_{DSON}	Switch On-Resistance for Vbus path during normal operation	V_{IN} = 5V, IO = 1.5A, V_{INPUT} = 5V				85		mΩ
IOZ	I/O leakage on signal pins (D+/- H, D+/-P) current when port is off	V_{IN} = 5.25V, V_{INPUT} from 0V to 3.6V					+/-2	µA
I_{OFF}	Signal leakage on signal pins (D+/- H, D+/-P) when chip is off	V_{IN} = 0V, V_{INPUT} from 0V to 5.25V					20	

Notes: (1) Typical are at V_{DD} = 5V, T_A = 25 °C ambient and maximum loading.

Capacitance (T_A = -40 to +85°C, f = 1MHz)

Parameter	Description	Test Condition	Typ	Max	Unit
C_{IN}	Control Logic Capacitance		2.5	3.4	pF
C_{OFF} - USB path only	Switch Capacitance across D+/- path when switch is OFF	EN = LOW	3.1	3.4	pF
C_{ON} - USB path only	Switch Capacitance across D+/- path when switch is ON	EN= High	6.0		pF

Dynamic Electrical Characteristics Over the Operating Range (differential)

Parameter	Description	Test Condition	Min	Typ	Max	Units
XTALK	Crosstalk	RL = 50Ω, freq = 240MHz		-29		dB
OIRR	Off-Isolation	RL = 50Ω, freq = 240MHz		-28		
-3dB BW	-3dB Bandwidth (along D+/- path)	RL = 50Ω		1400		MHz
-0.5dB BW	-0.5dB Bandwidth (along D+/- path)	RL = 50Ω		470		
INLOSS	Insertion loss (along D+/- path)	freq = 240MHz		-0.46		dB

(T = 25°C, Vin = 5V, R = 20Kohm, V_{ILIM}= 0V, unless otherwise noted)

Symbol	Parameter	Description	Test Condition	Min	Typ	Max	Units
Input	Input Current, CTL pins	V_{CTL} = 0V or 5.25V		-0.5		0.5	µA
I_{lim} (1)	OUT short circuit current limit	V_{ILIM_SEL} = Logic Low/ High	RRLIM0= 16 kΩ		3200		mA
			RRLIM0= 18 kΩ		2900		mA
			RRLIM0= 22 kΩ		2400		mA
			RRLIM0= 26 kΩ		2000		mA
			RRLIM0= 33 kΩ		1700		mA
			RRLIM0= 50 kΩ		900		mA
t_{IOS}	Response time to short-circuit	VIN = 5.0V			4		µs
Reverse leakage current	V_{OUT} = 5.25V, IN = GND	TJ = 25°C			0.2		µA
REVERSE VOLTAGE PROTECTION							
Reverse-voltage comparator trip point (Vout - Vin)				95	160	190	mV
Time from reverse voltage to power switch turn off				3	5	7	ms
UNDERVOLTAGE LOCKOUT							
Low-level input voltage, IN		V_{IN} rising		3.7		4.6	V
Hysteresis, IN		TJ = 25°C			75		mV
OVERCURRENT $\overline{FAULT}$							
Output low voltage, $\overline{FAULT}$		I_{FAULT} = 1mA				180	mV
Off-state current		$V_{\overline{FAULT}}$= 5V				1	µA
$\overline{FAULT}$ de glitch		$\overline{FAULT}$ de-glitch will filter out the glitches on $\overline{FAULT}$ to stabilize the $\overline{FAULT}$ signal			2		ms
THERMAL SHUTDOWN							
Thermal shutdown threshold				135			°C
Recovery from thermal shutdown				120			
Hysteresis					10		
Thermal shutdown threshold in current limit				130			
OverVoltage protection on OUT		An external voltage higher than 5.9V (typ) to OUT will shutdown power switch and will assert $\overline{FAULT}$		5.7	6.1	6.35	V

Notes: (1) I_{lim} is the current level that will limit the OCP block thereby triggering the FET to turn off.

CDP Mode

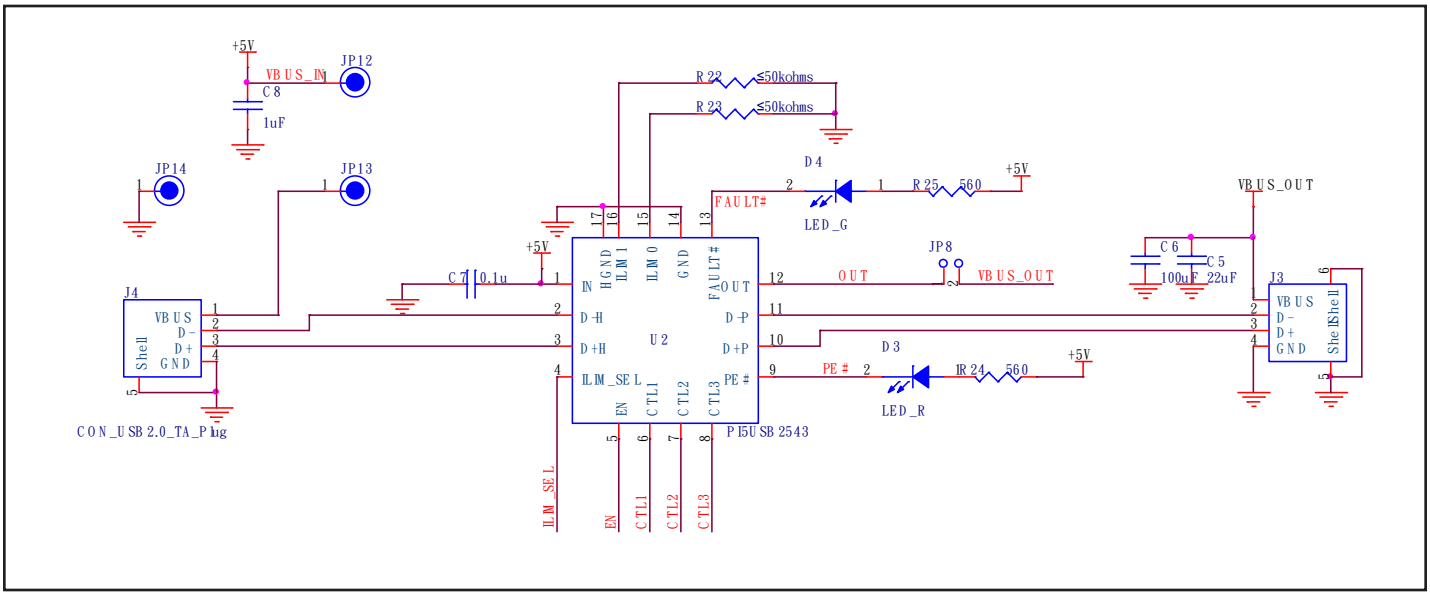
Symbol	Parameter	Test Condition	Min	Max	Units
VDM_SRC	Voltage source on D- for CDP detect	VD-P = 0.6V	0.5	0.7	V
IDP_SINK	DP_IN sink current	0.4V < = VD-P < 0.8V	50	150	uA

Parameter	Description	Test Condition(1)	Min.	Typ.	Max.	Units
Tpd	Propagation delay(2,3)			0.3		ns
Intra-Pair Skew(2)	Output skew, bit to bit (Between + and - of same pair)	See Test Circuit for Electrical Characteristics		10		ps

Charging times after CTL transition from 110 to 011

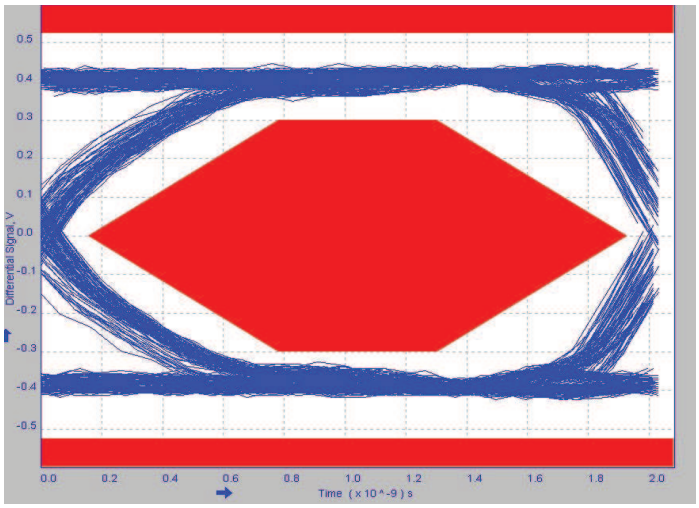
Parameter	Description & Test Condition	Min.	Typ.	Max.	Units
IPad Mode	CTL from 110 to 011		1.5		sec
IPhone Mode	CTL from 110 to 011		2.8		sec
Dedicated Mode	CTL from 110 to 011		2.8		sec

Application Reccomendations & Reference Design Diagram

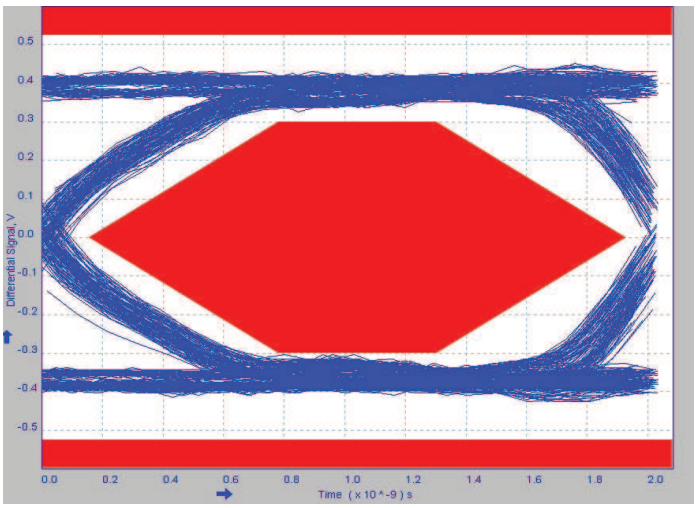


TYPICAL CHARACTERISTICS

EYE Diagram using USB compliance test pattern (with no switch)

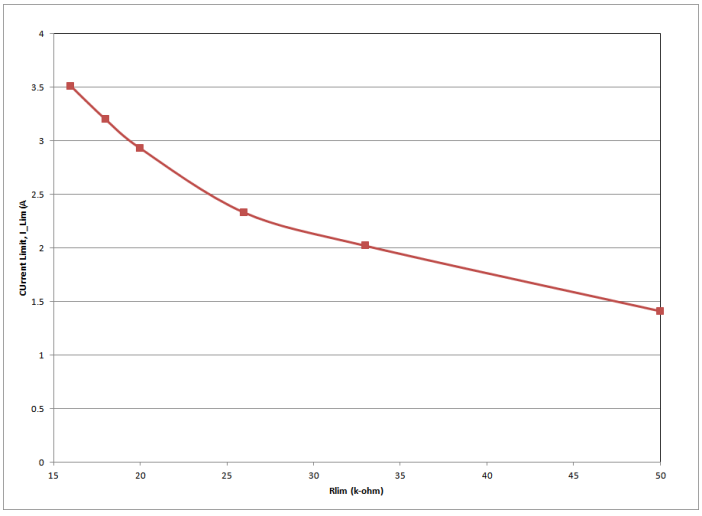


EYE Diagram using USB compliance test pattern (with switch)



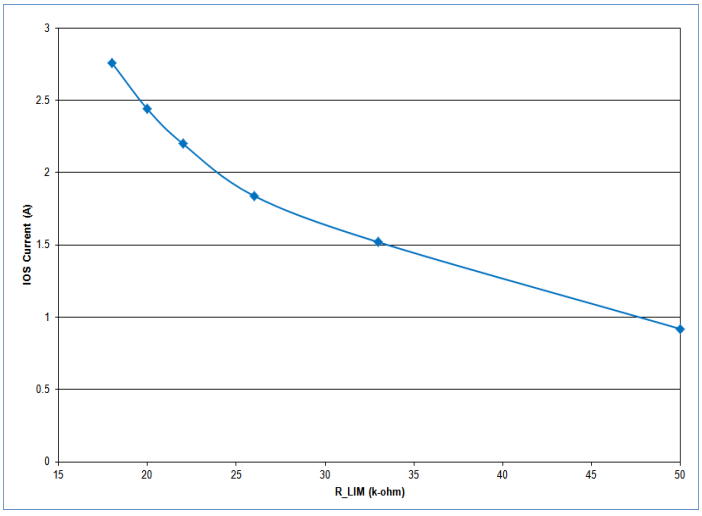
Max Current Allowed:

I_Lim vs Rlim; Vin= 5.0V, 25C



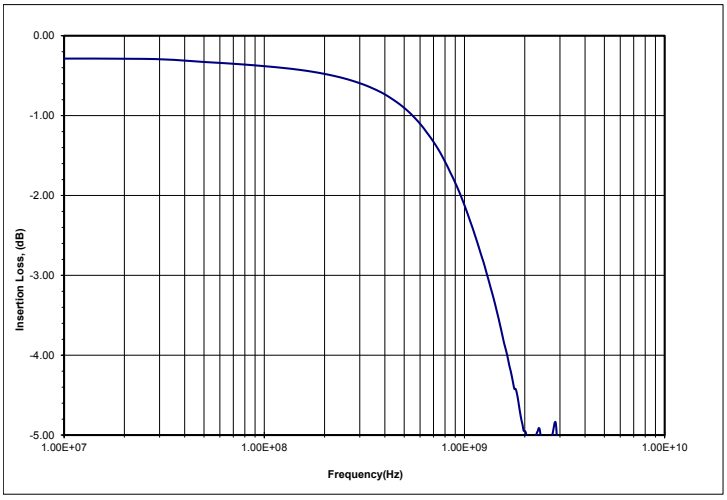
Output Short Circuit Current:

IOS vs Rlim; Vin= 5.0V, 25C

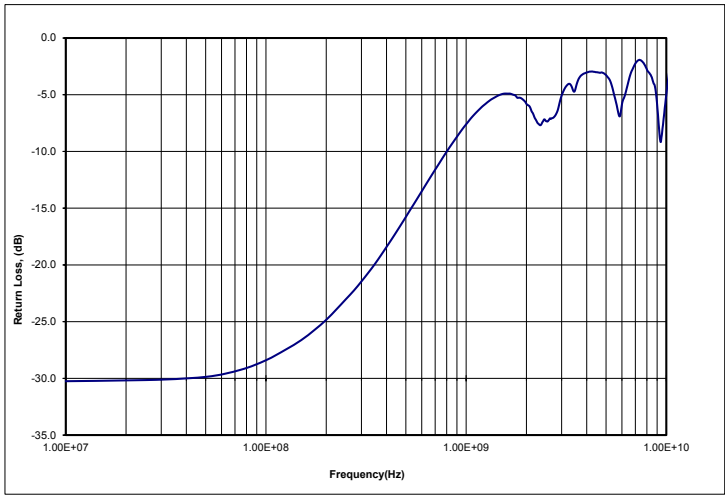


TYPICAL CHARACTERISTICS

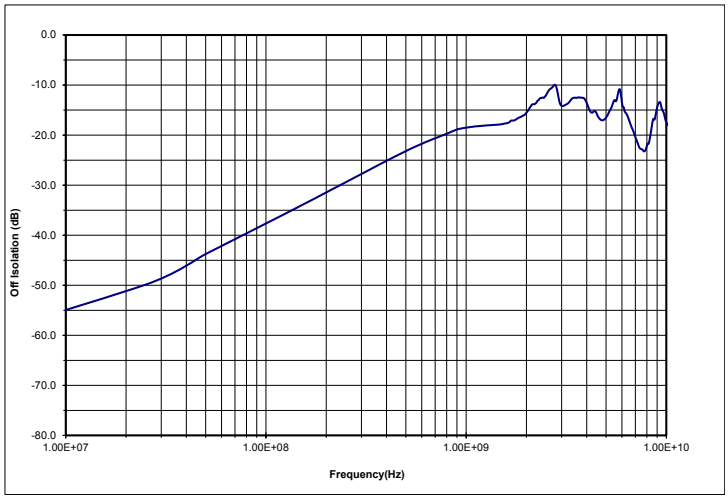
Insertion Loss vs Frequency



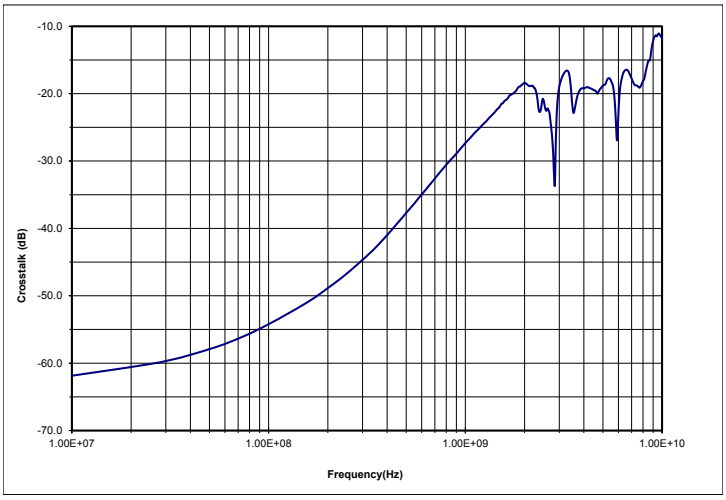
Return Loss vs Frequency

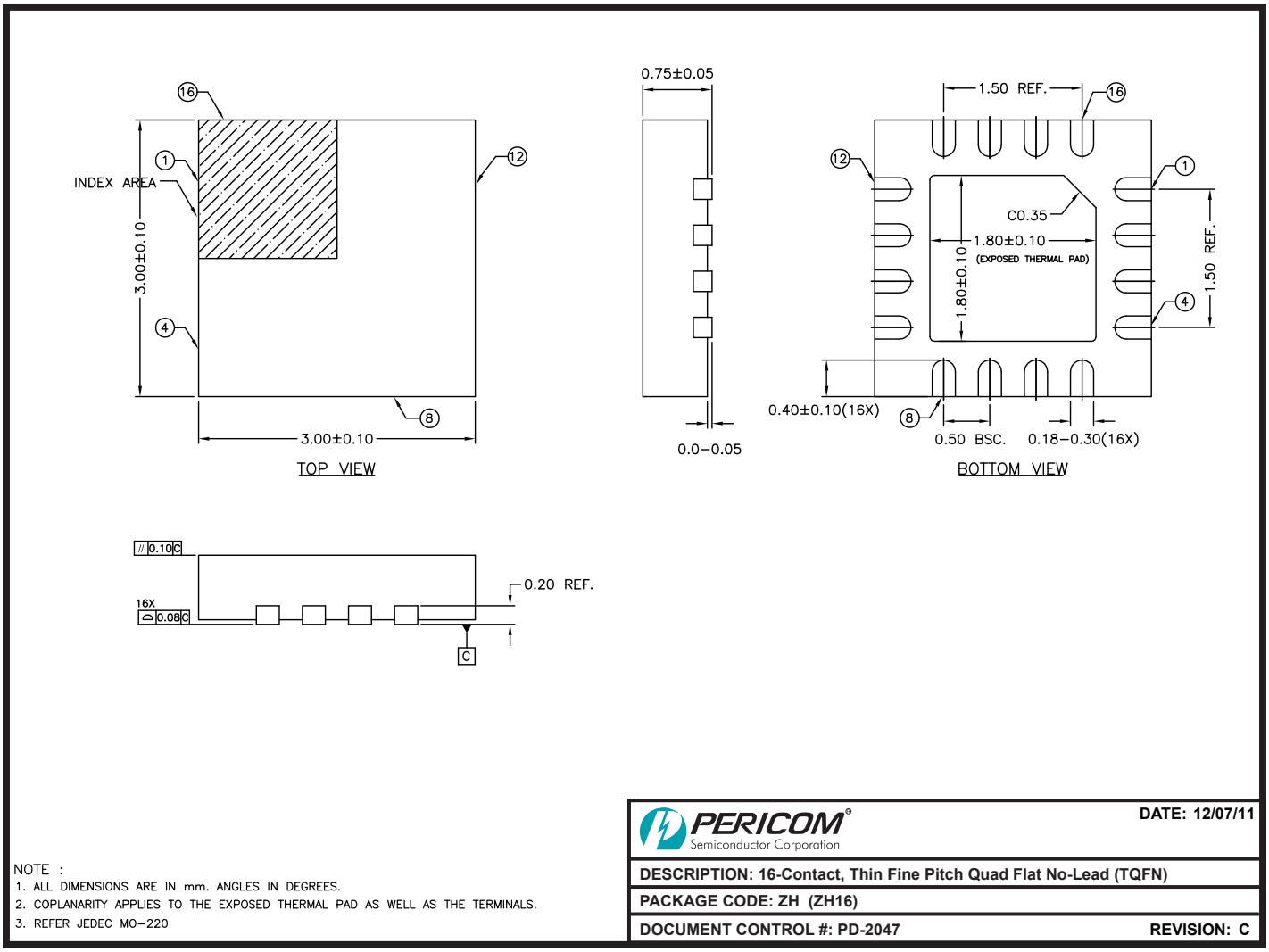


Off Isolation vs Frequency



Cross Talk vs Frequency





NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220

PERICOM Semiconductor Corporation — DATE: 12/07/11

DESCRIPTION: 16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH16)

DOCUMENT CONTROL #: PD-2047 — REVISION: C

11-0236

Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI5USB2543ZHE	ZH	Pb-free & Green, 16-pin TQFN	JK

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- Adding an "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging