3:1 ActiveEye™ HDMI™ Switch with Electrical Idle Detect

Features

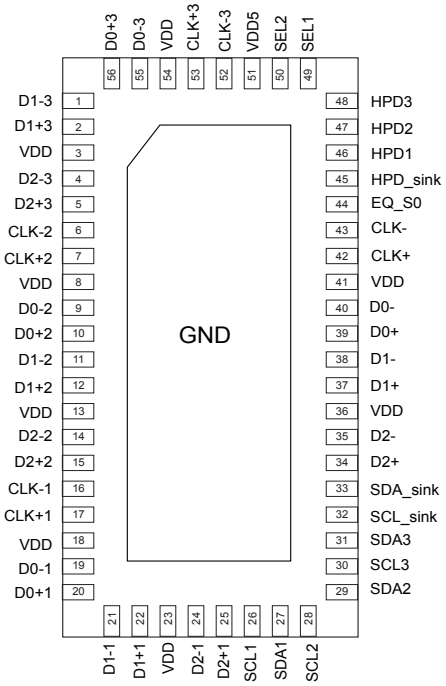
- 3 digital video inputs can be switched to a single output
- Each input can be AC coupled video or DC coupled, while the output will maintain its DC coupled, current-steering, TMDS compliance
- TMDS pixel clock support up to 250MHz max
- Deep Color™ support up to 36bits max per link
- Integrated DDC switch to connect DDC path from HDMI™ input connectors to HDCP block in the HDMI Receiver.
- Can support Clock Stretching on DDC path
- HDCP reset circuitry for quick communication when switching from one port to another
    - Automatic Termination turn-off circuitry when port is deselected
    - Clock Detection: Will disable output TMDS channels when no TMDS pixel clock is present
- Flexible termination;
    - When TMDS channel is off, 50ohm termination is changed to 800Kohm
- Integrated ESD on all TMDS input pins (Dx±Y and CLK±Y; Y = 1, 2, 3 and x = 0, 1, 2)
    - 8kV Human Body Model per JESD22
    - ±5kV contact per IEC61000-4-2
- Optimized Equalization with support for up to 20 meter input cable lengths
- Packaging (Pb-free and Green)
    - 56 contact TQFN (ZFE)
    - 56 pin TSSOP (AE)

Description

Fully compatible HDMI™ signal support with backward compatibility to the DVI 1.0 standard, Pericom's new "ActiveEye™" switch technology is all you need to connect multiple, unknown sources, to a single display. Without any affect on HDCP, these switches can be used almost anywhere. In addition to supporting DC coupled HDMI and DVI inputs, Pericom's PI3HDMI231-A can also level shift an AC coupled HDMI to a DC coupled HDMI output.

Pericom's HDMI product family has been designed specifically to support color depths of up to 12bits per channel, as specified in the HDMI revision 1.3 standard. We have integrated the entire interface solution so the TV designer doesn't have to think about it. This includes, integrated DDC switching.

Pin Description

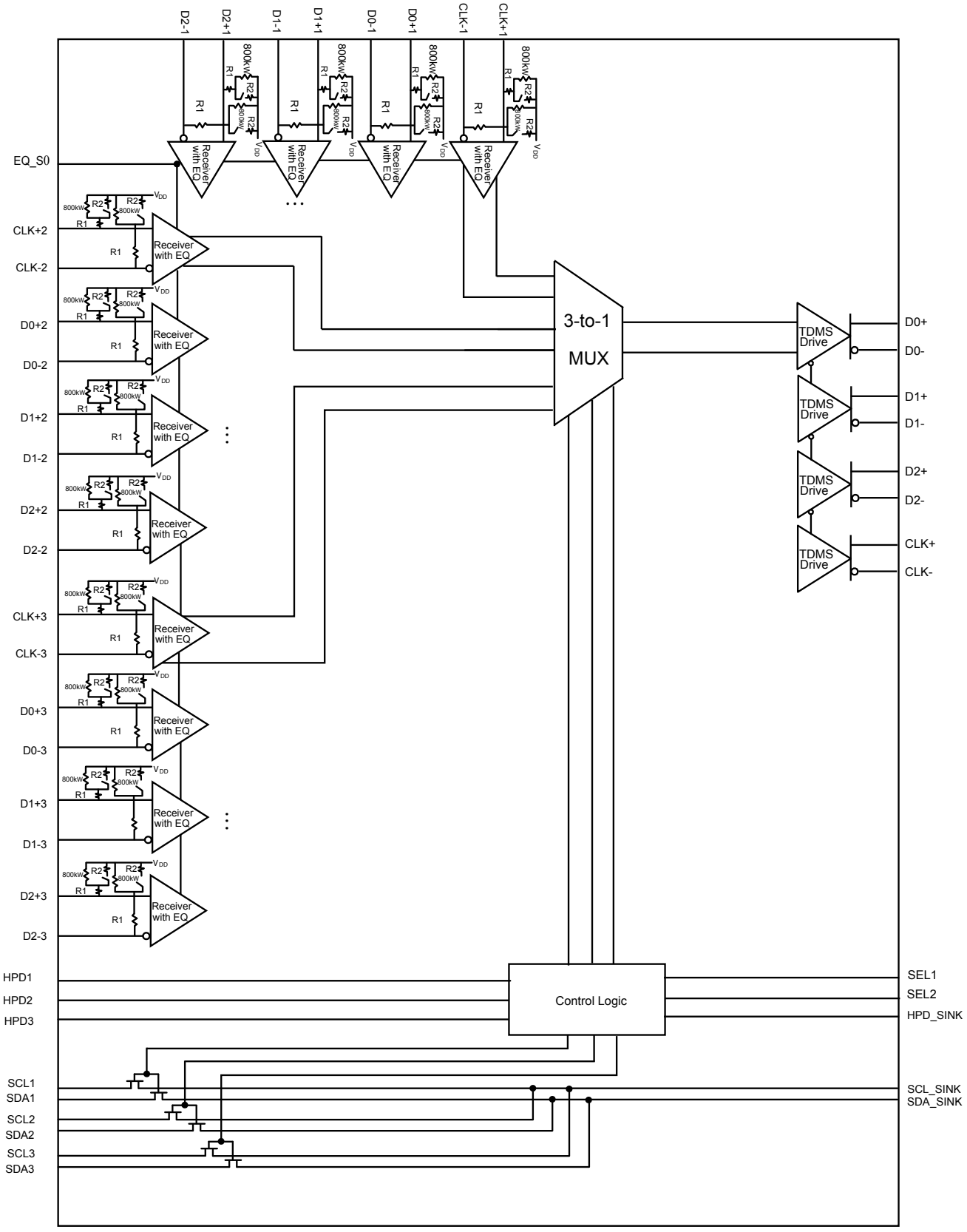


TQFN-56

VDD	1	56	CLK+3
D0-3	2	55	CLK-3
D0+3	3	54	VDD5
D1-3	4	53	SEL2
D1+3	5	52	SEL1
GND	6	51	HPD3
D2-3	7	50	HPD2
D2+3	8	49	HPD1
CLK-2	9	48	HPD_Sink
CLK+2	10	47	EQ_S0
VDD	11	46	CLK-
D0-2	12	45	CLK+
D0+2	13	44	GND
D1-2	14	43	D0-
D1+2	15	42	D0+
GND	16	41	D1-
D2-2	17	40	D1+
D2+2	18	39	VDD
CLK-1	19	38	D2-
CLK+1	20	37	D2+
VDD	21	36	SDA_Sink
D0-1	22	35	SCL_Sink
D0+1	23	34	SDA3
D1-1	24	33	SCL3
D1+1	25	32	SDA2
GND	26	31	SCL2
D2-1	27	30	SDA1
D2+1	28	29	SCL1

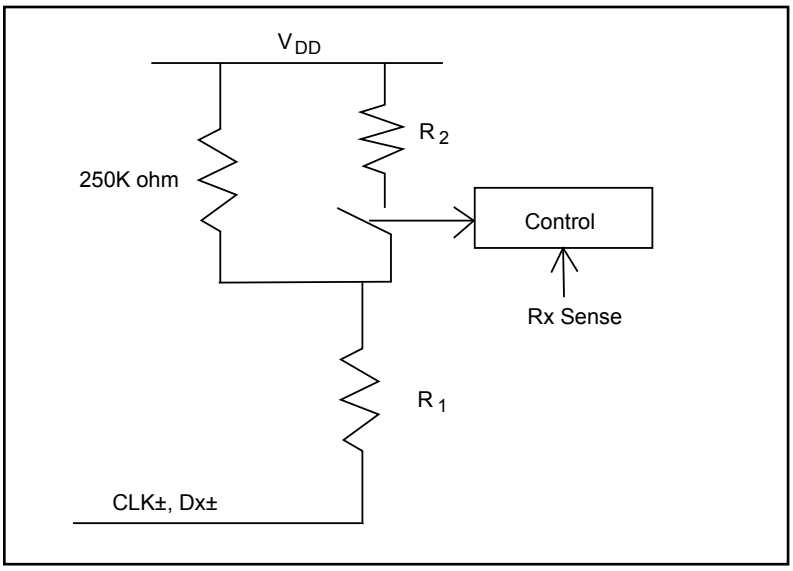
TSSOP-56

Block Diagram



Receiver Block

The HDMI™/DVI receive ports are terminated separately as follows:



Truth Table

EQ_S0(1)	EQ value on TMDS data channels
0	6dB @ 825MHz
1	12dB @ 825MHz

Notes:
1) Internal 100K-ohm pull down resistor

Each input has integrated equalization that can eliminate deterministic jitter caused by 20meter 24AWG cables. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, and DDC signals (R1 + R2 = 50ohm).

Transmitter Block

The transmitter block transmits the HDMI™/DVI data according to HDMI™ revision 1.3 transmitter spec.

Source Selection Look-up Table

Control Bits		I/O Selected		Hot Plug Detect Status		
SEL2	SEL1	TMDS output	SCL_SINK/SDA_SINK	HPD1	HPD2	HPD3
H	H	TMDS Port 1 is active and port 2 and 3 have 50ohm termination disconnected	SCL1/SDA1	HPD_SINK	L	L
H	L	TMDS Port 2 is active and port 1 and 3 have 50ohm termination disconnected	SCL2/SDA2	L	HPD_SINK	L
L	L	TMDS Port 3 is active and port 1 and 2 have 50ohm termination disconnected	SCL3/SDA3	L	L	HPD_SINK
L	H	NONE(Z) All terminations are dis-connected	NONE(Z) Are pulled HIGH by external pull-up termination	HPD_SINK	HPD_SINK	HPD_SINK

Electrical Specifications
Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{DD}	TMDS Supply Voltage	-0.3		4.0	V	1, 2
V_I	Input Voltage	-0.3		VDD+0.3	V	1, 2
V_O	Output Voltage	-0.3		VDD+0.3	V	1, 2
$V_{DD}5$	+5V power supply used during power down situation	-0.3		6.0	V	

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Electrical Specifications
Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	TMDS Analog Supply Voltage	3.135	3.3	3.465	V
$V_{DD}5$	+5V power supply used during power down (from HDMI connector)	4.5		5.5	V
T_A	Ambient Temperature (with power applied)	0	25	70	°C

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_{CC}	Supply current	SEL1/SEL2 = LOW/LOW LOW/HIGH HIGH/HIGH	$V_{IH} = V_{DD}$, $V_{IL} = V_{DD}$-0.6V RT=50Ω, V_{DD}=3.3V TMDS data inputs = 2.5Gbps HDMI data pattern TMDS clock input = 250MHz			120	mA
		SEL1/SEL2 = HIGH/LOW				35	
I_{DD}	5V power supply current consumption	5V is present, SEL1/SEL2 = X				5	mA
I_{CCQ}	3.3V supply current when 5V is not present	5V is not present, SEL1/SEL2 = X				5	mA

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
TMDS Differential pins						
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3V, RT = 50Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}– 400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				15%	2 x Vswing
$V_{OD(U)}$	Undershoot of output differential voltage				25%	2 x Vswing
$DV_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	I_I = 10uA	V_{DD}-10		V_{DD}+10	mV
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω
CLK_Detect	TMDS clock detection for normal operation. Outputs are Hi-Z if CLK signal detected is outside of this Normal operating range	Frequency	15		340	MHz
		Differential Voltage Swing	140			mV
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6V, V_{DD}5 = 5.5V			5	uA
I_{OFF}	Leakage current when V_{DD} is not present	V_{DD} = 0V or open, V_{DD}5 = 5.5V			10	uA

(Continued)

Switching Characteristics (over recommended operating conditions unless otherwise noted)

TMDS Differential Pins						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Units**
tpd	Propagation delay	V_{DD} = 3.3V, R_T = 50-ohm			2000	ps
t_r	Differential output signal rise time (20% - 80%)			140		
t_f	Differential output signal fall time (20% - 80%)			140		
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew				100	
$t_{jit(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data Input = 1.65 Gbps HDMI™ data pattern CLK Input = 165 MHz clock		15	30	
$t_{jit(pp)}$	Peak-to-peak output jitter DATA residual jitter			18	50	
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				600	
t_{dis}	Disable time				10	

DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Units**
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn	C_L = 10pF		0.4	2.5	ns

Control and Status Pins (OC_SX, EQ_SX, S, HPD_SINK, HPD)						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Units**
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPD)	C_L = 10pF		2	6.0	ns
$t_{sx(HPD)}$	Switch time (from port select to the latest valid status of HPD)			3	6.5	

Control Pins						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Units**
I_{IH}	High level digital input current(1)	V_{IH} = 2V or V_{DD}	-10		10	µA
I_{IL}	Low level digital input current(1)	V_{IL} = GND or 0.8V	-10		10	µA
V_{IH}	High Level Digital input Voltage		2.0		$V_{DD}5$	V
V_{IL}	low level digital input voltage		0		0.8	V

(Continued)

DDC I/O Pins						
I_{LK}	Input leakage current	V_I = 0.1 V_{DD} to V_{DD} to isolated DDC inputs	-10		10	µA
C_{IO}	Input/Output capacitance	V_I peak-peak = 1V, 100 KHz			10	pF
R_{ON}	Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	W

HPD Path						
I_{IH}	High level digital input current	V_{IH} = 2V or V_{DD}	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND or 0.8V	-10		10	µA
V_{OH}	Single-ended high level output voltage	I_{OH} = -100µA	2.4		V_{DD}	V
V_{OL}	Single-ended low level output voltage	I_{OL} = 100µA	GND		0.4	V

I^2C Pins (SCL1, SDA1, SCL2, SDA2, SCL3, SDA3)						
I_{ikg}	Input leakage current	V_I = 5.5V	-50		50	µA
		V_I = V_{DD}	-10		10	

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V_{DD} pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitors on each V_{DD} pins, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

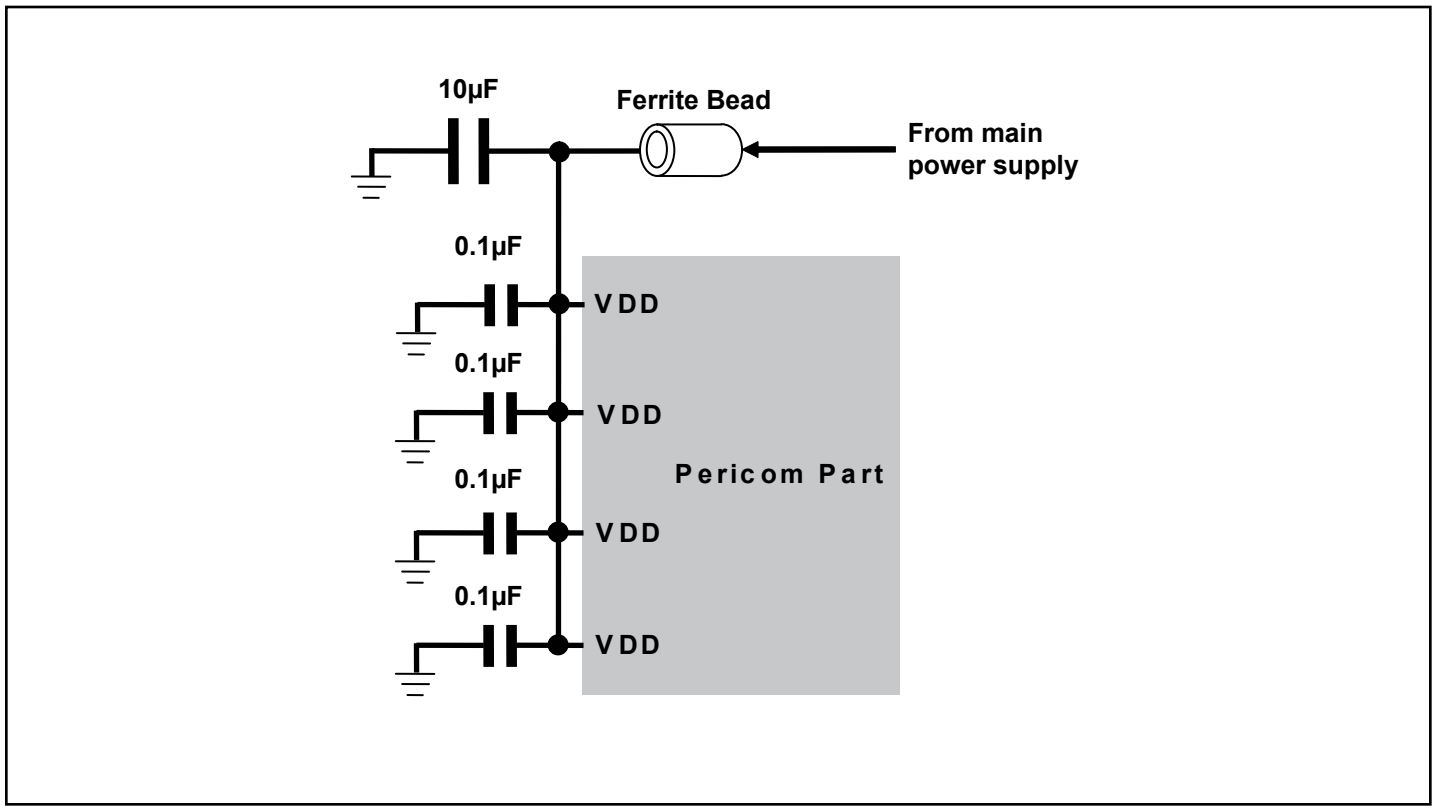


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling CapacitorPlacement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

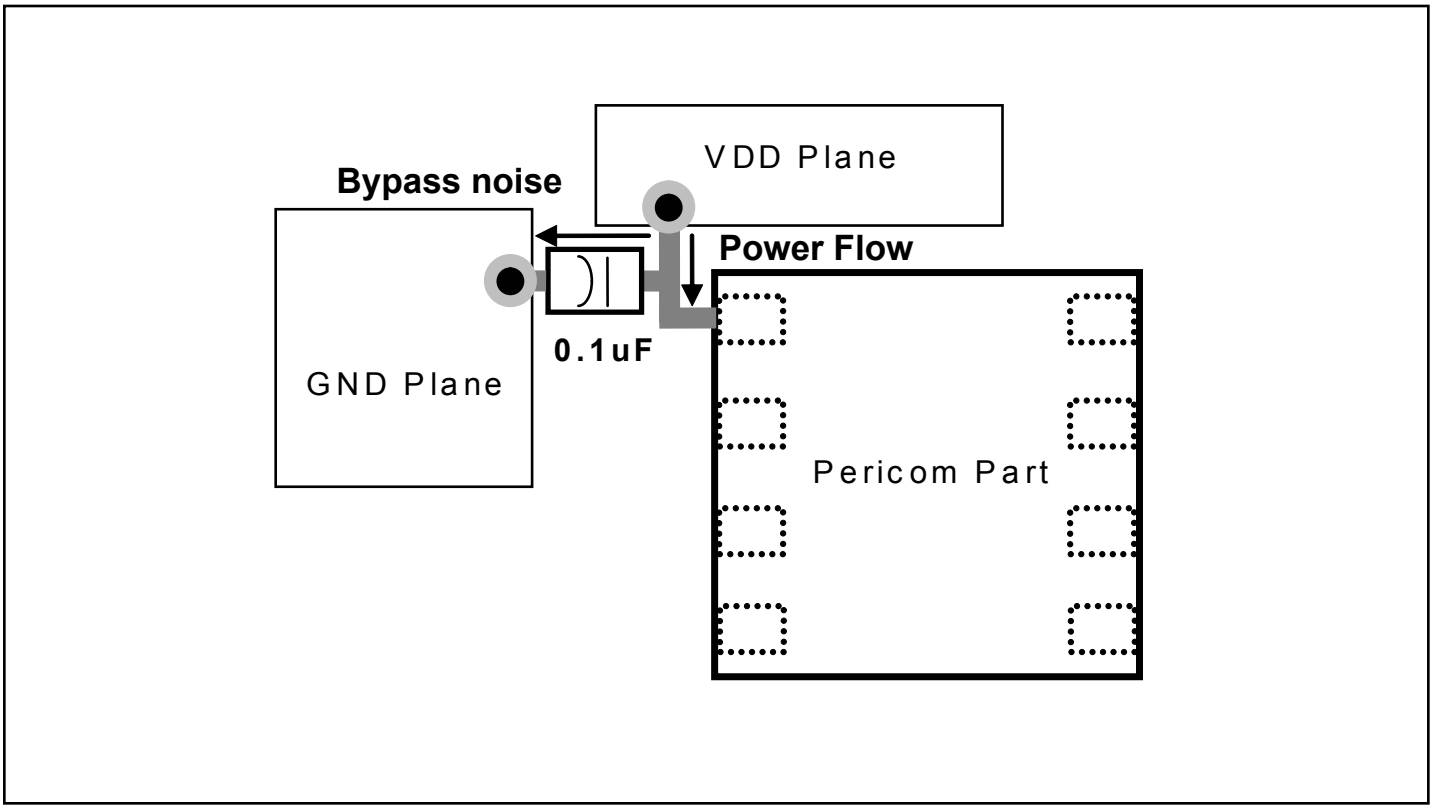
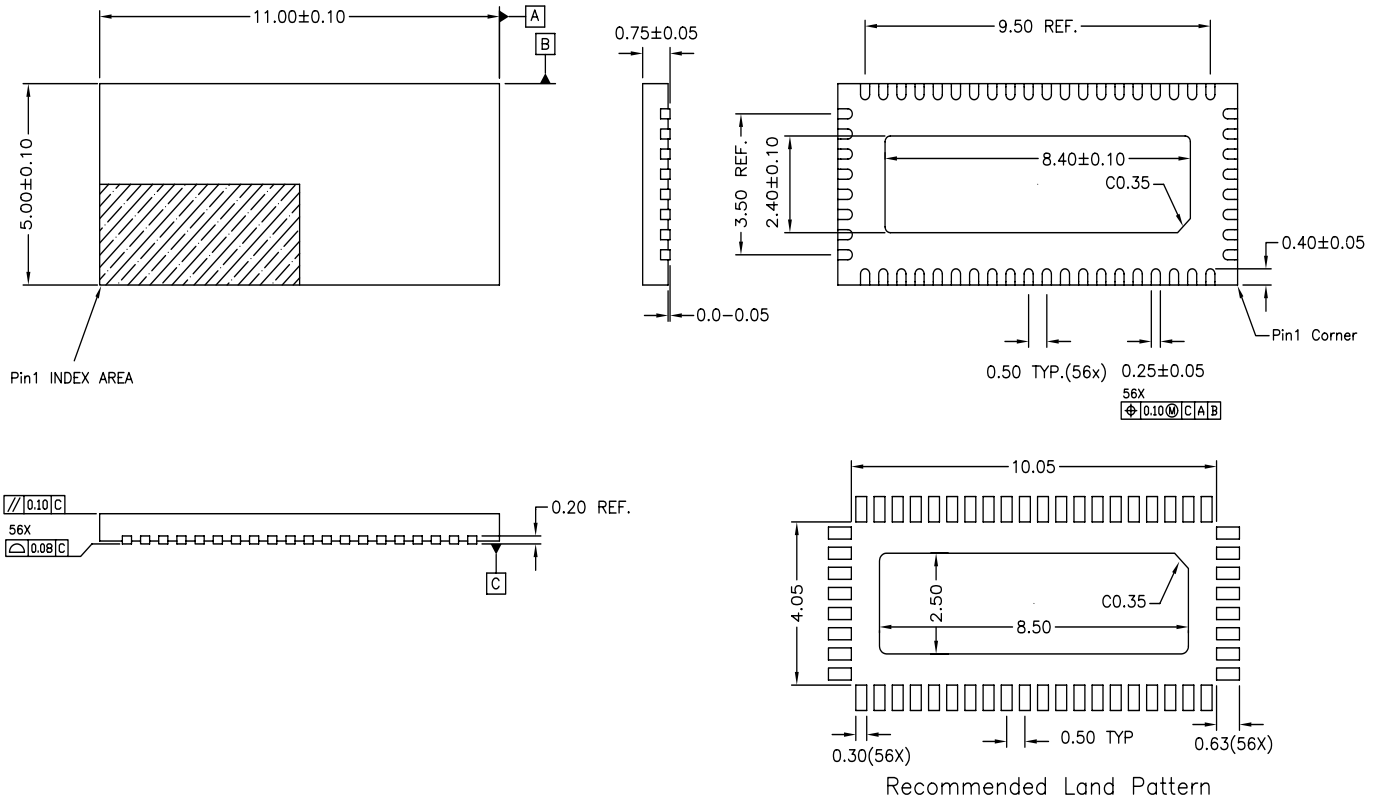


Figure 2 Layout and Decoupling Capacitor Placement Diagram

Package Mechanical: 56-pin, Low Profile Quad Flat Package (ZF56)



NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220 MODIFIED.
4. Thermal Via Diameter. Recommended 0.2~0.33mm
5. Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation

DATE: 05/15/08

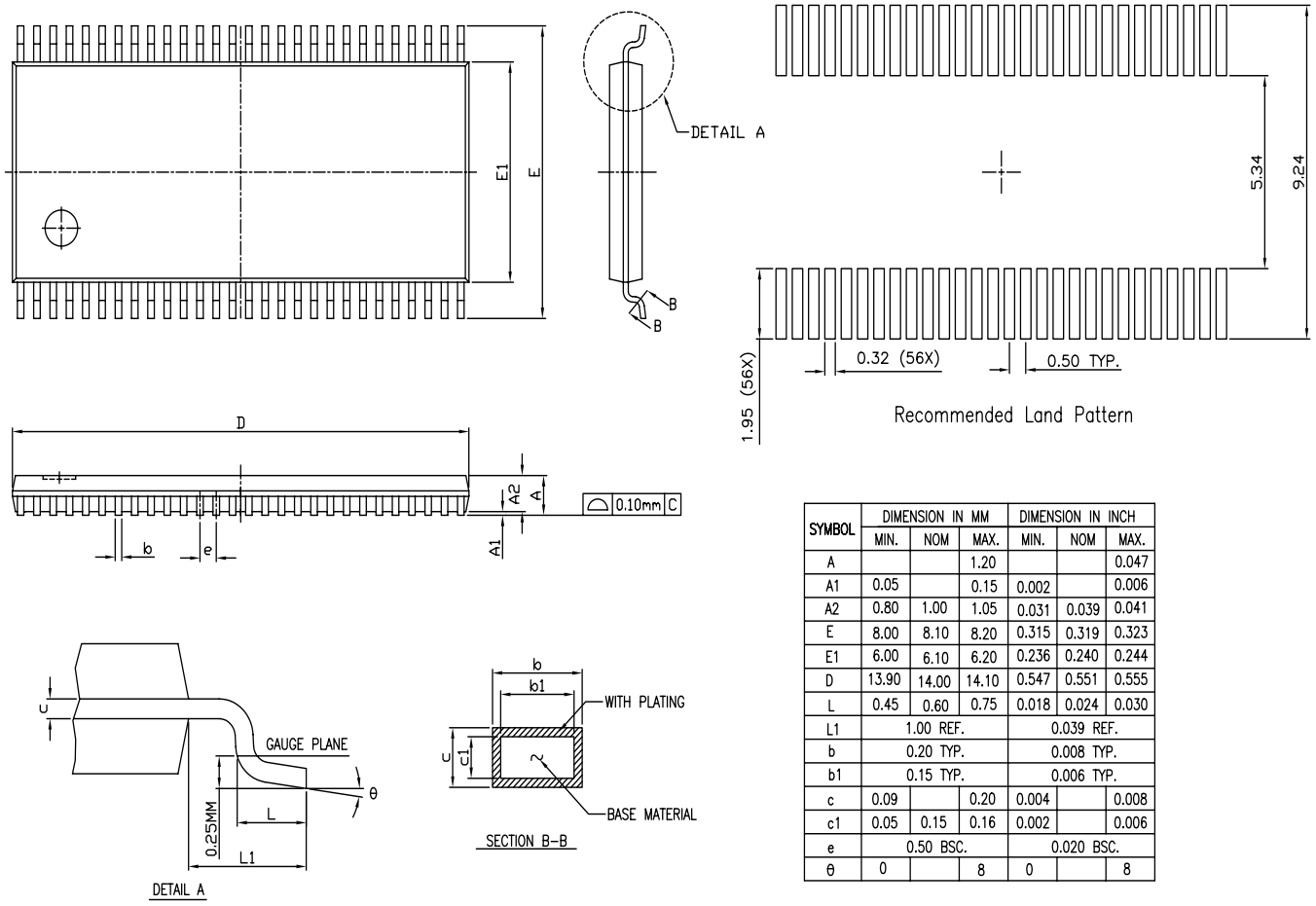
DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)

PACKAGE CODE: ZF56

DOCUMENT CONTROL #: PD-2024 **REVISION: C**

08-0208

Package Mechanical: 56-pin, TSSOP (A56)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
D	13.90	14.00	14.10	0.547	0.551	0.555
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	0.20 TYP.			0.008 TYP.		
b1	0.15 TYP.			0.006 TYP.		
c	0.09		0.20	0.004		0.008
c1	0.05	0.15	0.16	0.002		0.006
e	0.50 BSC.			0.020 BSC.		
θ	0		8	0		8

PERICOM Semiconductor Corporation

DATE: 09/11/06

DESCRIPTION: 56-pin, 240-mil wide TSSOP

PACKAGE CODE: A56

DOCUMENT CONTROL #: PD-1502 REVISION: M

Notes:
1. Controlling dimensions in millimeters.
2. Ref: JEDEC MO-153F/EE
3. Package Outline Exclusive of Mold Flash and Metal Burr

06-0736

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI231-AZFE	ZFE	56-pin, Pb-free & Green TQFN
PI3HDMI231-AAE	AE	56-pin, Pb-free & Green TSSOP

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & Deep Color are trademarks of Silicon Image