

**HDMI™ Switch with non-blocking EQ Circuitry**
**Features**

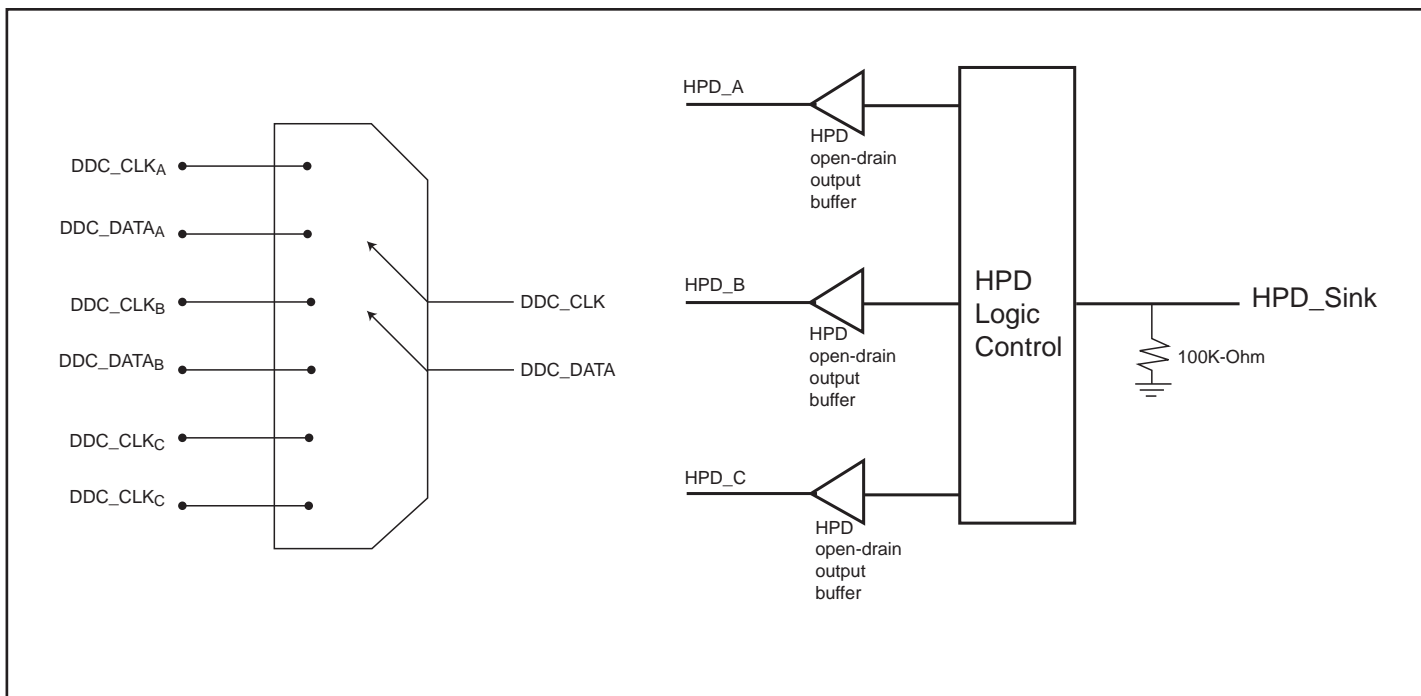
- Differential channel 3:1 Mux/DeMux for TDMS signals
- 3:1 Mux/DeMux for DDC signals
- non-EQ blocking circuitry to utilize ideal EQ found in main receiver chipset
- Low power consumption to support Energy Star Compliance
- Data rate support up to 3.4Gbps (16bit color depth per channel)
- 2 pin control for port selection
- 3.3V power and 5V standby power
- ESD protection on all I/O pins
  - ±8kV contact per IEC61000-4-2
  - 7kV HBM per JESD22
- Packaging (Pb-free & Green): 72 - Contact TQFN

**Description**

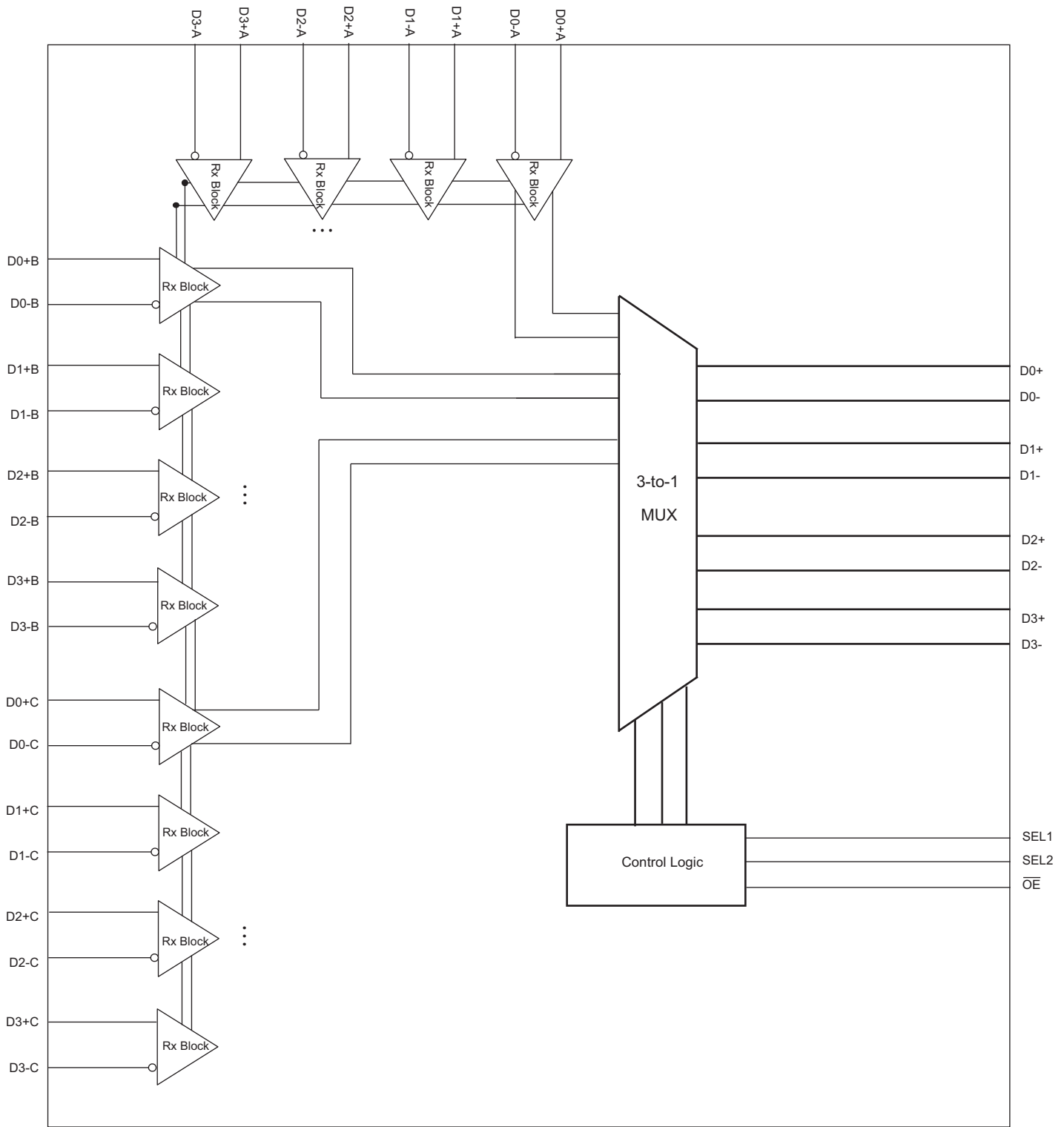
Pericom Semiconductor's PI3HDMI™ series of switch circuits are targeted for high-resolution video networks that are based on DVI/HDMI standards. The PI3HDMI1310-A is a 3-to-1 HDMI Mux/DeMux Switch. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation. The maximum DVI/HDMI data rate of 3.4Gbps provides the resolution required by next generation HDTV and PC graphics. Three differential channels are used for data (video signals for DVI or audio/video signals for HDMI), and one differential channel is used for Clock for decoding the TMDS signals at the outputs.

PI3HDMI1310-A was designed specifically to meet ATC-Sink requirements. Therefore, Pericom recommends locating this switch at the sink to switch between multiple sources.

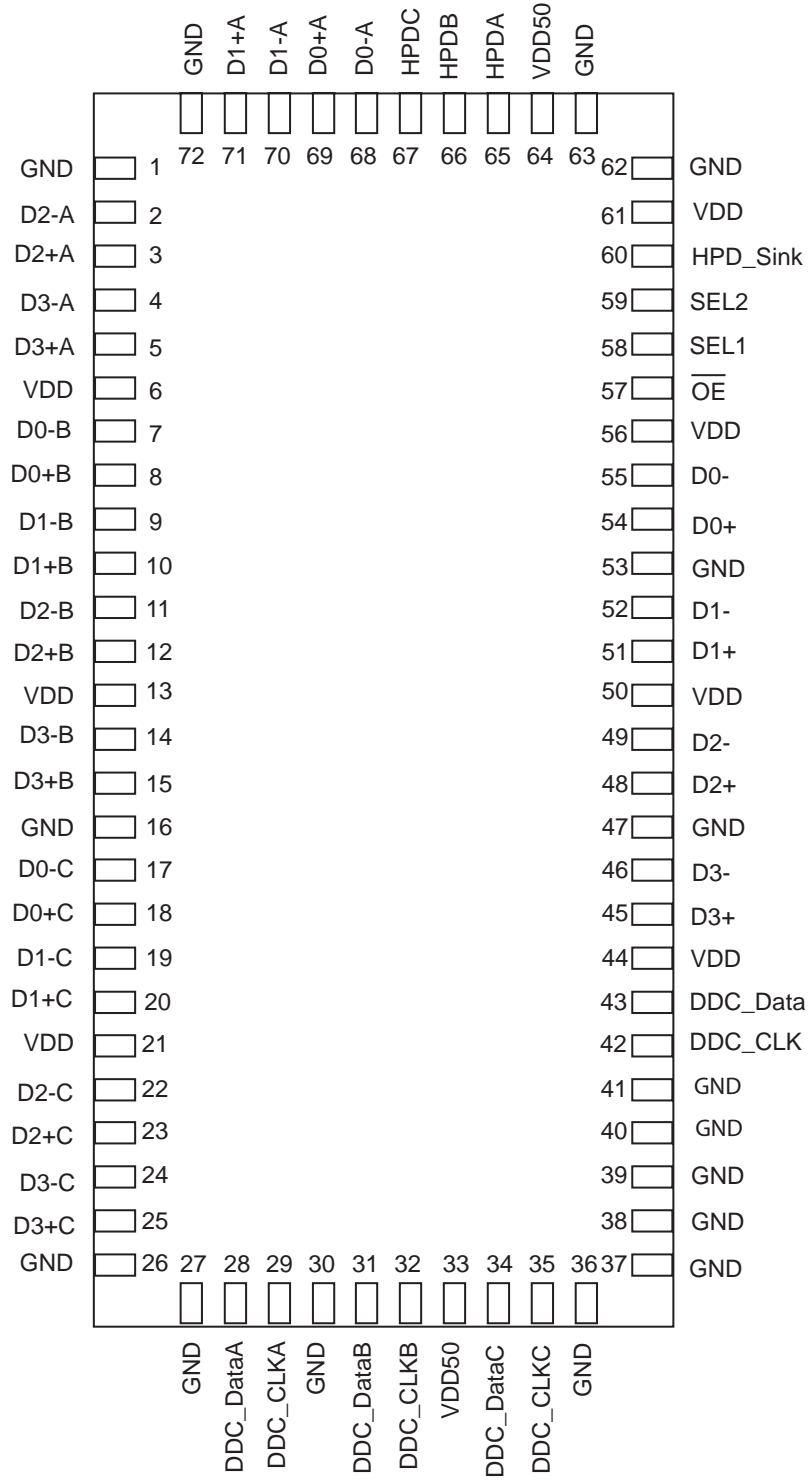
All input pins are protected with Pericom's ESD protection circuits, supporting protection against ESD damage as high as ±8kV contact per IEC6000-4-2 spec.

**Block Diagram (AUX/DDC Switch Channels and HPD Control Channels)**


## High Speed Differential Signal Switch Block



**Pin Configuration (Top View)**



**Pin Description**

Pin #	Pin Name	Pin Type	Description															
69, 68, 71, 70, 3, 2, 5, 4,	Dx±A (X = 0, 1, 2, 3)	I/O	Port A High Speed inputs															
8, 7, 10, 9, 12, 11, 15, 14	Dx±B (X = 0, 1, 2, 3)	I/O	Port B High Speed inputs															
18, 17, 20, 19, 23, 22, 25, 24	Dx±C (X = 0, 1, 2, 3)	I/O	Port C High Speed inputs															
65, 66, 67	HPDA, HPDB, HPDC	Output	HPD open-drain outputs for each port. Logic will follow truth table on page 7. External 1Kohm pull-up to 5V is required															
33, 64	VDD50	Power	5.0V voltage rail from HDMI/DVI connector. Used during standby-mode.															
60	HPD_Sink	Input	GP I/O pin from SCALAR. Internal 100Kohm pull-down.															
29, 28, 32, 31, 35, 34, 42, 43	DDC_CLKx, DDC_Datax	I/O	I <sup>2</sup> C signals for DDC communication on TMDS ports															
55, 54, 53, 52, 51, 49, 48, 46, 45	DX± (x = 0, 1, 2, 3)	I/O	4-differential high speed Output signals															
58, 59	SEL1, SEL2	Inputs	<table border="1"> <thead> <tr> <th>SEL1</th> <th>SEL2</th> <th>Output Port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Port A</td> </tr> <tr> <td>0</td> <td>1</td> <td>Port B</td> </tr> <tr> <td>1</td> <td>0</td> <td>Port C</td> </tr> <tr> <td>1</td> <td>1</td> <td>Hi-Z</td> </tr> </tbody> </table>	SEL1	SEL2	Output Port	0	0	Port A	0	1	Port B	1	0	Port C	1	1	Hi-Z
			SEL1	SEL2	Output Port													
			0	0	Port A													
			0	1	Port B													
1	0	Port C																
1	1	Hi-Z																
6, 13, 21, 44, 50, 56, 61	V <sub>DD</sub>	Power	3.3V Power Supply															
1, 16, 26, 27, 30, 36, 37, 38, 39, 40, 41, 53, 62, 63, 72	GND	Power	Ground.															
57	$\overline{\text{OE}}$	Input	Output enable (Active LOW). When HIGH, all outputs are Hi-Z and chip is placed into Standby Mode. Under Standby Mode, the current supply is from VDD50.															

## BLOCK DIAGRAM EXPLANATION

### DDC Switch Block

Passive NMOS based 3:1 mux for DDC channels from each HDMI/DVI input connector. This section can remain active even when 3.3V supply is gone, as long as 5.0V from TMDS connector is connects to the PI3HDMI1310-A IC.

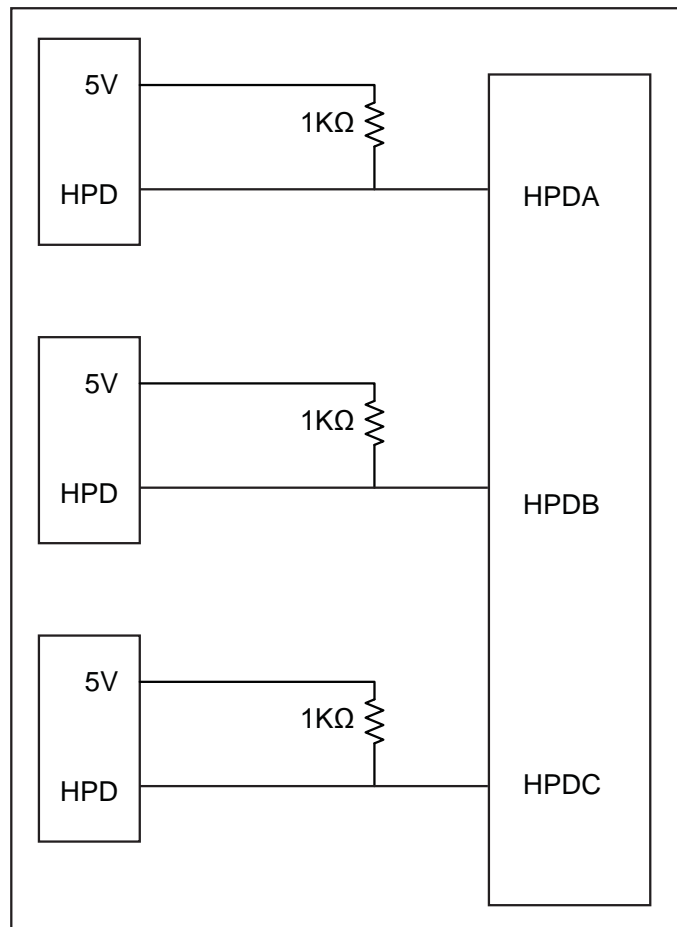
### 3:1 High speed Differential Channel Block

4-differential channels per port. 3 channels are targeted for high speed data channels (250Mbps to 3.4Gbps) and 1 channel is targeted for high speed clock signal (25MHz to 340MHz).

### HPD Control Channels Block

Drives each HPD channels through the input pin, HPD\_Sink.

This signal will need to drive external pull-down transistor circuit before connecting to the HDMI/DVI connector. The external pull down circuit will look like the following:



**Truth table for HPDx signals**

Control Pins				Hot Plug Detect Status		
$\overline{OE}$	SEL1	SEL2	HPD_Sink	HPD A	HPD B	HPD C
x	L	L	L	Hi-Z	Hi-Z	Hi-Z
x	L	L	H	L	Hi-Z	Hi-Z
x	L	H	L	Hi-Z	Hi-Z	Hi-Z
x	L	H	H	Hi-Z	L	Hi-Z
x	H	L	L	Hi-Z	Hi-Z	Hi-Z
x	H	L	H	Hi-Z	Hi-Z	L
x	H	H	L	Hi-Z	Hi-Z	Hi-Z
x	H	H	H	Hi-Z	Hi-Z	Hi-Z

\*All Hi-Z will become H if external pull-up connected at the output.

**Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage to Ground Potential .....	-0.5V to +3.6V
DC Input Voltage .....	-0.5V to 3.6V
DC Output Current .....	120mA
Power Dissipation .....	0.5W

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics for Switching over Operating Range** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ )

Parameter	Description	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units
$V_{IH}$	Input HIGH Voltage	Guaranteed HIGH level	1.5			V
$V_{IL}$	Input LOW Voltage	Guaranteed LOW level	-0.5		0.65	
$V_{IK}^{(1)}$	Clamp Diode Voltage	$V_{DD} = \text{Max.}, I_{IN} = -18\text{mA}$		-0.7	-1.2	
$I_{IH}$	Input HIGH Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}$			$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{DD} = \text{Max.}, V_{IN} = \text{GND}$			$\pm 5$	
$I_{OFF}$	Off Leakage Current	$V_{DD} = 0\text{V}$			10	
<b>Status Pins (HPD_SINK)</b>						
$V_{IH}$	LVTTL Input HIGH Voltage		2		5.3	V
$V_{IL}$	LVTTL Input LOW Voltage		GND		0.8	
$R_p$	Pull-down Resistance	$V_{DD50} = 5.0\text{V}$		100K		Ohm

1. Substrate diode voltage drop. For testing reference.

**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
I <sub>DD</sub>	Operating Power Supply Current	V <sub>DD</sub> = Max., V <sub>SELx</sub> = GND or V <sub>DD</sub>		6	10	mA
I <sub>DDQ</sub>	Standby Supply Current	$\overline{\text{OE}}$ - High		3	5	

**Dynamic Electrical Characteristics Over the Operating Range** (T<sub>A</sub> = -40° to +85°C, V<sub>DD</sub> = 3.3V ±10%, GND=0V)

Parameter	Description	Test Conditions	Min	Typ. <sup>(2)</sup>	Max	Units
X <sub>TALK</sub>	Crosstalk on High Speed Channels	See Fig. 3 for Measurement Setup	f = 1.13 GHz	-34		dB
			f = 825 MHz	-36		
O <sub>IRR</sub>	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f = 1.13 GHz	-28		dB
			f = 825 MHz	-32		
I <sub>LOSS</sub>	Differential Insertion Loss on High Speed Channels (see figure 1)	DR = 1.54Gbps DR = 2.0Gbps DR = 2.25Gbps DR = 3.0Gbps DR = 3.4Gbps		-1.5 -1.73 -1.82 -1.99 -2.08		dB
BW	-3dB BW for TMDS channels			3.0		GHz
<b>Status Pins (HPD) - open drain output buffer</b>						
V <sub>OL(TTL)</sub>	TTL Low-level output voltage	I <sub>OL</sub> = 4mA			0.4	V

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C ambient and maximum loading.

Fig.1 Differential Insertion Loss and Return Loss Test Circuit

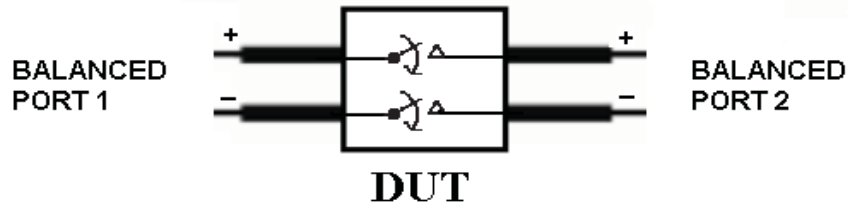


Fig.2 Differential Off Isolation Test Circuit

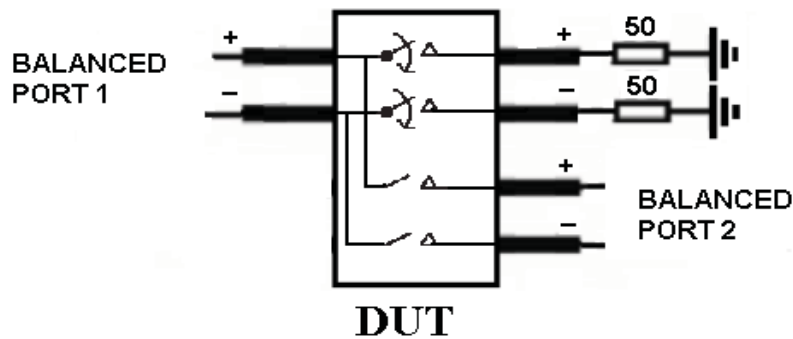
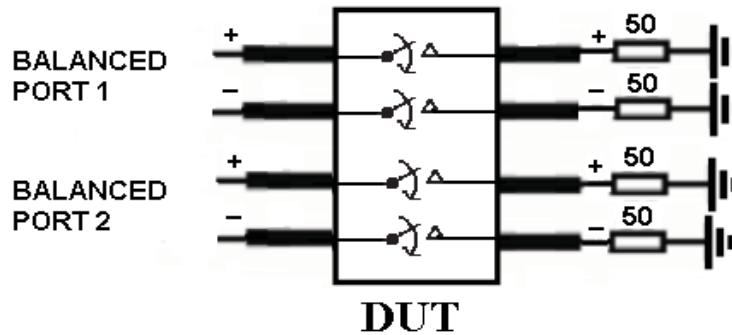


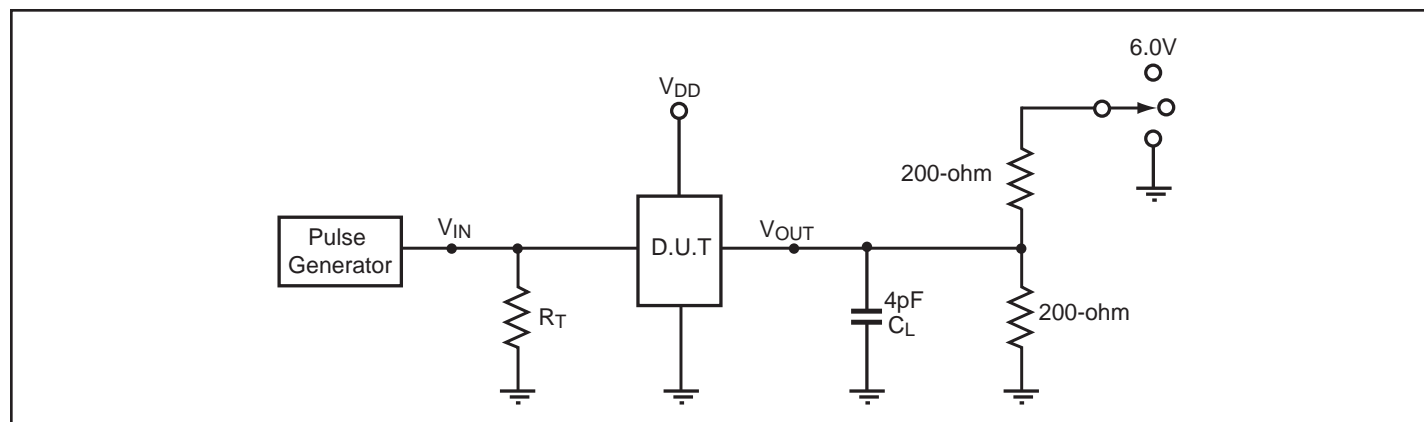
Fig.3 Differential Near End Crosstalk Test Circuit



**Switching Characteristics** ( $T_A = -40^\circ$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ )

Parameter	Description	Min.	Max.	Units
$t_{PZH}$ , $t_{PZL}$	Line Enable Time	0.5	25	ns
$t_{PHZ}$ , $t_{PLZ}$	Line Disable Time	0.5	25	
$t_{b-b}$	Bit-to-bit skew within the same differential pair		15	ps
$t_{ch-ch}$	Channel-to-channel skew		35	

**Test Circuit for Electrical Characteristics<sup>(1-5)</sup>**



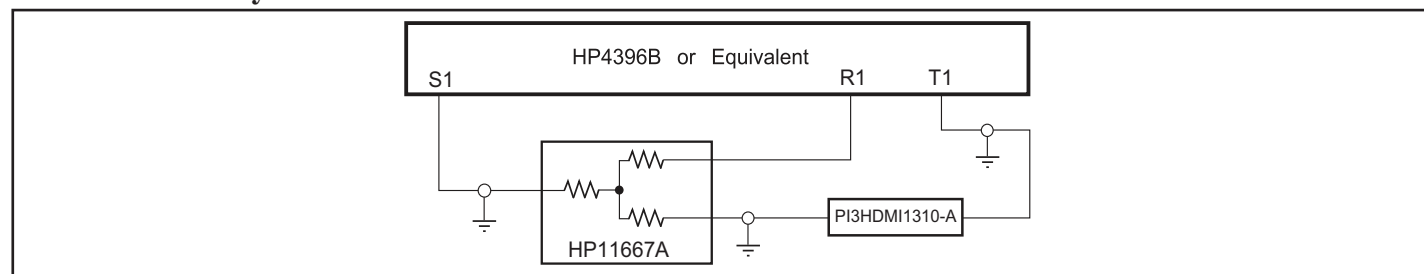
**Notes:**

- $C_L$  = Load capacitance: includes jig and probe capacitance.
- $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator
- Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics:  $PRR \leq \text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_R \leq 2.5\text{ns}$ ,  $t_F \leq 2.5\text{ns}$ .
- The outputs are measured one at a time with one transition per measurement.

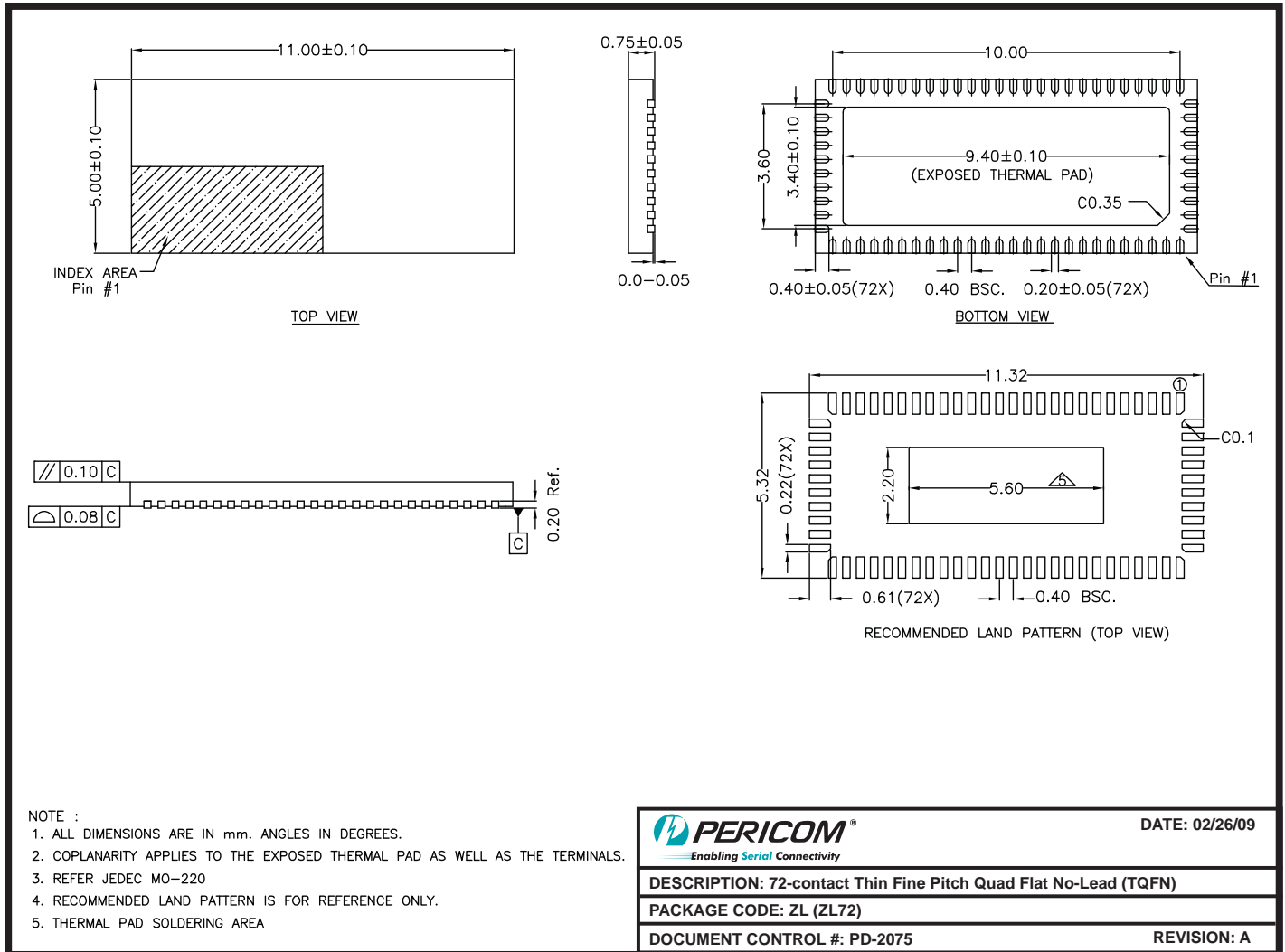
**Switch Positions**

Test	Switch
$t_{PLZ}$ , $t_{PZL}$ (output on B-side)	6.0V
$t_{PHZ}$ , $t_{PZH}$ (output on B-side)	GND
Prop Delay	Open

**Test Circuit for Dynamic Electrical Characteristics**



**Packaging Mechanical: 72-Contact TQFN**



09-0134

**Note:**

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information**

Ordering Code	Package Code	Package Description
PI3HDMI1310-AZLE	ZL	Pb-free and Green 72-contact TQFN

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging