

Ceramic Heating Controller (LCD)

Features

- High watt density Alumina Heaters
- Pulse trigger with high current for SCR
- Quickly Heat-Up and Quickly Lost-Heat Recover
- External adjustable to fit wide range heating plates
- External adjustable to fit TCR of sensors
- Full temperature compensation and insensitive to environment temperature
- Internal zener
- 11 heat temperature settings
- Auto power off for PT8A3351/3/5/7
- Backlights for indicating work status
- LCD screen for showing temperature setting
- Dual Temperature (Fahrenheit/Centigrade) Display
- Wet function: It will keep heating on state to level 2.
- Dual voltage (120V/240V) operations.
- Support 3 keys, on/off, up and down
- SOIC-24, QFN-24 and TSSOP-24 package

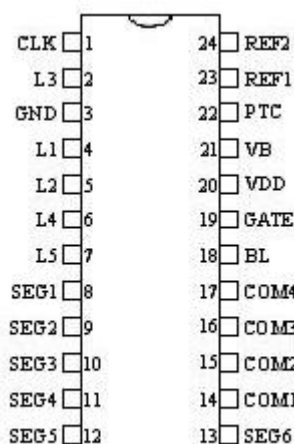
Description

The PT8A335xA/B is special designed for ceramic heating control with 11 temperature levels(show as below function comparison table). It can drive SCR directly and detect heater temperature by heater-self without extra temperature sensor. It has 3 keys for function setting. LCD displays and backlight indicate the working status. Build-in timer will be auto-power off after power on 1 hour for 60Hz or 1.2 hour for 50Hz.

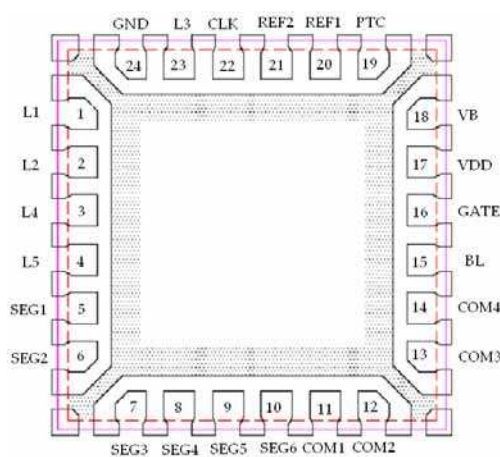
Applications

- Ceramic heating controller

Pin Configuration



SOIC-24/TSSOP-24



QFN-24

Pin Description

Name	Pin No.		Type	Description
	SOIC-24/TSSOP-24	QFN-24		
CLK	1	22	I	Clock input from power line and Detect operation voltage.
L3	2	23	I	Input to adjust Recovery Rate.
L1	4	1	I	Power on/off key inputs
L2	5	2	I	Up and down key inputs.
L4	6	3	I	High: LCD shows °F, Low : LCD shows °C.
L5	7	4	I	Supply LCD power.
SEG1,SEG2, SEG3,SEG4, SEG5,SEG6,	8,9,10,11,12,13	5,6,7,8,9,10	O	LCD digits control output.
COM1,COM 2, COM3,COM 4	14,15,16,17	11,12,13,14	O	LCD digits control output.
BL	18	15	O	Drive LCD backlight
GATE	19	16	O	SCR trigger output, active high
VB	21	18	O	PTC sampling power source
PTC	22	19	I	Temperature sensor input
REF1	23	20	I	Reference 1 for internal comparator
REF2	24	21	O	Reference 2 for internal comparator
GND	3	24	Power	Ground and Power
VDD	20	17		

The block diagram illustrates the internal architecture of the L3960 LCD controller and its connections to external L3, L4, and L5 signals. Key components and their interconnections are as follows:

- Internal Components:**
 - POR (Power-On Reset):** Receives `rst` and outputs `rst` to the `Line Clk Sample` block.
 - Line Clk Sample:** Receives `CLK` and outputs `50Hz` to the `OSC` block.
 - OSC (Oscillator):** Outputs `80kHz` to the `Recover ADJ` block and provides a `stop` signal to the `Timing` block.
 - Recover ADJ:** Receives `L3` and provides a signal to the `Timing` block.
 - Timing:** Receives `stop` and `Recover ADJ` signals. It outputs `ptci` to the `CTRL` block and `vbo` to the `Res Chain` block.
 - CTRL (Control):** Receives `ptci` and `vbo` signals. It outputs `LEVEL` to the `Level Set` block and `GATE` to the `Res Chain` block.
 - Level Set:** Receives `LEVEL` and outputs `LEVEL` to the `KEY IN` block.
 - KEY IN:** Receives `LEVEL` and outputs `BL` to the `L1 (Up/Dn)` signal.
 - Res Chain (Resistor Chain):** Receives `VB`, `REF1`, `REF2`, and `GATE` signals. It outputs `VB` to the `Level Set` block and `ptci` to the `CTRL` block.
 - LCD Driver:** Receives `Vlcd` from the `L5` signal and outputs `COM1` through `SEG6` to the `L4` signal. It also receives `F_C select` from the `L4` signal.
 - Test:** Receives `test1` through `test6` signals and outputs `test1` through `test6` signals.
 - TIMER:** Receives `Timer_rst` and outputs `Timer_rst` to the `CTRL` block.
- External Signals:**
 - L3:** Provides a signal to the `Recover ADJ` block.
 - L4:** Provides `F_C select` to the `LCD Driver`.
 - L5:** Provides `Vlcd` to the `LCD Driver`.
 - COM1, COM2, COM3, COM4, SEG1, SEG2, SEG3, SEG4, SEG5, SEG6:** Output signals from the `LCD Driver`.
 - BL:** Output signal from the `KEY IN` block.
 - L1 (Up/Dn), L2 (On/Off):** Input signals to the `KEY IN` block.
 - VB, REF1, REF2, GATE:** Input signals to the `Res Chain` block.
 - rst:** Input signal to the `POR` block.
 - CLK:** Input signal to the `Line Clk Sample` block.
 - 50Hz, 80kHz:** Internal clock signals.
 - stop:** Internal signal from the `OSC` block to the `Timing` block.
 - ptci, vbo:** Internal signals between the `CTRL` and `Res Chain` blocks.
 - LEVEL:** Internal signal between the `CTRL` and `Level Set` blocks.
 - test1, test2, test3, test4, test5, test6:** Test signals to and from the `Test` block.
 - Timer_rst:** Input signal to the `TIMER` block.

Storage Temperature	-55°C to +150°C
Ambient Temperature with Power applied.....	-20°C to +85°C
Supply Voltage to Ground Potential (Input & V _{DD} Only)	-0.5V to +6.5V
Supply Voltage to Ground Potential (Output s Only)	-0.5V to +6.5V
DC Input Voltage	-0.5V to +6.5V
Input/Output Current	50mA
Input/Output Current (Pin VDD, VB only).....	200mA
Power Dissipation	500mW

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Sym	Parameter	Pin	Min	Typ	Max	Unit
V _{DD}	Operating Voltage	VDD	4.0	-	V _Z	V
T _A	Operating temperature	-	-20	-	85	°C