



**Pin Description<sup>(1)</sup>**

| Name             | Pin #       | Type | Description  |
|------------------|-------------|------|--|
| V <sub>EE</sub>  | 8           | P    | Connect to negative power supply   |
| CLK_SEL          | 2           | I    | Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50kΩ pull down. |
| CLK0             | 3           | I    | Differential LVPECL clock input with 75kΩ pull-down  |
| /CLK0            | 4           | I    | Inverting differential LVPECL clock input. Defaults to V <sub>DD</sub> /2 if left floating.                              |
| CLK1             | 6           | I    | Differential LVPECL clock input with 75kΩ pull-down  |
| /CLK1            | 7           | I    | Inverting differential LVPECL clock input. Defaults to V <sub>DD</sub> /2 if left floating.                              |
| NC               | 5           |      | No Connect   |
| V <sub>DDO</sub> | 9,16, 25,32 | P    | Output Power pin   |
| V <sub>DD</sub>  | 1           | P    | Core Power Supply  |
| Q3, /Q3          | 24,23       | O    | Differential output pair, LVPECL interface level.  |
| Q2, /Q2          | 27,26       | O    | Differential output pair, LVPECL interface level.  |
| Q1, /Q1          | 29,28       | O    | Differential output pair, LVPECL interface level.  |
| Q0, /Q0          | 31,30       | O    | Differential output pair, LVPECL interface level.  |
| Q9, /Q9          | 11,10       | O    | Differential output pair, LVPECL interface level.  |
| Q8, /Q8          | 13,12       | O    | Differential output pair, LVPECL interface level.  |
| Q7, /Q7          | 15,14       | O    | Differential output pair, LVPECL interface level.  |
| Q6, /Q6          | 18,17       | O    | Differential output pair, LVPECL interface level.  |
| Q5, /Q5          | 20,19       | O    | Differential output pair, LVPECL interface level.  |
| Q4, /Q4          | 22,21       | O    | Differential output pair, LVPECL interface level.  |

**Note:**

1. I = Input, O = Output, P = Power supply connection.

**Pin Characteristics**

| Symbol | Parameter                        | Conditions | Min. | Typ. | Max. | Units |
|--------|----------------------------------|------------|------|------|------|-------|
| R      | Input Pullup/Pulldown Resistance |            |      | 50   |      | kΩ    |

**Control Input Function Table**

| Inputs | Outputs |
|--------|---------|
| 0      | CLK0    |
| 1      | CLK1    |

### Absolute Maximum Ratings<sup>(1)</sup>

| Symbol           | Parameter                           | Conditions        | Min  | Typ | Max                   | Units   |
|------------------|-------------------------------------|-------------------|------|-----|-----------------------|---------|
| V <sub>DD</sub>  | Supply voltage                      | Referenced to GND |      |     | 4.6                   | V       |
| V <sub>IN</sub>  | Input voltage                       | Referenced to GND | -0.5 |     | V <sub>DD</sub> +0.5V | V       |
| I <sub>OUT</sub> | Surge Current                       |                   |      |     | 100                   | mA      |
| T <sub>STG</sub> | Storage temperature                 |                   | -65  |     | 150                   | °C      |
| V <sub>BB</sub>  | Smk/source Current, I <sub>BB</sub> |                   | -0.5 |     | +0.5                  | mA      |
| Θ <sub>jA</sub>  | Package Thermal Resistance          |                   |      |     | 86                    | °C/Watt |
| Θ <sub>jC</sub>  | Package Thermal Resistance          |                   |      |     | 12.7                  | °C/Watt |

**Note:**

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Operating Conditions

| Symbol           | Parameter                   | Conditions | Min   | Typ | Max | Units |
|------------------|-----------------------------|------------|-------|-----|-----|-------|
| V <sub>DD</sub>  | Power Supply Voltage        |            | 3.0   |     | 3.6 | V     |
| V <sub>DDO</sub> | Output Power Supply Voltage |            | 2.375 |     | 3.6 | V     |
| T <sub>A</sub>   | Ambient Temperature         |            | -40   |     | 85  | °C    |

### LVC MOS/LVTTL DC Characteristics (T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.3V ±5%, V<sub>DDO</sub> = 2.5V ±5% to 3.3V ±10%)

| Symbol          | Parameter          |         | Conditions                                   | Min  | Typ | Max                  | Units |
|-----------------|--------------------|---------|--|------|-----|----------------------|-------|
| V <sub>IH</sub> | Input High Voltage | CLK_SEL |  | 2    |     | V <sub>DD</sub> +0.3 | V     |
| V <sub>IL</sub> | Input Low Voltage  | CLK_SEL |  | -0.3 |     | 0.8                  |       |
| I <sub>IH</sub> | Input High Current | CLK_SEL | V <sub>IN</sub> = V <sub>DD</sub> = 3.6V     |      |     | 150                  | μA    |
| I <sub>IL</sub> | Input Low Current  | CLK_SEL | V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.6V | -5   |     |                      | μA    |

**LVPECL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ ,  $V_{DDO} = 2.5\text{V} \pm 5\%$  to  $3.3\text{V} \pm 10\%$ )

| Symbol      | Parameter                                | Conditions                               | Min   | Typ  | Max           | Units         |
|-------------|--|--|---|------|---------------|---------------|
| $I_{IH}$    | Input High Current                       | CLK0, CLK1                               | $V_{IN} = V_{DD} = 3.6\text{V}$               |      | 150           | $\mu\text{A}$ |
|             |  | /CLK0, /CLK1                             | $V_{IN} = V_{DD} = 3.6\text{V}$               |      | 150           | $\mu\text{A}$ |
| $I_{IL}$    | Input Low Current                        | CLK0, CLK1                               | $V_{DD} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ | -5   |               | $\mu\text{A}$ |
|             |  | /CLK0, /CLK1                             | $V_{DD} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ | -150 |               | $\mu\text{A}$ |
| $V_{PP}$    | Peak-to-peak Voltage                     |  | 0.3   |      | 1             | V             |
| $V_{CMR}$   | Common Mode Input Voltage <sup>(1)</sup> |  | $V_{EE}+1.5$                                  |      | $V_{DD}$      | V             |
| $V_{OH}$    | Output High Voltage <sup>(2)</sup>       | $V_{DDO} = 2.5\text{V}$ or $3.3\text{V}$ | $V_{DDO}-1.4$                                 |      | $V_{DDO}-0.9$ | V             |
| $V_{OL}$    | Output Low Voltage <sup>(2)</sup>        | $V_{DDO} = 2.5\text{V}$ or $3.3\text{V}$ | $V_{DDO}-2.0$                                 |      | $V_{DDO}-1.7$ | V             |
| $V_{SWING}$ | Peak-to-peak Output Voltage Swing        |  | 0.6   |      | 1.0           | V             |
| $I_{EE}$    | Power Supply Current                     | @ 400 MHz                                |   | 120  | 140           | mA            |

**Notes:**

- For single-ended applications, the maximum input voltage for CLK and /CLK is  $V_{DD}+0.3\text{V}$
- Outputs terminated with  $50\Omega$  to  $V_{DD}-2.0\text{V}$

**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ ,  $V_{DDO} = 2.5\text{V} \pm 5\%$  to  $3.3\text{V} \pm 10\%$ )

| Symbol    | Parameter                            | Conditions  | Min | Typ | Max | Units |
|-----------|--------------------------------------|---|-----|-----|-----|-------|
| $f_{max}$ | Output Frequency                     |   |     |     | 500 | MHz   |
| $t_{pd}$  | Propagation Delay <sup>(1)</sup>     |   |     |     | 4   | ns    |
| $T_{sk}$  | Output-to-output Skew <sup>(2)</sup> |   |     | 35  | 60  | ps    |
| $t_r/t_f$ | Output Rise/Fall time                | 20% - 80%   | 150 |     | 700 | ps    |
| odc       | Output duty cycle                    | $f \leq 400\text{ MHz}$                           | 45  |     | 55  | %     |
| $J_{add}$ | Additive jitter                      | $V_{DD} = V_{DDO} = 2.5\text{V}$ or $3.3\text{V}$ |     | 75  |     | fs    |

**Notes:**

- Measured from the differential input to the differential output crossing point
- Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point

**Additive Jitter Calculation**

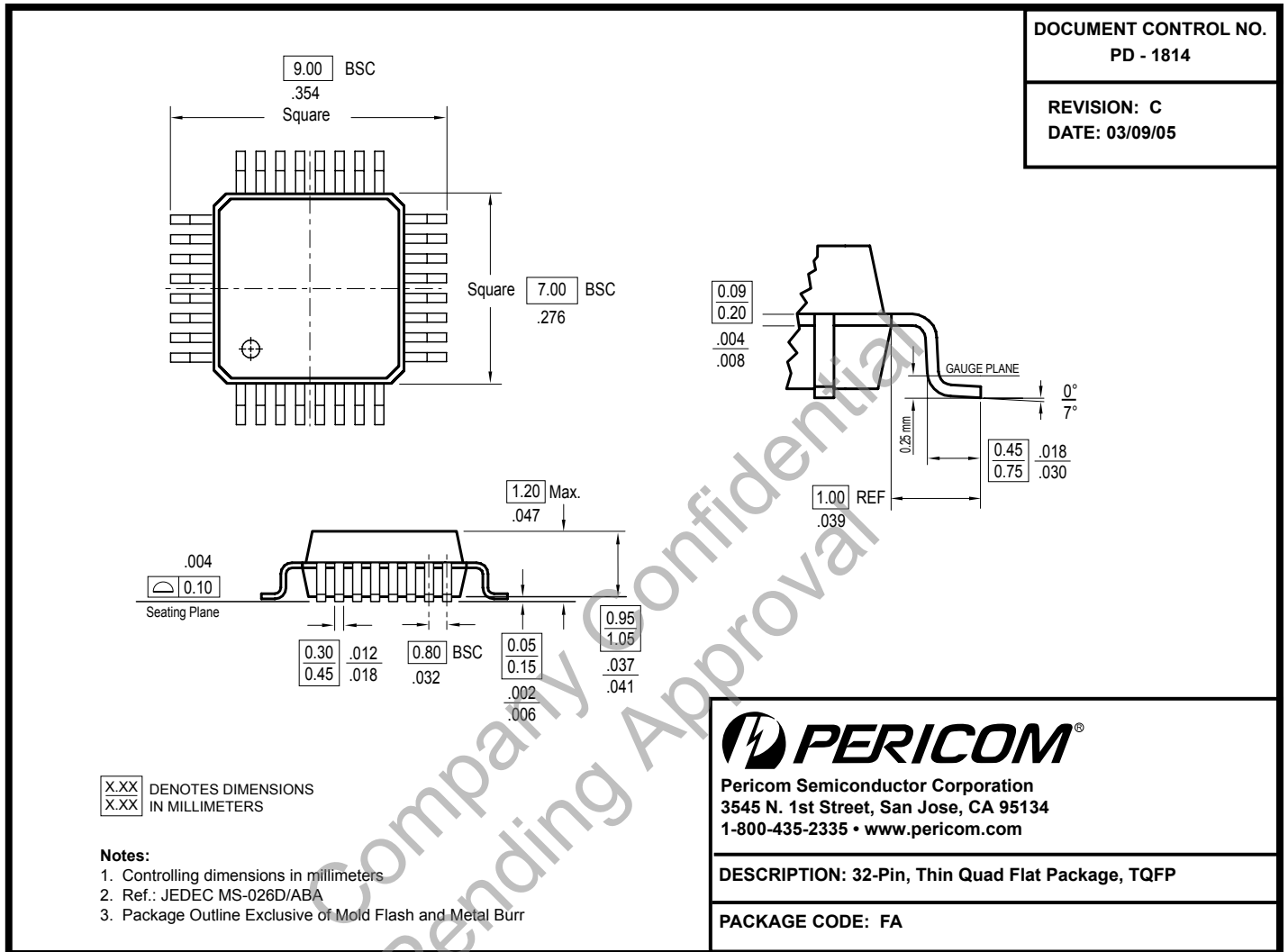
The additive jitter is measured at 12KHz to 20MHz standard noise band with the LVPECL differential input clock at 156.25MHz.

$$additive\ jitter = \sqrt{jitter\_out^2 - jitter\_in^2}$$

**Summary of Phase Jitter (Diff. Input and Diff. Output)**

|                                      | Input | Output | Additive Jitter | Unit   |
|--------------------------------------|-------|--------|-----------------|--------|
| $V_{DD} = 3.3\text{V}$ , 12kHz-20MHz | 253.7 | 259.7  | 55.5            | fs RMS |
| $V_{DD} = 2.5\text{V}$ , 12kHz-20MHz | 186.6 | 201.3  | 75.5            | fs RMS |

**Packaging Mechanical: 32-pin TQFP (FA)**



**Ordering Information(1,2,3)**

| Ordering Code  | Package Code | Package Description          |
|----------------|--------------|------------------------------|
| PI6C4853111FAE | FA           | Pb-free & Green, 32-pin TQFP |