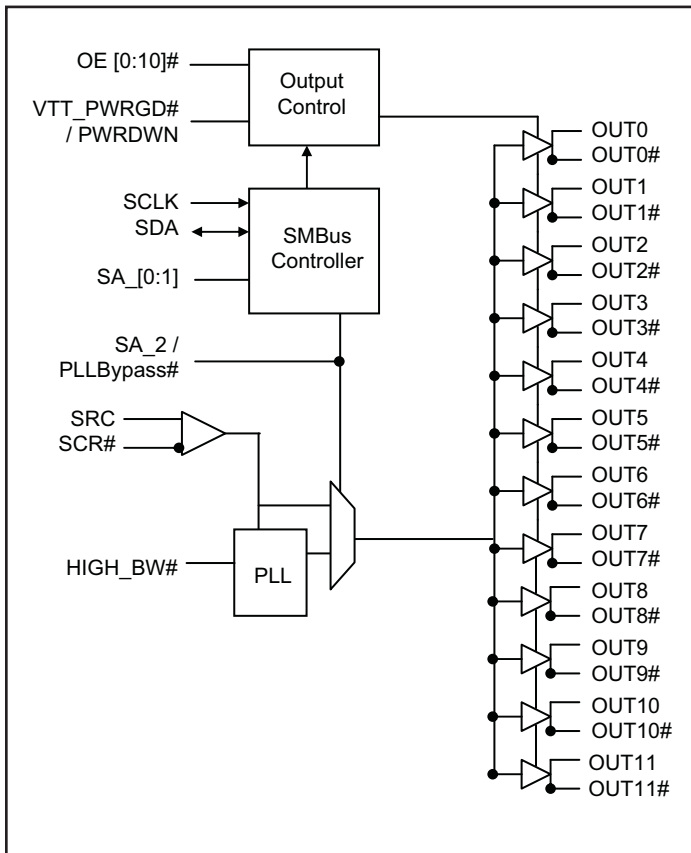
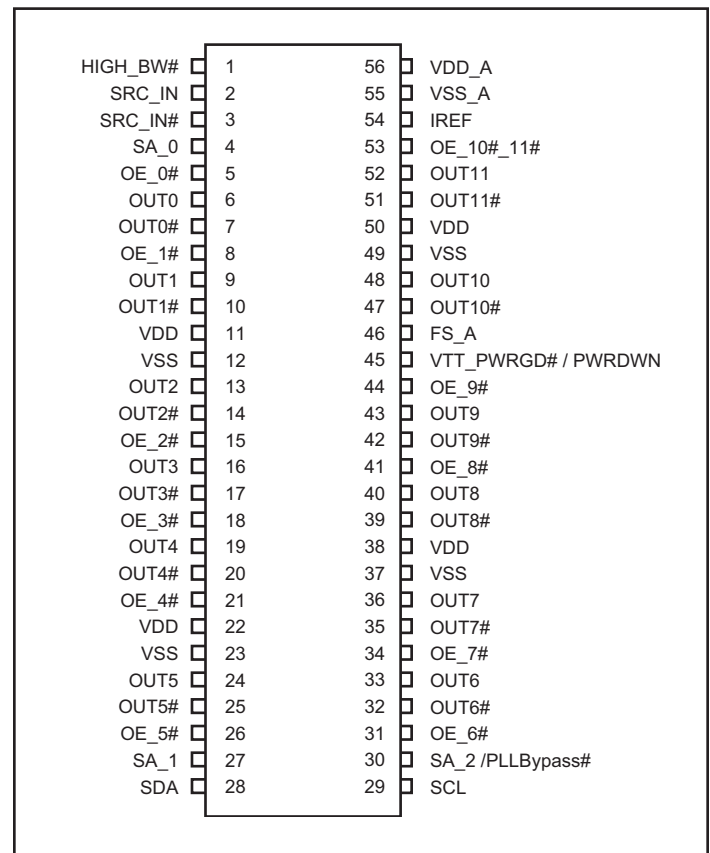


1:12 Clock Driver for Intel PCIe® Chipsets
Features

- Twelve Pairs of PCIe® Differential Clocks (HCSL compatible signaling)
- Low skew < 50ps
- Low jitter < 50ps
- Output Enable for all outputs
- Outputs tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or Fan out operation
- Gear Ratio supporting different output frequencies
- 3.3V Operation
- 56-pin Package (Pb-Free & Green):
 - TSSOP (A56)

Description

PI6C21200 is a high-speed, low-noise PCIe® differential clock buffer designed to be a companion with PI6C410B clock synthesizer. The device distributes twelve copies of the differential SRC clock coming from PI6C410B. The output frequency can be ratioed to offer a derivative frequency from the input frequency. Each differential output is controlled by individual OE pin, except OUT10 and OUT11 are sharing one OE_10#_11# pin. The clock outputs are controlled by input selection of SA_0, SA_1, SA_2 via SMBus, SCLK and SDA.

Block Diagram

Pinout Diagram


Pin Descriptions

| Pin Name | Type | Pin Number | Descriptions |
|--------------------------|--------|---|--|
| PLL_BW# | Input | 1 | 3.3V LVTTL input for selecting the PLL bandwidth. (High = Low BW) |
| SRC & SRC# | Input | 2, 3 | 0.7V Differential SRC input from PI6C410B clock synthesizer |
| OUT[0:9] & OUT[0:9]# | Output | 6, 7, 9, 10, 13, 14, 16, 17, 19, 20, 24, 25, 32, 33, 35, 36, 39, 40, 42, 43 | 0.7V Differential outputs, geared to the ratio of input clock. Can be configured to be 1:1 ratio. |
| OUT[10:11] & OUT[10:11]# | Output | 47, 48, 51, 52 | 0.7V Differential outputs, geared to the ratio of input clock same as OUT[0:9]. Can be configured to be 1:1 ratio. |
| OE_[0:9]# | Input | 5, 8, 15, 18, 21, 26, 31, 34, 41, 44 | 3.3V LVTTL input for enabling outputs, active low. Control each OUT[0:9] pair. |
| OE_10#_11# | Input | 53 | 3.3V LVTTL input for enabling outputs, active low. Control each OUT[10:11] pair. |
| SA_[0:1] | Input | 4, 27 | 3.3V LVTTL input for selecting the SMBus address |
| SA_2 / PLL-BYPASS# | Input | 30 | 3.3V LVTTL input for selecting fan-out of PLL operation, and SMBus address. 0 = PLL Bypass, 1 = PLL mode |
| SCLK | Input | 29 | SMBus compatible SCLOCK input |
| SDA | I/O | 28 | SMBus compatible SDATA |
| IREF | Input | 54 | External resistor connection to set the differential output current |
| FS_A | Input | 46 | 3.3V LVTTL inputs for CPU frequency selection 0 = above 200 MHz, 1 = below 200 MHz |
| VTT_PWRGD# / PWRDWN | Input | 45 | 3.3V LVTTL input for Power Down operation, active high |
| VDD | Power | 11, 22, 38, 50 | 3.3V Power Supply for Outputs |
| VSS | Ground | 12, 23, 37, 49 | Ground for Outputs |
| VSS_A | Ground | 55 | Ground for PLL |
| VDD_A | Power | 56 | 3.3V Power Supply for PLL |

Serial Data Interface (SMBus)

PI6C21200 is a slave only SMBus device that supports random byte read and write indexed block read and write protocol using a single 7-bit address and read/write bit as shown below.

SMBus Address Selection by SA_[0:2]

| SA_2/ PLLBypass# | SA_1 | SA_0 | SMBus Address | PLL Mode |
|---------------------|------|------|------------------|-------------|
| 0 | 0 | 0 | D0 | Bypass |
| 0 | 0 | 1 | D2 | Bypass |
| 0 | 1 | 0 | D4 | Bypass |
| 0 | 1 | 1 | D6 | Bypass |
| 1 | 0 | 0 | D8 | PLL |
| 1 | 0 | 1 | DA | PLL |
| 1 | 1 | 0 | DC | PLL |
| 1 | 1 | 1 | DE | PLL |

Indexed Block Read and Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|---|---------------------|---|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 Bits '00000000' Stand for block operation | 11:18 | Command Code - 8 Bits '00000000' Stand for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count from master - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29:36 | Data byte 0 from master - 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 1 from master - 8 bits | 30:37 | Byte count from slave - 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge from host |
| | Data bytes from master/Acknowledge | 39:46 | Data byte 0 from slave - 8 bits |
| | Data byte N - 8 bits | 47 | Acknowledge from host |
| | Acknowledge from slave | 48:55 | Data byte 1 from slave - 8 bits |
| | Stop | 56 | Acknowledge from host |
| | | | Data bytes from slave/Acknowledge |
| | | | Data byte N from slave - 8 bits |
| | | | Acknowledge from host - 38 bits |
| | | | Stop |

Random Byte Read and Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|--|--------------------|--|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write = 0 | 9 | Write - 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed. | 11:18 | Command Code - 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed. |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master - 8 bits | 20:27 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave - 8 bits |
| | | 38 | Acknowledge from master - 38 bits |
| | | 39 | Stop |

Data Byte 0: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|--|------|------------------------------------|----------------------------|
| 0 | FSB Gear Ratio SMBus | RW | 1 | |
| 1 | FSB Gear Ratio SMBus | RW | Depends on FS_A pin ⁽¹⁾ | |
| 2 | FSB Gear Ratio SMBus | RW | 0 | |
| 3 | FSB Gear Ratio SMBus | RW | Depends on FS_A pin ⁽¹⁾ | |
| 4 | FS_A PI6C410B latched input | RW | Latch | |
| 5 | Reserved | RW | 1 | |
| 6 | Group of 2 gear ratio select 1 = 1:1, 0 = Gear Raito | RW | 1 | OUT[10:11], OUT[10:11]# |
| 7 | Group of 10 gear ratio select 1 = 1:1, 0 = Gear Raito | RW | 1 | OUT[0:9], OUT[0:9]# |

Note:

1. When FS_A = 1, Bit 1 = 0 and Bit 3 = 1; When FS_A = 0, Bit 1 = 1 and Bit 3 = 0

Data Byte 1: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---|------|--------------------|--------------------|
| 0 | OUTPUTS enable 1 = Enabled 0 = Hi-Z | RW | 1 = Enabled | OUT0, OUT0# |
| 1 | | RW | 1 = Enabled | OUT1, OUT1# |
| 2 | | RW | 1 = Enabled | OUT2, OUT2# |
| 3 | | RW | 1 = Enabled | OUT3, OUT3# |
| 4 | | RW | 1 = Enabled | OUT4, OUT4# |
| 5 | | RW | 1 = Enabled | OUT5, OUT5# |
| 6 | | RW | 1 = Enabled | OUT6, OUT6# |
| 7 | | RW | 1 = Enabled | OUT7, OUT7# |

Data Byte 2: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---|------|--------------------|-----------------------|
| 0 | OUTPUTS enable 1 = Enabled 0 = Hi-Z | RW | 1 = Enabled | OUT8, OUT8# |
| 1 | | RW | 1 = Enabled | OUT9, OUT9# |
| 2 | | RW | 1 = Enabled | OUT10, OUT10# |
| 3 | | RW | 1 = Enabled | OUT11, OUT11# |
| 4 | Reserved | RW | | |
| 5 | PLL/BYPASS# 0 = Fanout, 1 = PLL | RW | 1 = PLL | OUT[0:11], OUT[0:11]# |
| 6 | PLL Bandwidth 0 = High Bandwidth, 1 = Low Bandwidth | RW | 1 = Low | OUT[0:11], OUT[0:11]# |
| 7 | Outputs current select at PWRDWN = 1 1 = 2 x I _{REF} , 0 = HiZ | RW | 1 | |

Data Byte 3: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---------------------------------------|------|-------------------------|--------------------|
| 0 | OE_0#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT0, OUT0# |
| 1 | OE_1#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT1, OUT1# |
| 2 | OE_2#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT2, OUT2# |
| 3 | OE_3#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT3, OUT3# |
| 4 | OE_4#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT4, OUT4# |
| 5 | OE_5#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT5, OUT5# |
| 6 | OE_6#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT6, OUT6# |
| 7 | OE_7#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin | OUT7, OUT7# |

Data Byte 4: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---|------|-------------------------------------|----------------------------|
| 0 | OE_8#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin at power up | OUT8, OUT8# |
| 1 | OE_9#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin at power up | OUT9, OUT9# |
| 2 | OE_10#_11#, 1 = Disable (Hi-Z), 0 = Enable | R | Depends on state of pin at power up | OUT[10:11], OUT[10:11]# |
| 3 | Reserved | R | | |
| 4 | Reserved | R | | |
| 5 | Readback – PLLBypass input | R | Latch value of pin at power up | |
| 6 | Readback – HIGH_BW# input | R | Latch value of pin at power up | |
| 7 | Readback – FS_A input | R | Latch value of pin at power up | |

Data Byte 5: Pericom ID Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---------------|------|--------------------|--------------------|
| 0 | Pericom ID | R | 0 | NA |
| 1 | | R | 0 | NA |
| 2 | | R | 0 | NA |
| 3 | | R | 0 | NA |
| 4 | Revision Code | R | 0 | NA |
| 5 | | R | 0 | NA |
| 6 | | R | 0 | NA |
| 7 | | R | 0 | NA |

Data Byte 6: Device ID Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|--------------|------|--------------------|--------------------|
| 0 | Device ID 0 | R | 0 | NA |
| 1 | Device ID 1 | R | 0 | NA |
| 2 | Device ID 2 | R | 1 | NA |
| 3 | Device ID 3 | R | 1 | NA |
| 4 | Device ID 4 | R | 0 | NA |
| 5 | Device ID 5 | R | 0 | NA |
| 6 | Device ID 6 | R | 0 | NA |
| 7 | Device ID 7 | R | 0 | NA |

Data Byte 7: Byte Counter Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected |
|-----|---|------|--------------------|--------------------|
| 0 | BC0 - Writing to the register configures how many bytes will be read back | RW | 1 | NA |
| 1 | BC1 - Writing to the register configures how many bytes will be read back | RW | 1 | NA |
| 2 | BC2 - Writing to the register configures how many bytes will be read back | RW | 1 | NA |
| 3 | BC3 - Writing to the register configures how many bytes will be read back | RW | 0 | NA |
| 4 | BC4 - Writing to the register configures how many bytes will be read back | RW | 0 | NA |
| 5 | BC5 - Writing to the register configures how many bytes will be read back | RW | 0 | NA |
| 6 | BC6 - Writing to the register configures how many bytes will be read back | RW | 0 | NA |
| 7 | BC7 - Writing to the register configures how many bytes will be read back | RW | 0 | NA |

Programmable Gear Ratio – Output Frequency

| FS_A | SMBus Byte 0 | | | | Input | Output | Gear Ratio | CPU Input Frequency (MHz) | | | | |
|----------|--------------|----------|----------|----------|----------|----------|--------------|---------------------------|--------------|--------------|--------------|--------------|
| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | M | N | (N/M) | 200 | 266.7 | 320 | 333.3 | 400 |
| 0 | 0 | 0 | 0 | 0 | 3 | 1 | 0.333 | NA | NA | 106.7 | 111.1 | 133.3 |
| 0 | 0 | 0 | 0 | 1 | 5 | 2 | 0.400 | NA | 106.7 | 128.0 | 133.3 | 160.0 |
| 0 | 0 | 0 | 1 | 0 | 12 | 5 | 0.417 | NA | 111.1 | 133.3 | 138.9 | 166.7 |
| 0 | 0 | 0 | 1 | 1 | 2 | 1 | 0.500 | 100.0 | 133.3 | 160.0 | 166.7 | 200.0 |
| 0 | 0 | 1 | 0 | 0 | 5 | 3 | 0.600 | 120.0 | 160.0 | 192.0 | 200.0 | 240.0 |
| 0 | 0 | 1 | 0 | 1 | 8 | 5 | 0.625 | 125.0 | 166.7 | 200.0 | 208.3 | NA |
| 0 | 0 | 1 | 1 | 0 | 3 | 2 | 0.667 | 133.3 | 177.8 | 213.3 | 222.2 | 266.7 |
| 0 | 0 | 1 | 1 | 1 | 4 | 3 | 0.750 | 150.0 | 200.0 | 240.0 | NA | NA |
| 0 | 1 | 0 | 0 | 0 | 6 | 5 | 0.833 | 166.7 | 222.2 | NA | NA | NA |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.000 | 200.0 | 266.7 | 320.0 | 333.3 | 400.0 |
| 0 | 1 | 0 | 1 | 0 | 5 | 6 | 1.200 | 240.0 | 320.0 | 384.0 | 400.0 | 480.0 |
| 0 | 1 | 0 | 1 | 1 | 4 | 5 | 1.250 | 250.0 | 333.3 | 400.0 | 416.6 | 500.0 |
| 0 | 1 | 1 | 0 | 0 | 3 | 4 | 1.333 | 266.7 | NA | NA | NA | NA |
| 0 | 1 | 1 | 0 | 1 | 2 | 3 | 1.500 | 300.0 | 400.0 | 480.0 | NA | NA |
| 0 | 1 | 1 | 1 | 0 | 3 | 5 | 1.667 | 333.3 | 444.4 | NA | NA | NA |
| 0 | 1 | 1 | 1 | 1 | 1 | 2 | 2.000 | 400.0 | NA | NA | NA | NA |

Note:

1. Line in BOLD is power-up default for FS_A = 0 for Pericom Semiconductor's PI6C410B.

Programmable Gear Ratio - Output Frequency -- Continued

| FS_A | SMBus Byte 0 | | | | Input | Output | Gear Ratio | CPU Input Frequency (MHz) | | | | |
|----------|--------------|----------|----------|----------|----------|----------|--------------|---------------------------|--------------|--------------|--------------|--------------|
| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | M | N | (N/M) | 100 | 133.3 | 160 | 166.67 | 200 |
| 1 | 0 | 0 | 0 | 0 | 3 | 1 | 0.333 | NA | NA | 53.3 | 55.6 | 66.7 |
| 1 | 0 | 0 | 0 | 1 | 5 | 2 | 0.400 | NA | 53.3 | 64.0 | 66.7 | 80.0 |
| 1 | 0 | 0 | 1 | 0 | 12 | 5 | 0.417 | NA | 55.6 | 66.7 | 69.4 | 83.3 |
| 1 | 0 | 0 | 1 | 1 | 2 | 1 | 0.500 | 50.0 | 66.7 | 80.0 | 83.3 | 100.0 |
| 1 | 0 | 1 | 0 | 0 | 5 | 3 | 0.600 | 60.0 | 80.0 | 96.0 | 100.0 | 120.0 |
| 1 | 0 | 1 | 0 | 1 | 8 | 5 | 0.625 | 62.5 | 83.3 | 100.0 | 104.2 | NA |
| 1 | 0 | 1 | 1 | 0 | 3 | 2 | 0.667 | 66.7 | 88.9 | 106.7 | 111.1 | 133.3 |
| 1 | 0 | 1 | 1 | 1 | 5 | 4 | 0.800 | 80.0 | 106.7 | 128.0 | 133.3 | 160.0 |
| 1 | 1 | 0 | 0 | 0 | 6 | 5 | 0.833 | NA | 111.1 | 133.3 | 138.9 | 166.7 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1.000 | 100.0 | 133.3 | 160.0 | 166.7 | 200.0 |
| 1 | 1 | 0 | 1 | 0 | 5 | 6 | 1.200 | 120.0 | 160.0 | 192.0 | 200.0 | 240.0 |
| 1 | 1 | 0 | 1 | 1 | 4 | 5 | 1.250 | 125.0 | 166.7 | 200.0 | 208.3 | NA |
| 1 | 1 | 1 | 0 | 0 | 3 | 4 | 1.333 | 133.3 | 177.8 | 213.3 | 222.2 | 266.7 |
| 1 | 1 | 1 | 0 | 1 | 2 | 3 | 1.500 | 150.0 | 200.2 | 240.0 | 250.0 | 300.0 |
| 1 | 1 | 1 | 1 | 0 | 3 | 5 | 1.667 | 166.7 | 222.2 | 266.7 | 277.8 | 333.3 |
| 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2.000 | 200.0 | 266.7 | 320.0 | 333.3 | 400.0 |

Note:

1. Line in BOLD is power-up default for FS_A = 0 for Pericom Semiconductor's PI6C410B.

Functionality

| VTT_PWRGD# / PWRDWN | OUT | OUT# |
|---------------------|-------------------------------|--------|
| 0 | Normal | Normal |
| 1 | 2 x I _{REF} or Float | Low |

| OE# pin | OE (SMBus bit) | OUT | OUT# |
|---------|----------------|--------|--------|
| 0 | 1 | Normal | Normal |
| 0 | 0 | Hi-Z | Hi-Z |
| 1 | 1 | Hi-Z | Hi-Z |
| 1 | 0 | Hi-Z | Hi-Z |

Power Down (PWRDWN assertion)

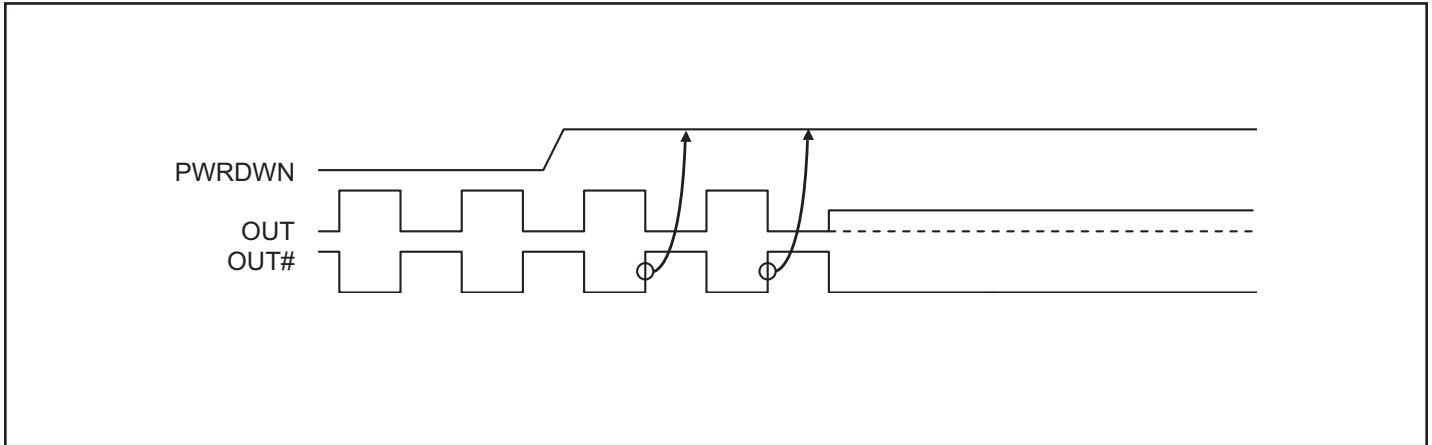


Figure 1. Power down sequence

Power Down (PWRDWN De-assertion)

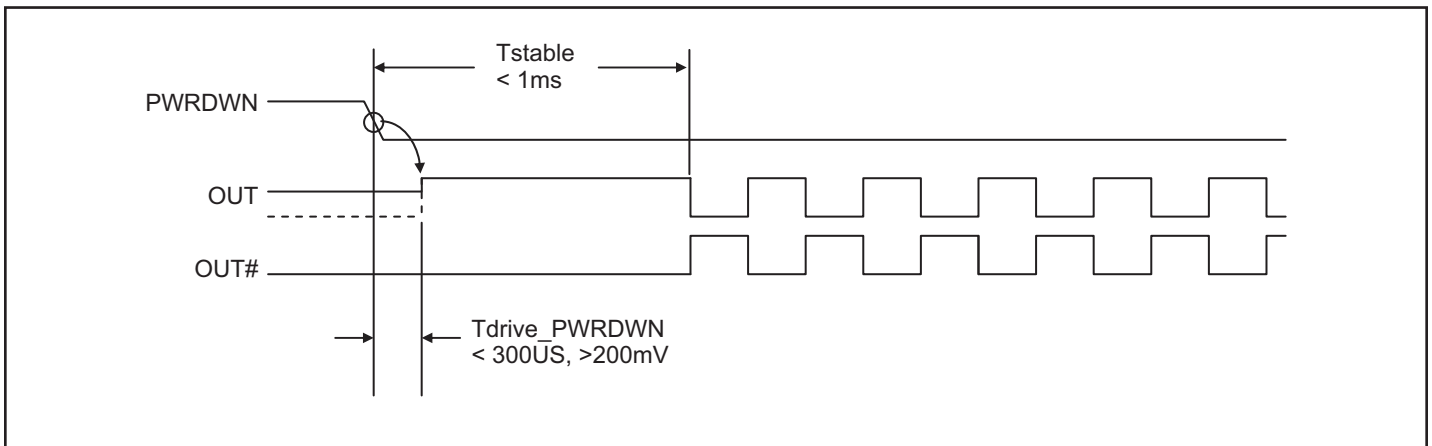
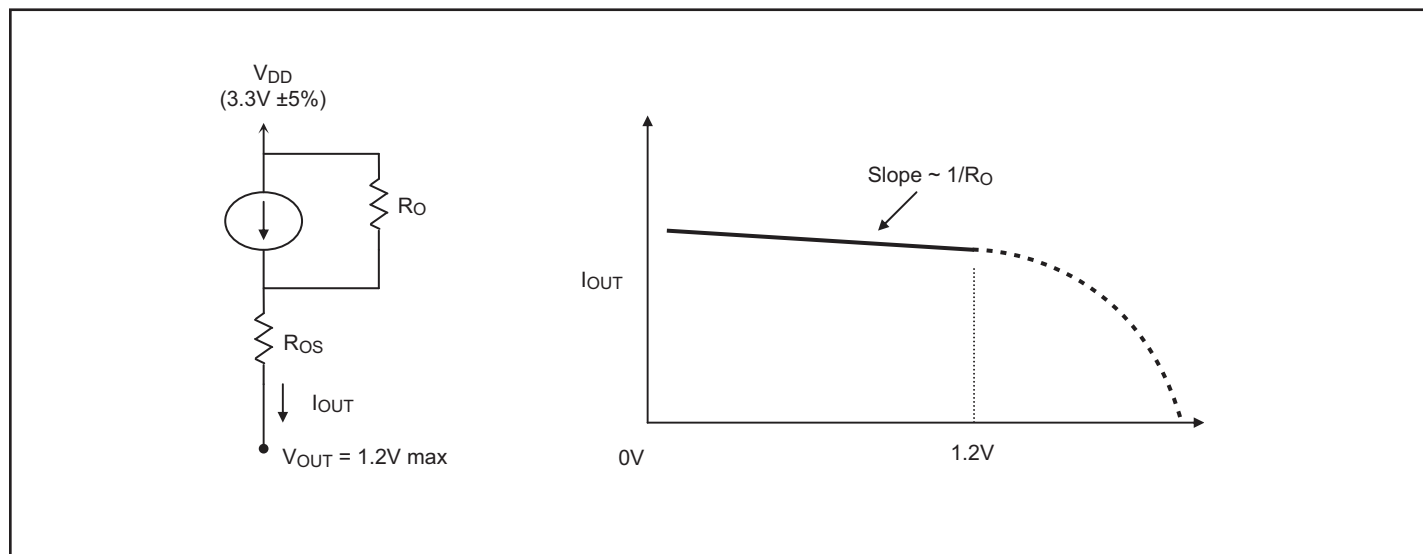


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:11], OUT[0:11]#

Figure 3. Simplified diagram of current-mode output buffer
Differential Clock Buffer Characteristics

| Symbol | Minimum | Maximum |
|-----------|---------------|-------------|
| R_O | 3000 Ω | N/A |
| R_{OS} | unspecified | unspecified |
| V_{OUT} | N/A | 850mV |

Current Accuracy

| Symbol | Conditions | Configuration | Load | Min. | Max. |
|-----------|-------------------------|---|---|--------------------|--------------------|
| I_{OUT} | $V_{DD} = 3.30 \pm 5\%$ | $R_{REF} = 475\Omega$ 1% $I_{REF} = 2.32\text{mA}$ | Nominal test load for given configuration | -12% $I_{NOMINAL}$ | +12% $I_{NOMINAL}$ |

Note:

- $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

| Board Target Trace/Term Z | Reference R, $I_{ref} = V_{DD}/(3xRr)$ | Output Current | $V_{OH} @ Z$ |
|---------------------------|--|-----------------------------|--------------|
| 100 Ω differential | $R_{REF} = 475\Omega$ 1%, $I_{REF} = 2.32\text{mA}$ | $I_{OH} = 6 \times I_{ref}$ | 0.7V @ 50 |

Absolute Maximum Ratings (Over operating free-air temperature range)

| Symbol | Parameters | Min. | Max. | Units |
|-------------------|--------------------------|------|------|-------|
| V _{DD_A} | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| V _{DD} | 3.3V I/O Supply Voltage | -0.5 | 4.6 | |
| V _{IH} | Input High Voltage | | 4.6 | |
| V _{IL} | Input Low Voltage | -0.5 | | |
| T _s | Storage Temperature | -65 | 150 | °C |
| V _{ESD} | ESD Protection | 2000 | | V |

Note:

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3 ±5%)

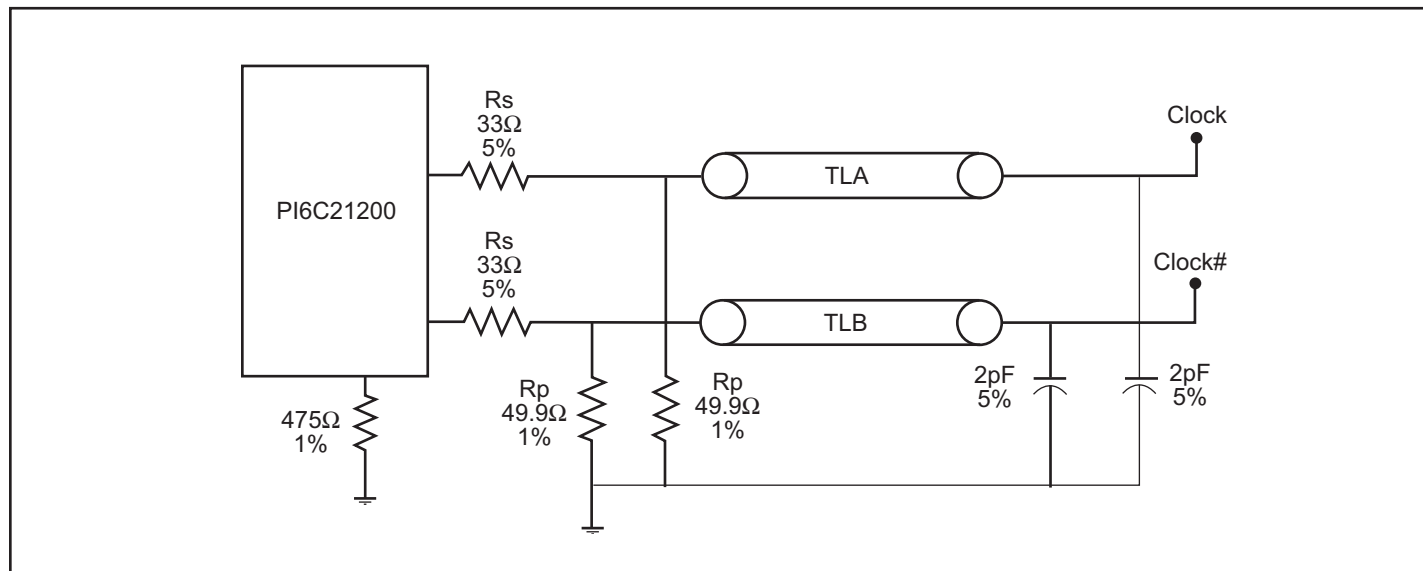
| Symbol | Parameters | Condition | Min. | Max. | Units |
|-------------------|--------------------------|---|-----------------------|-----------------------|-------|
| V _{DD_A} | 3.3V Core Supply Voltage | | 3.135 | 3.465 | V |
| V _{DD} | 3.3V I/O Supply Voltage | | 3.135 | 3.465 | |
| V _{IH} | 3.3V Input High Voltage | V _{DD} | 2.0 | V _{DD} + 0.3 | |
| V _{IL} | 3.3V Input Low Voltage | | V _{SS} - 0.3 | 0.8 | |
| I _{IK} | Input Leakage Current | 0 < V _{IN} < V _{DD} | -5 | +5 | µA |
| V _{OH} | 3.3V Output High Voltage | I _{OH} = -1mA | 2.4 | | V |
| V _{OL} | 3.3V Output Low Voltage | I _{OL} = 1mA | | 0.4 | |
| I _{OH} | Output High Current | I _{OH} = 6 × I _{REF} , I _{REF} = 2.32mA | 12.2 | 15.6 | mA |
| C _{IN} | Input Pin Capacitance | | 3 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | | 6 | |
| L _{PIN} | Pin Inductance | | | 7 | nH |
| I _{DD} | Power Supply Current | V _{DD} = 3.465V, F _{CPU} = 400 MHz | | 375 | mA |
| I _{SS} | Power Down Current | Driven outputs | | 90 | |
| I _{SS} | Power Down Current | Tristate outputs | | 24 | |
| T _A | Ambient Temperature | | 0 | 70 | °C |

AC Switching Characteristics ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

| Symbol | Parameters | Min | Max. | Units | Notes |
|-------------------------------------|--|------|-----------|-------|-------|
| T_{rise} / T_{fall} | Rise and Fall Time (measured between 0.175V to 0.525V) | 125 | 525 | ps | 3 |
| $\Delta T_{rise} / \Delta T_{fall}$ | Rise and Fall Time Variation | | 75 | | 3 |
| | Rise/Fall Matching | | 10 | % | 3 |
| T_{pd} | PLL Mode | | ± 250 | ps | |
| | Non-PLL Mode | 3 | | ns | |
| T_{skew} | Output-to-Output Skew OUT [9:0] or OUT [10:11] | | 50 | ps | 4 |
| T_{skew} | Output-to-Output Skew OUT [9:0] to OUT [10:11] | | 75 | | 4 |
| T_{jitter} | Cycle-to-Cycle Jitter | | 50 | | 4 |
| V_{HIGH} | Voltage High including overshoot | 660 | 850 | mV | 3 |
| V_{LOW} | Voltage Low including undershoot | -150 | | | 3 |
| V_{CROSS} | Absolute crossing poing voltages | 250 | 550 | | 3 |
| ΔV_{CROSS} | Total Variation of Vcross over all edges | | 100 | | 3 |
| T_{DC} | Duty Cycle | 45 | 55 | % | 4 |

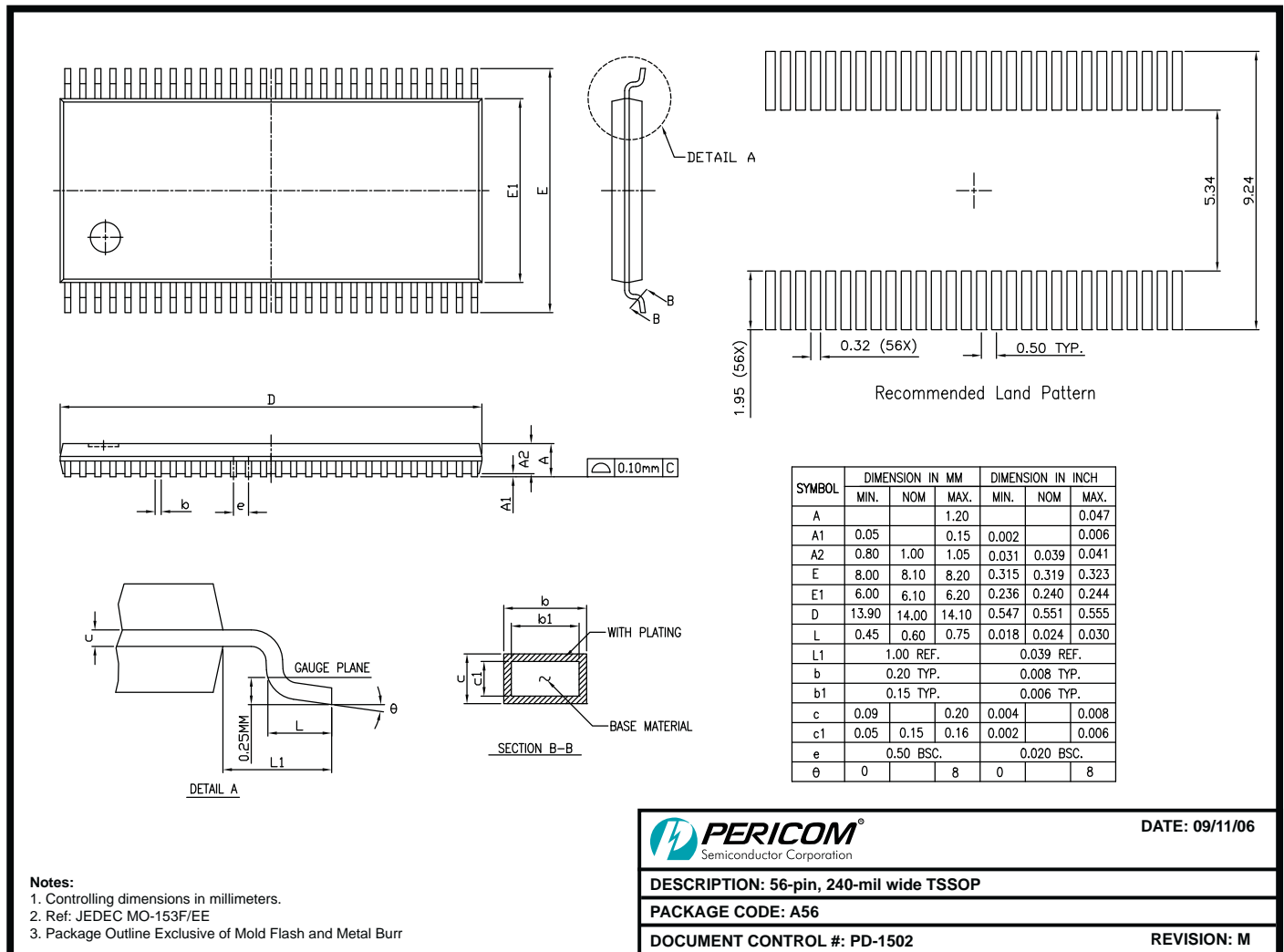
Notes:

- Measurement taken from Single Ended waveform.
- Measurement taken from Differential waveform.
- Test configuration is $R_S = 33.2\Omega$, $R_p = 49.9\Omega$, and 2pF.


Configuration Test Load Board Termination

Figure 4. Configuration test load board termination
Note:

- TLA and TLB are 3" transmission lines.

Packaging Mechanical: 56-Pin, 240-mil wide TSSOP (A)



- Notes:**
1. Controlling dimensions in millimeters.
 2. Ref: JEDEC MO-153F/EE
 3. Package Outline Exclusive of Mold Flash and Metal Burr

| | |
|--|----------------|
|  Semiconductor Corporation | DATE: 09/11/06 |
| DESCRIPTION: 56-pin, 240-mil wide TSSOP | |
| PACKAGE CODE: A56 | |
| DOCUMENT CONTROL #: PD-1502 | REVISION: M |

06-0736

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information:

| Ordering Code | Packaging Code | Package Type |
|---------------|----------------|--|
| PI6C21200AE | A | 56-Pin, 240-mil wide, 0.5mm pitch TSSOP, Pb-Free and Green |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel