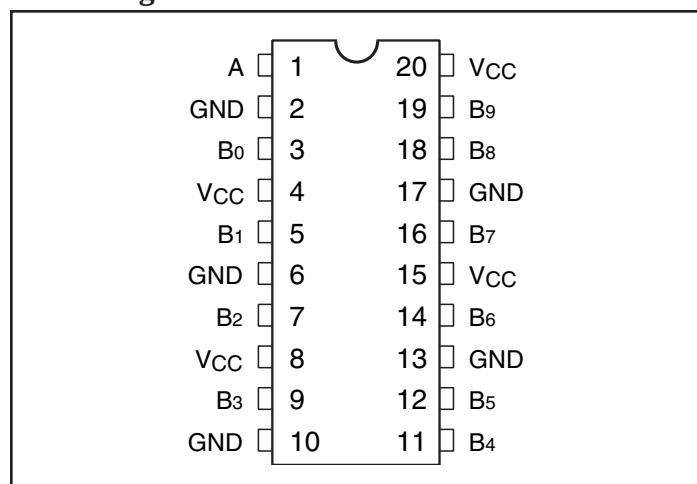


Fast CMOS Clock Driver
Features

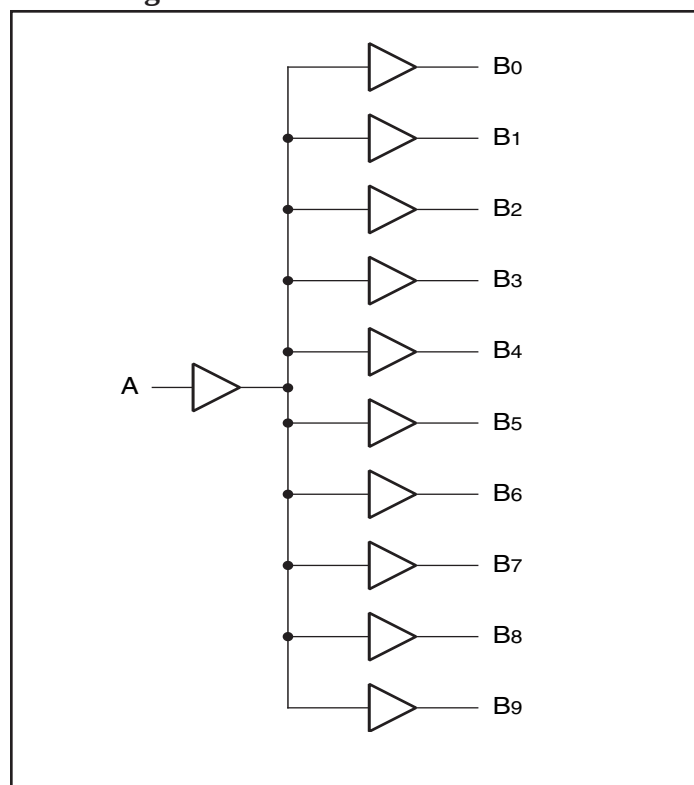
- Guaranteed low skew: 0.25ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5ns propagation delay
- TTL input and CMOS output compatible
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- Industrial Operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Packaging (Pb-free & Green available):
 - 20-pin 150-mil wide QSOP (Q)
 - 20-pin 300-mil SOIC (S)

Description

Pericom Semiconductor's PI49FCT807T clock driver feature one input and ten outputs. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

Pin Configuration

Pin Description

Pin Name	Description
A	Input
B0 - B9	Outputs
GND	Ground
VCC	Power

Block Diagram


Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)...	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current.....	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 40°C to +85°C, V_{CC} = 5.0V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min	Typ ⁽²⁾	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} =Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.3		V
V _{OL}	Output LOW Current	V _{CC} =Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48.0mA		0.2	0.5	V
			I _{OL} = 12mA			0.2	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = 2.7V			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = 0.5V			-1	μA
I _I	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC} (Max.)				20	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		-60	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND			-120		mA
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V				100	μA
V _H	Input Hysteresis				150		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6.0	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max	V _{IN} = GND or V _{CC}		3	30	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open 50% Duty Cycle, Per Output Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.4	0.6	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 50 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		20	30 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		20.7	33 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

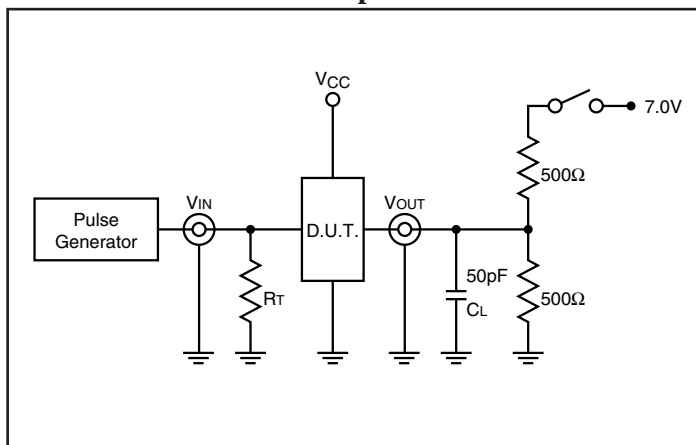
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	807/2807T		807AT		807BT		807CT		Units
			Com.		Com.		Com.		Com.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay A TO B _N	C _L = 50pF R _L = 500Ω	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	ns
tSK(o)	Skew between two outputs of same package ⁽³⁾			0.5		0.5		0.35		0.25	ns
tSK(p)	Skew between opposite tran- sitions of same output (tPHL — tPLH) ⁽³⁾			0.5		0.5		0.35		0.35	ns
tSK(t)	Skew between outputs of different package at same power supply, temperature and speed grade ⁽³⁾			1.0		1.0		0.75		0.75	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.

Tests Circuits For All Outputs⁽¹⁾



Switch Position

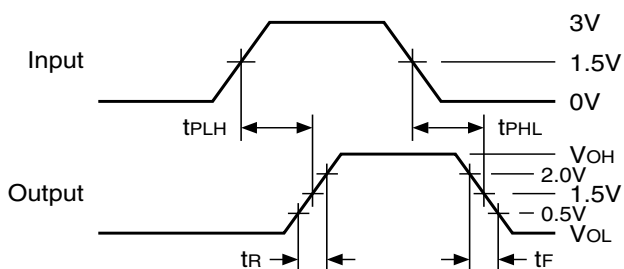
Definitions:

C_L = Load capacitance: includes jig and probe capacitance.

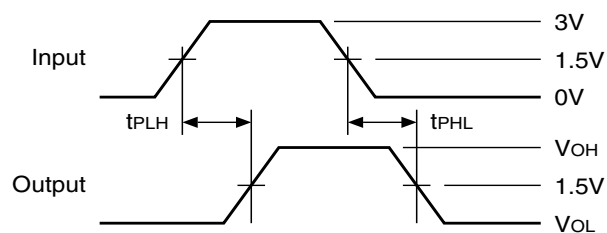
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Switching Waveforms

Propagation Delay

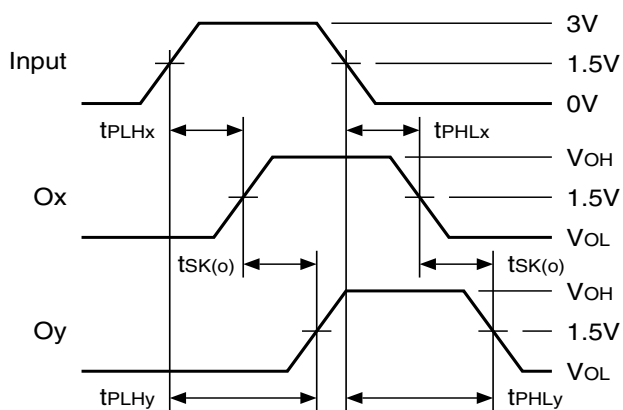


Pulse Skew – $t_{SK(p)}$



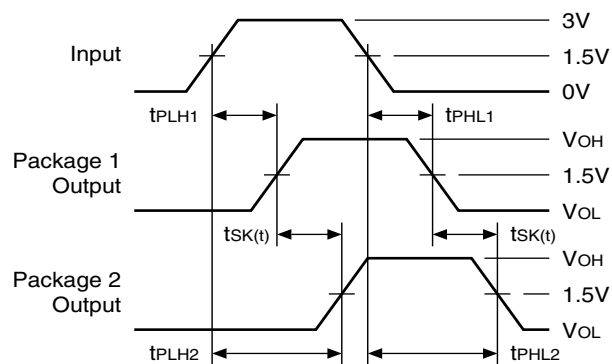
$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

Output Skew – $t_{SK(o)}$

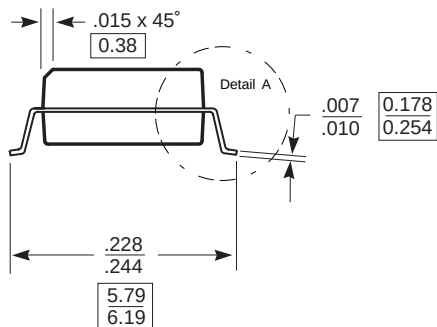
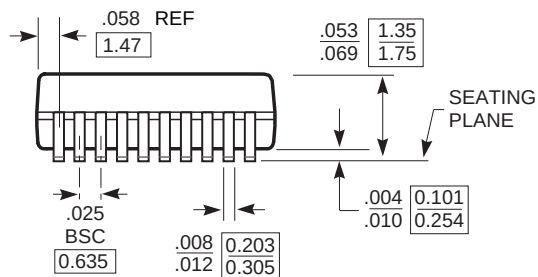
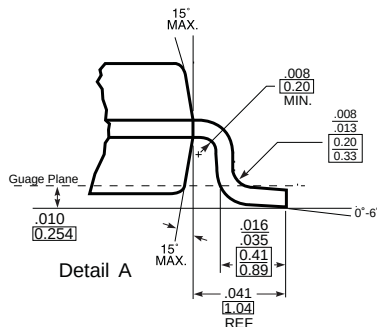
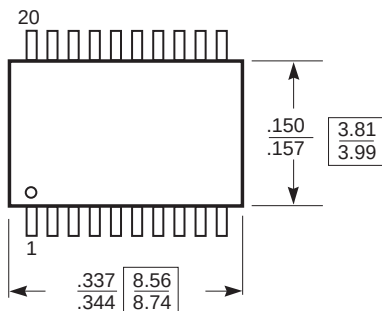


$$t_{SK(o)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Package Skew – $t_{SK(t)}$



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$



X.XX DENOTES DIMENSIONS
X.XX IN MILLIMETERS

- Note:
- 1) Controlling dimensions in inches.
 - 2) Ref: JEDEC MO-137B/AD
 - 3) Dimensions do not include mold flash, protrusions or gate burrs

DOCUMENT CONTROL NO.
PD - 1202

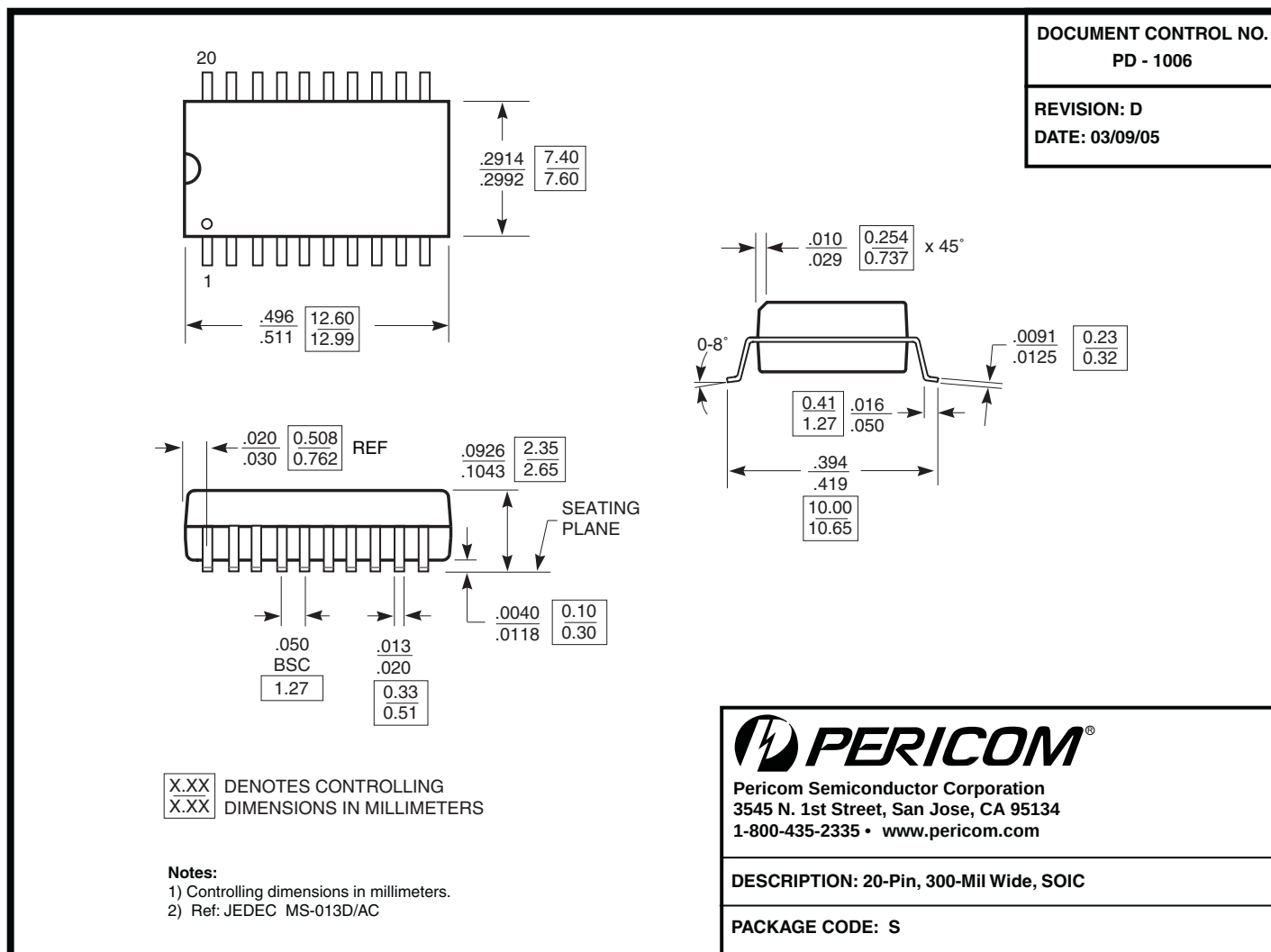
REVISION: H
DATE: 10/22/07



Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 20-Pin, 150-Mil Wide, QSOP

PACKAGE CODE: Q


Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information(1,2,3)

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT807CTQEX	Q	C	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT807CTSEX	S	C	Pb-free & Green, 20-pin 300-mil SOIC
PI49FCT807TQEX	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT807TSEX	S	Blank	Pb-free & Green, 20-pin 300-mil SOIC

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X Suffix = Tape/Reel