ArcticLink® III BX6 Solution Platform Data Sheet

Platform Highlights

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

I²C Client

- CPU interface for configuring and controlling internal registers and look-up tables (LUT).

NOTE: The MIPI interface can also be used instead of I²C.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks.

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Applications Overview

The ArcticLink III BX6 solution platform is a display interface bridge device enabling the connection of a MIPI 2-lane or MIPI 4-lane processor with a MIPI/RGB, LVDS/RGB, or MIPI/LVDS display, with up to a maximum resolution of 1920x1200 (60 fps). Featuring a small 4.5 mm x 4.5 mm package, the ArcticLink III BX6 solution platform is a low power solution designed for smartphones and tablets.

ArcticLink III BX6 Solution Platform Variants

The ArcticLink III BX6 solution platform features six distinct variants as described in **Table 1**.

Table 1: ArcticLink III BX6 Solution Platform Variants

Part Number	Device Input	Device Output	Max. Resolution[a] (60 FPS)	Primary Application
BX6B2E	MIPI-2[b]	MIPI-2[b] and RGB	1366 x 768	Smartphones and tablets with pico projectors
BX6B3E	MIPI-4[c]	MIPI-4[c] and RGB	1920 x 1200	Smartphones and tablets with pico Projectors
BX6B2G	MIPI-2[b]	LVDS-1[d] and RGB	1280 x 720	Tablets with a secondary need for HDMI/MHL encoders
BX6B3G	MIPI-4[c]	LVDS-2[e] and RGB	1920 x 1200	Tablets with a secondary need for HDMI/MHL encoders
BX6B2H	MIPI-2[b]	MIPI-2[b] and LVDS-1[e]	1280 x 720	Tablets with a secondary need for HDMI/MHL encoders
BX6B3H	MIPI-4[c]	MIPI-4[c]and LVDS-2[f]	1920 x 1200	Tablets with a secondary need for HDMI/MHL encoders

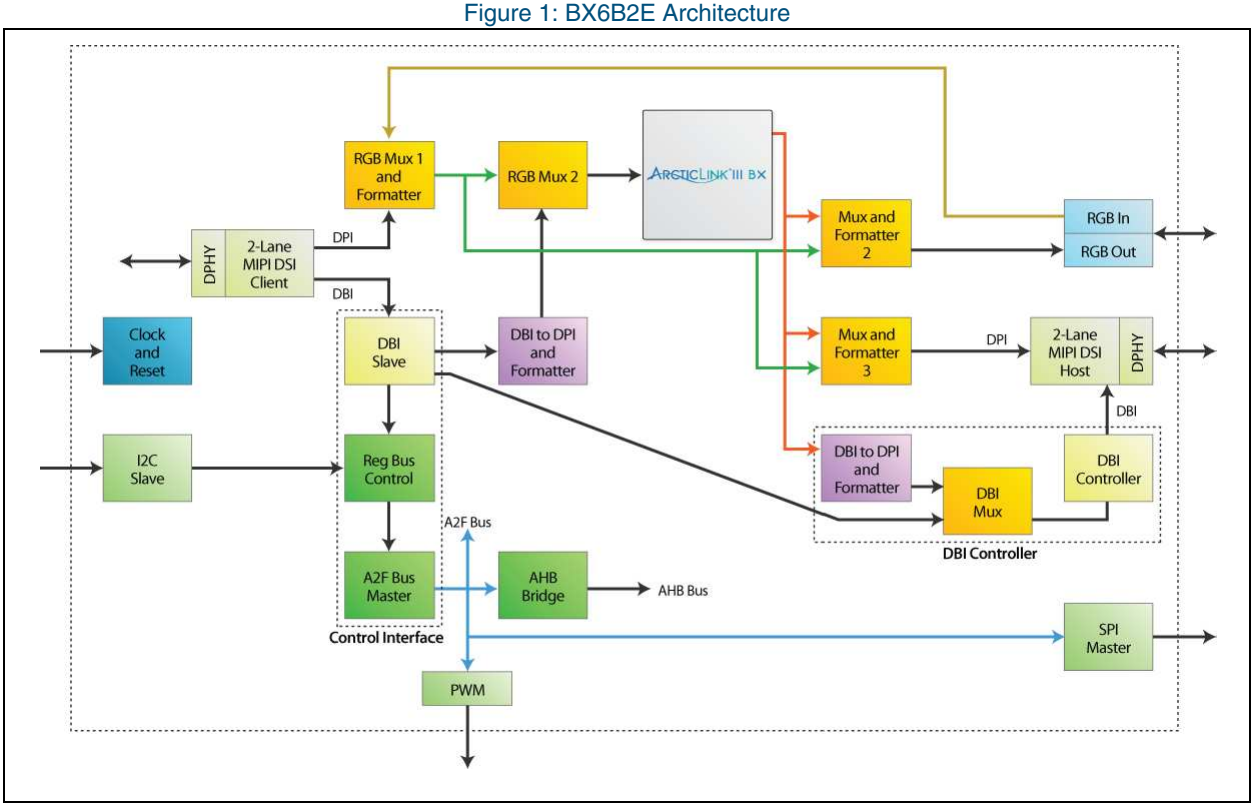
a. MIPI “video mode” only.
b. MIPI-2: Two lane MIPI.
c. MIPI-4: Four lane MIPI.
d. LVDS-1: One channel LVDS.
e. LVDS-2: Two channel LVDS

Data Paths

BX6B2E — MIPI-2 to MIPI-2 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 1: BX6B2E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and RGB

Control path input and outputs are:

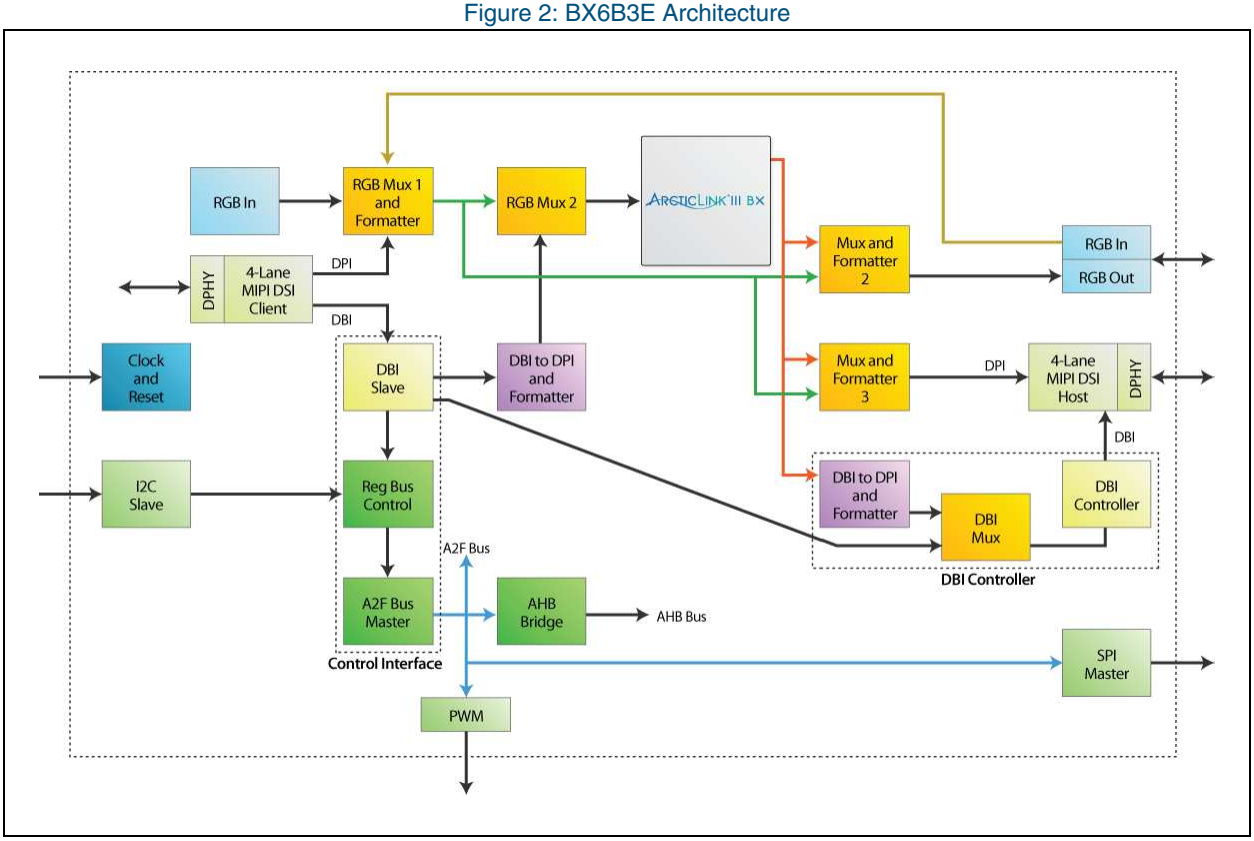
- Input – I^2C and/or MIPI DBI
- Output – SPI and/or MIPI DBI

Maximum resolution is WXGA (1366 x 768) at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B3E — MIPI-4 to MIPI-4 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 2: BX6B3E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and RGB

Control path input and outputs are:

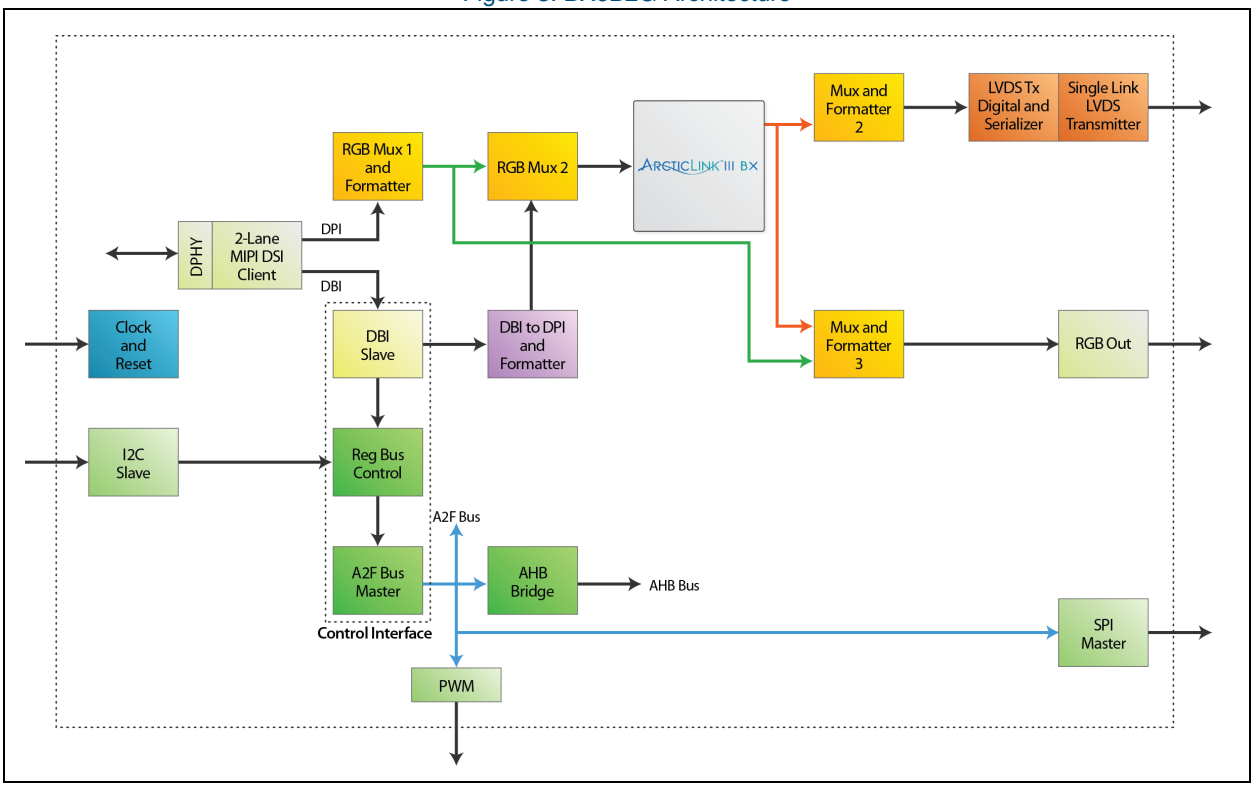
- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI and/or MIPI DBI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B2G — MIPI-2 to LVDS-1 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 3: BX6B2G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – RGB and LVDS-1

Control path input and outputs are:

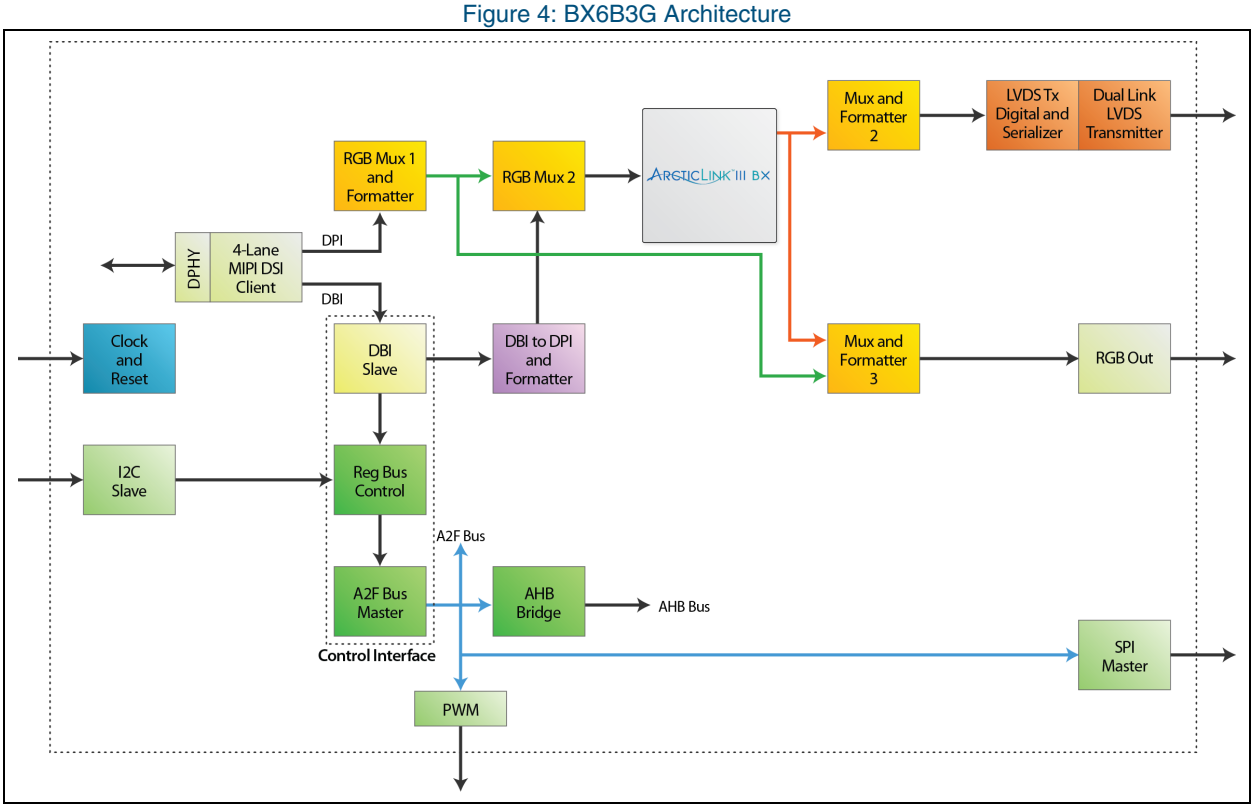
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 720 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX6B3G — MIPI-4 to LVDS-2 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 4: BX6B3G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB and LVDS-2

Control path input and outputs are:

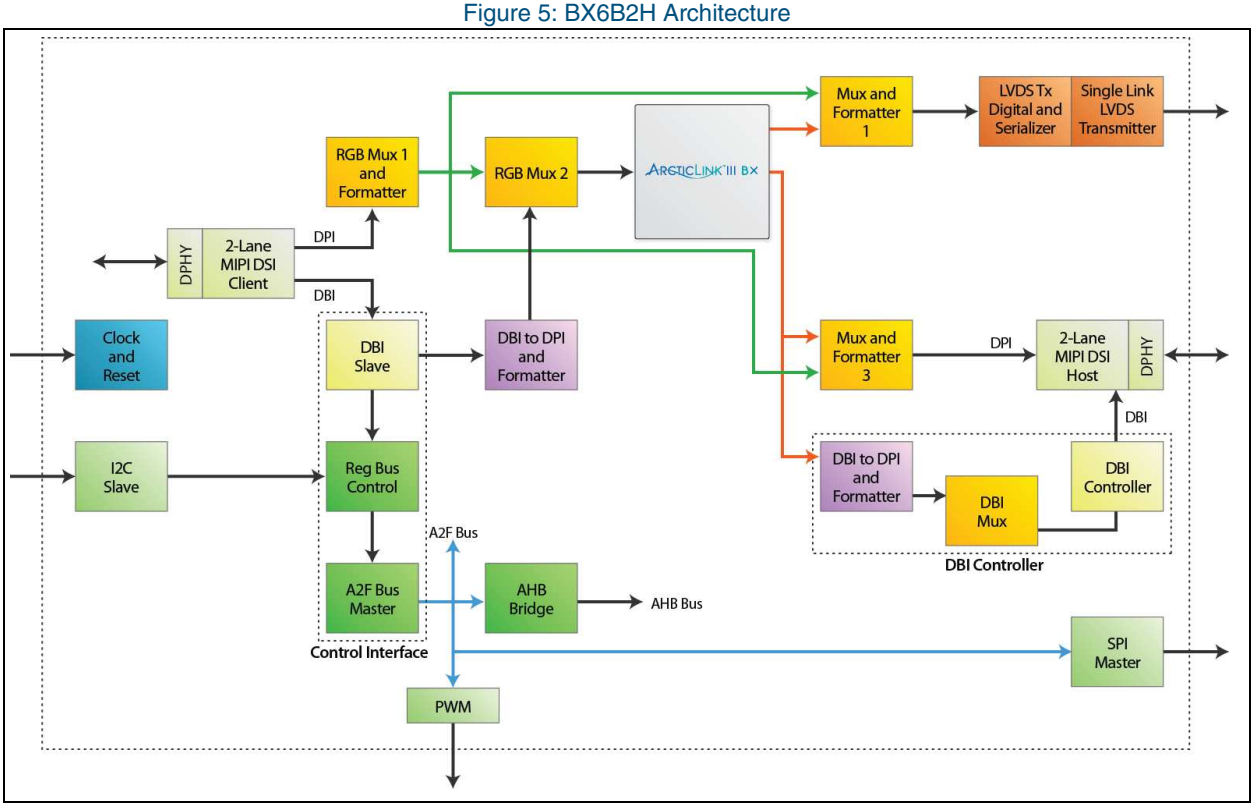
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B2H — MIPI-2 to MIPI-2 and LVDS-1

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 5: BX6B2H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and LVDS-1

Control path input and outputs are:

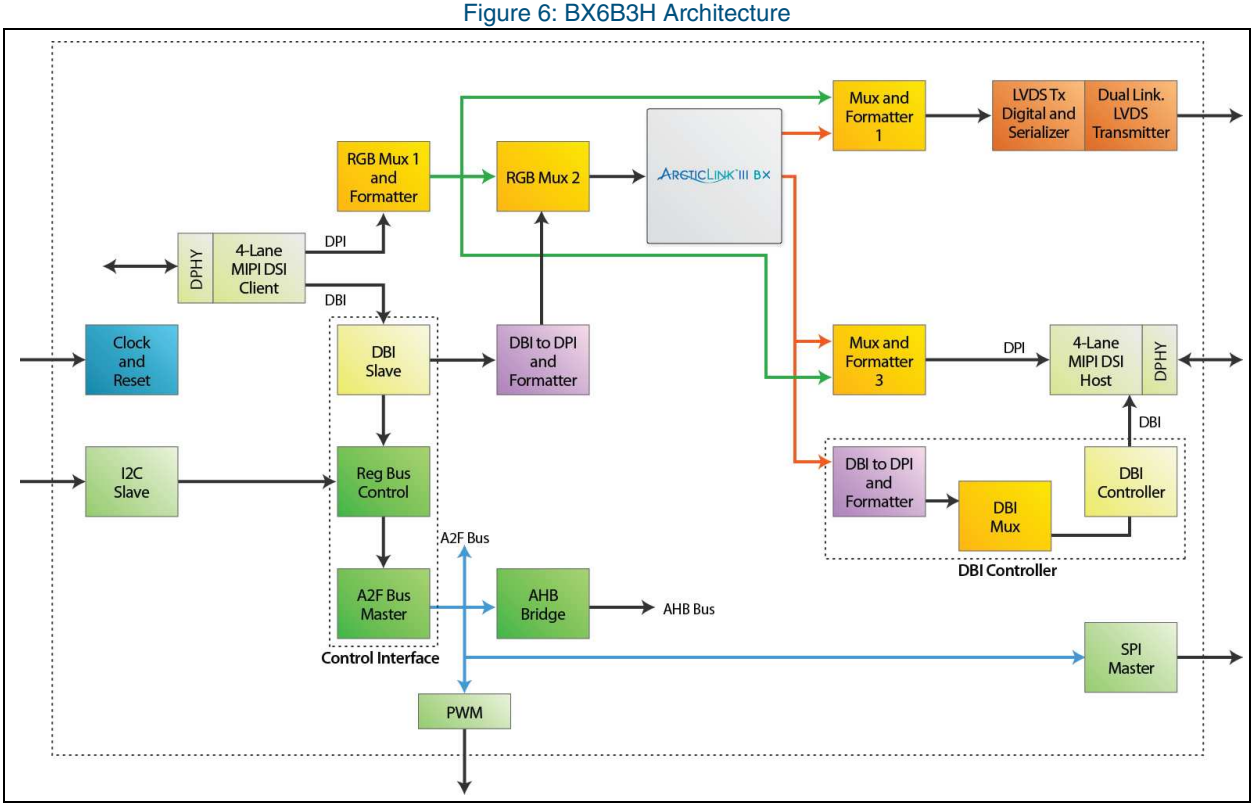
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 720 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX6B3H — MIPI-4 to MIPI-4 and LVDS-2

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 6: BX6B3H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and LVDS-2

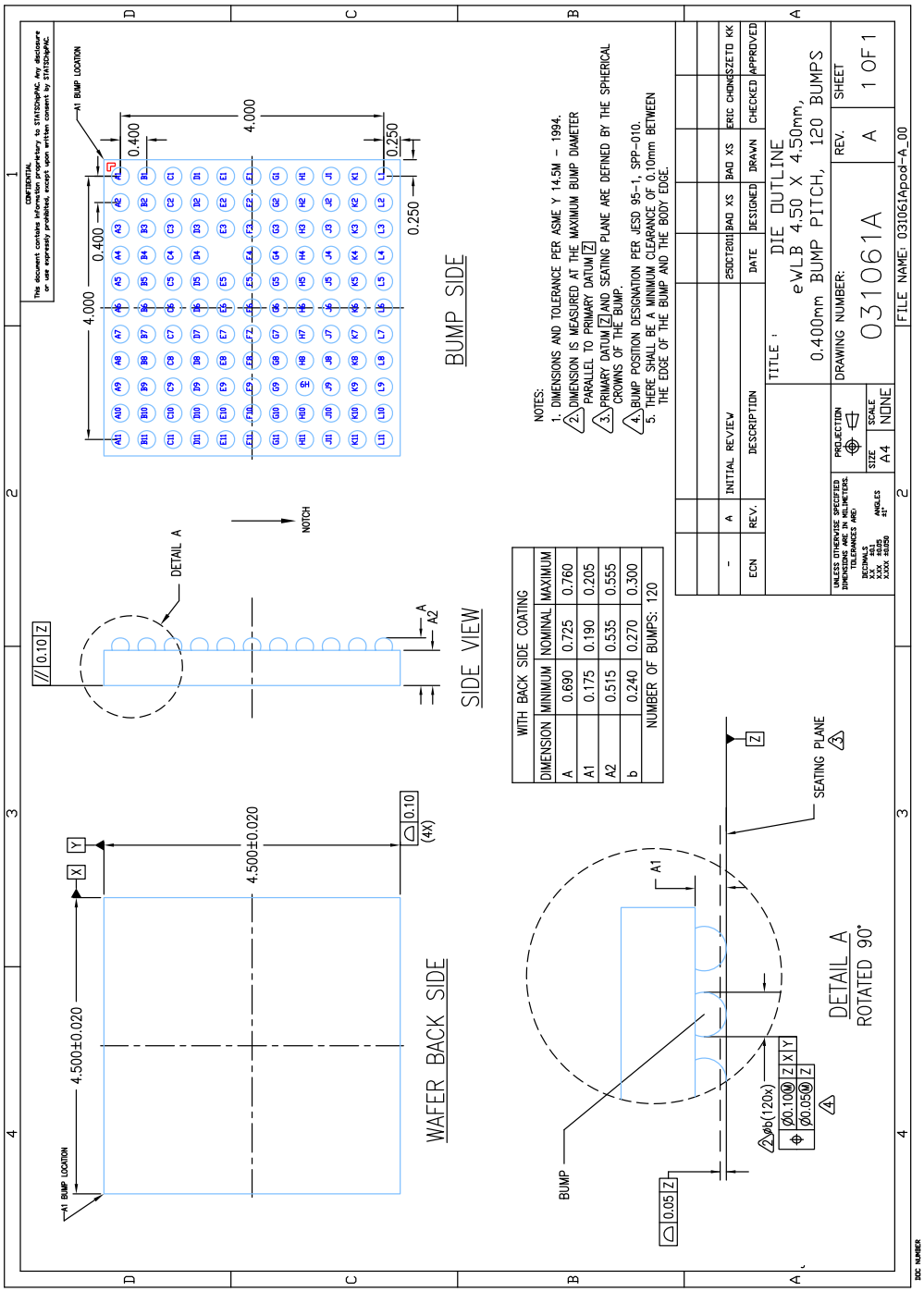
Control path input and outputs are:

- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

Mechanical Drawing

Figure 7: BX6 CSSP 120 (0.4 mm) Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release
1.1	March 2013	Paul Karazuba and Kathleen Bylsma Added packages BX6B2G, BX6B3G, BX6B2H and BX6B3H.

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