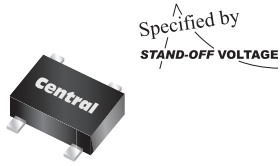


**CMYTVS5-2**

**SURFACE MOUNT SILICON  
LOW CAPACITANCE  
5 VOLT, 2-LINE  
TVS/DIODE ARRAY**



[www.centrasemi.com](http://www.centrasemi.com)



**SOT-543 CASE**

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMYTVS5-2 is a 2-line TVS/Diode array packaged in the SOT-543 surface mount case. This device, with its low capacitance, was designed to protect two high speed data or transmission lines from over-voltage transients and ESD damage.

**MARKING CODE: C52****FEATURES:**

- 15kV ESD protection
- Low capacitance
- Low clamping voltage
- Protects two I/O lines
- Protects supply voltage rail

**APPLICATIONS:**

- USB 2.0 power and data line protection
- HDMI
- DVI
- Ethernet ports

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Peak Power Dissipation (8x20 $\mu\text{s}$ )  
ESD Voltage (IEC61000-4-2, Air)  
Operating and Storage Junction Temperature

**SYMBOL**

$P_{PK}$  60  
 $V_{ESD}$  15  
 $T_J, T_{stg}$  -55 to +150

**UNITS**

W  
kV  
 $^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS PER DIODE:** ( $T_A=25^\circ\text{C}$ )

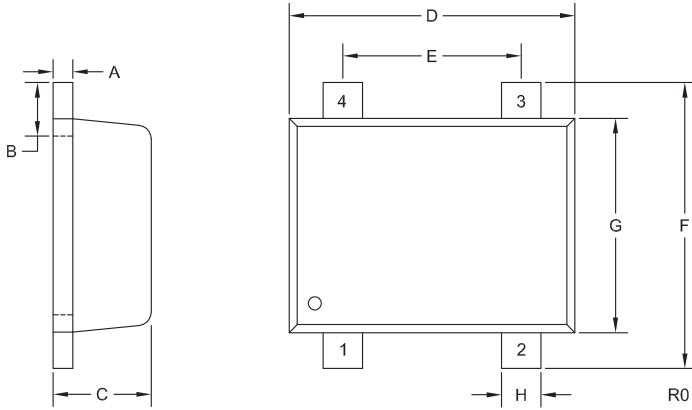
Maximum Reverse Stand-Off Voltage $V_{RWM}$	Minimum Reverse Breakdown Voltage pin 4 to pin 1 $V_Z @ I_Z$		Maximum Reverse Leakage Current pin 4 to pin 1 $I_R @ V_R$		Maximum Clamping Voltage I/O to pin 1 (8x20 $\mu\text{s}$ ) $V_C @ I_{PP}$		Maximum Clamping Voltage I/O to pin 1 (8x20 $\mu\text{s}$ ) $V_C @ I_{PP}$		Off State Junction Capacitance I/O to GND ( $V_R=0, f=1.0\text{MHz}$ ) $C_J$		Off State Junction Capacitance I/O to I/O ( $V_R=0, f=1.0\text{MHz}$ ) $C_J$	
	V	V	mA	$\mu\text{A}$	V	V	A	V	A	TYP pF	MAX pF	TYP pF
5.0	6.2	1.0	1.0	5.0	9.0	1.0	12	5.0	0.9	1.2	0.5	0.6

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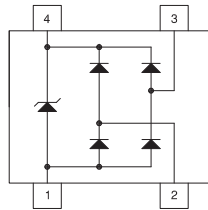
**SOT-543 CASE - MECHANICAL OUTLINE**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.002	0.007	0.07	0.17
B	0.004	0.012	0.10	0.30
C	0.019	0.024	0.50	0.60
D	0.059	0.067	1.50	1.70
E	0.035	0.044	0.90	1.10
F	0.059	0.067	1.50	1.70
G	0.044	0.052	1.10	1.30
H	0.006	0.011	0.17	0.27

SOT-543 (REV: R0)

**PIN CONFIGURATION**

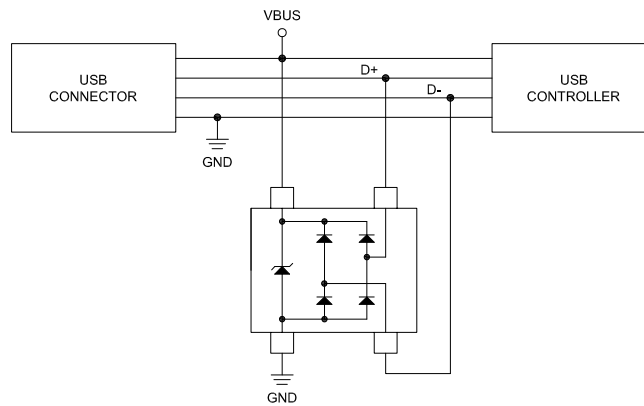


**LEAD CODE:**

- 1) Ground
- 2) I/O
- 3) I/O
- 4) Supply Voltage ( $V_{CC}$ )

**MARKING CODE: C52**

**TYPICAL APPLICATION - USB 2.0**



R1 (4-January 2013)

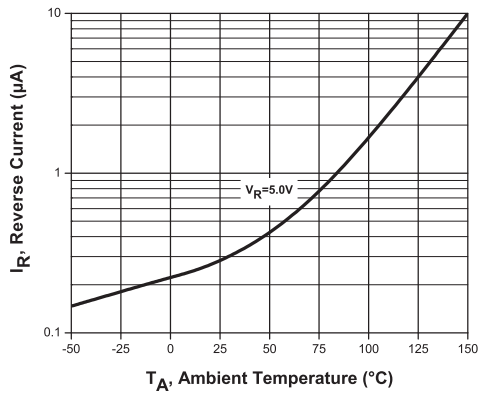
CMYTVS5-2

SURFACE MOUNT SILICON  
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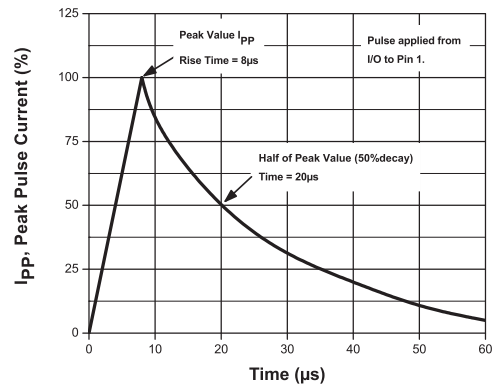


TYPICAL ELECTRICAL CHARACTERISTICS

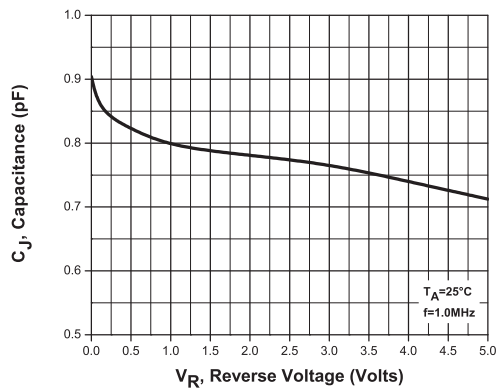
Typical Reverse Leakage Current Pin 4 to Pin 1



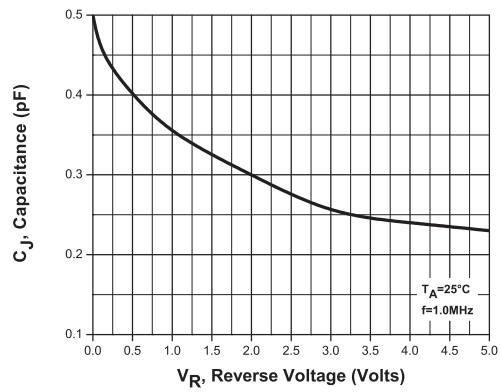
8x20 $\mu s$  Surge Current Waveform



Typical Capacitance I/O to GND



Typical Capacitance I/O to I/O



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