

CTLM8110-M832D
MULTI DISCRETE MODULE™
SURFACE MOUNT P-CHANNEL
ENHANCEMENT-MODE SILICON MOSFET
AND
LOW V_F SILICON SCHOTTKY RECTIFIER



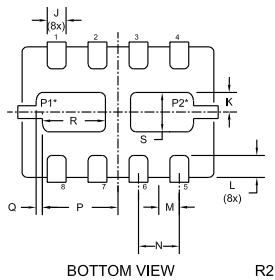
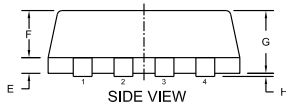
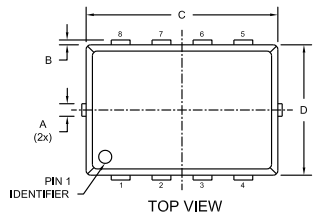
ELECTRICAL CHARACTERISTICS - Q1 - Continued: (T_A=25°C)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Q _{g(tot)}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		3.56		nC
Q _{gs}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		0.36		nC
Q _{gd}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		1.52		nC
C _{rss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		80		pF
C _{iss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		200		pF
C _{oss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		60		pF
t _{on}	V _{DD} =10V, V _{GS} =4.5V, I _D =0.95A, R _G =6.0Ω		20		ns
t _{off}	V _{DD} =10V, V _{GS} =4.5V, I _D =0.95A, R _G =6.0Ω		25		ns

ELECTRICAL CHARACTERISTICS - D1: (T_A=25°C)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _R	V _R =5.0V			10	μA
I _R	V _R =8.0V			20	μA
I _R	V _R =15V			50	μA
BV _R	I _R =100μA	40			V
V _F	I _F =10mA			0.29	V
V _F	I _F =100mA			0.36	V
V _F	I _F =500mA			0.45	V
V _F	I _F =1.0A			0.55	V
C _J	V _R =4.0V, f=1.0MHz		50		pF

TLM832D CASE - MECHANICAL OUTLINE

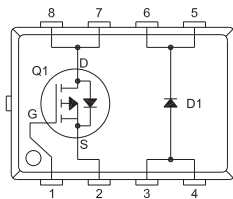


* Note:
 - Exposed pad P1 common to pins 7 and 8
 - Exposed pad P2 common to pins 5 and 6

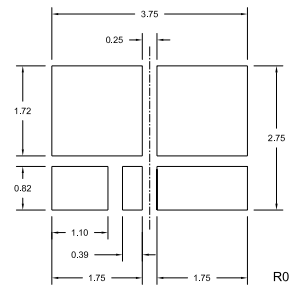
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M		0.013		0.325
N		0.026		0.650
P	0.040	0.048	1.010	1.210
Q		0.004		0.100
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

PIN CONFIGURATION



SUGGESTED MOUNTING PADS
 For Maximum Power Dissipation
 (Dimensions in mm)



For standard mounting refer to TLM832D Package Details

LEAD CODE:

- 1) Gate Q1 5) Cathode D1
- 2) Source Q1 6) Cathode D1
- 3) Anode D1 7) Drain Q1
- 4) Anode D1 8) Drain Q1

MARKING CODE: CFR

R2 (2-August 2011)