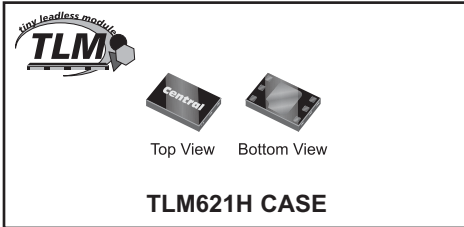


CTLDM8120-M621H

**SURFACE MOUNT
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



www.centrasemi.com



• Device is **Halogen Free** by design

APPLICATIONS:

- Load / Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS: (T_A=25°C)

Drain-Source Voltage
 Gate-Source Voltage
 Continuous Drain Current (Steady State)
 Continuous Drain Current, t≤5.0s
 Continuous Source Current (Body Diode)
 Maximum Pulsed Drain Current, tp=10μs
 Maximum Pulsed Source Current, tp=10μs
 Power Dissipation (Note 1)
 Operating and Storage Junction Temperature
 Thermal Resistance (Note 1)

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8120-M621H is a very low profile (0.4mm) P-Channel enhancement-mode MOSFET in a small, thermally efficient, 1.5mm x 2mm TLM™ package.

MARKING CODE: CNF

FEATURES:

- Low r_{DS(ON)} (0.24Ω MAX @ V_{DS}=1.8V)
- High Current (I_D=0.95A)
- Logic Level Compatible
- Small, 1.5 x 2.0 x 0.4mm Ultra Low Height Profile TLM™

SYMBOL		UNITS
V _{DS}	20	V
V _{GS}	8.0	V
I _D	860	mA
I _D	950	mA
I _S	360	mA
I _{DM}	4.0	A
I _{SM}	4.0	A
P _D	1.6	W
T _J , T _{stg}	-65 to +150	°C
θ _{JA}	75	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _{GSSF} , I _{GSSR}	V _{GS} =8.0V, V _{DS} =0		1.0	50	nA
I _{DSS}	V _{DS} =20V, V _{GS} =0		5.0	500	nA
BV _{DSS}	V _{GS} =0, I _D =250μA	20	24		V
V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.76	1.0	V
V _{SD}	V _{GS} =0, I _S =360mA			0.9	V
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.95A		85	150	mΩ
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.77A		85	142	mΩ
r _{DS(ON)}	V _{GS} =2.5V, I _D =0.67A		130	200	mΩ
r _{DS(ON)}	V _{GS} =1.8V, I _D =0.2A		190	240	mΩ
Q _{g(tot)}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		3.56		nC
Q _{gs}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		0.36		nC
Q _{gd}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		1.52		nC

Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

R2 (2-August 2011)

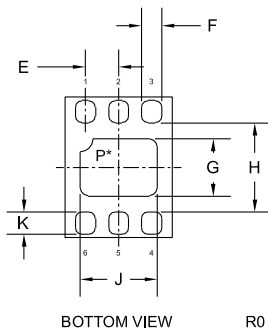
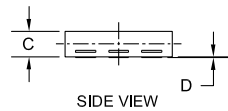
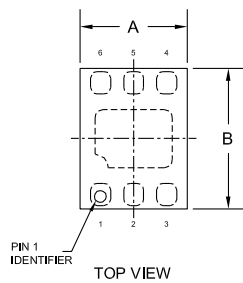
CTLDM8120-M621H
SURFACE MOUNT
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



ELECTRICAL CHARACTERISTICS - Continued: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
g_{FS}	$V_{DS}=10\text{V}, I_D=810\text{mA}$	2.0			S
C_{rSS}	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		80		pF
C_{iss}	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		200		pF
C_{oss}	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		60		pF
t_{on}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=950\text{mA}, R_G=6.0\Omega$		20		ns
t_{off}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=950\text{mA}, R_G=6.0\Omega$		25		ns

TLM621H CASE - MECHANICAL OUTLINE

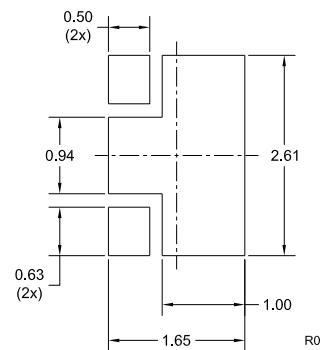


*Exposed pad P internally connected to pins 2, 3, 4, and 5.

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

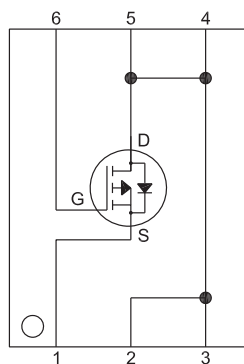
TLM621H (REV:R0)

OPTIONAL MOUNTING PADS
(Dimensions in mm)



For standard mounting refer to TLM621H Package Details

PIN CONFIGURATION



LEAD CODE:

- 1) Source
- 2) Drain
- 3) Drain
- 4) Drain
- 5) Drain
- 6) Gate

MARKING CODE: CNF

R2 (2-August 2011)