

CTLDM7003-M621

**SURFACE MOUNT
N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



Top View Bottom View

TLM621 CASE

- Device is **Halogen Free** by design

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

Drain-Source Voltage
Drain-Gate Voltage
Gate-Source Voltage
Continuous Drain Current
Maximum Pulsed Drain Current
Power Dissipation (Note 1)
Operating and Storage Junction Temperature
Thermal Resistance



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DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7003-M621 is a Silicon N-Channel Enhancement-mode MOSFET in a small, thermally efficient, TLM™ 2x1mm package.

MARKING CODE: CS

FEATURES:

- ESD Protection up to 2kV
- Low $r_{DS(ON)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small TLM™ 2x1mm Package

SYMBOL		UNITS
V_{DS}	50	V
V_{DG}	50	V
V_{GS}	12	V
I_D	280	mA
I_{DM}	1.5	A
P_D	0.9	W
T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$
θ_{JA}	139	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=5.0\text{V}$			100	nA
I_{GSSF}, I_{GSSR}	$V_{GS}=10\text{V}$			2.0	μA
I_{GSSF}, I_{GSSR}	$V_{GS}=12\text{V}$			2.0	μA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0$			50	nA
BV_{DSS}	$V_{GS}=0, I_D=10\mu\text{A}$	50			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.49		1.0	V
V_{SD}	$V_{GS}=0, I_S=115\text{mA}$			1.4	V
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=50\text{mA}$		1.6	3.0	Ω
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=50\text{mA}$		1.3	2.5	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		1.1	2.0	Ω
g_{FS}	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			mS
C_{rss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			5.0	pF
C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			50	pF
C_{oss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			25	pF

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 33mm².

R1 (17-February 2010)

CTLDM7003-M621

SURFACE MOUNT

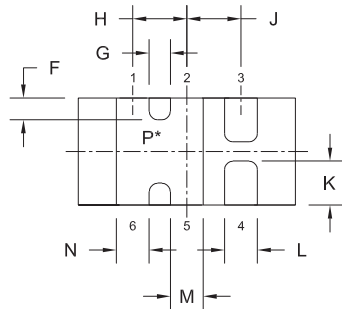
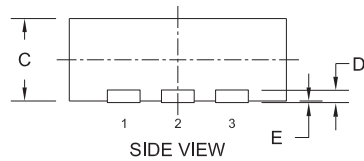
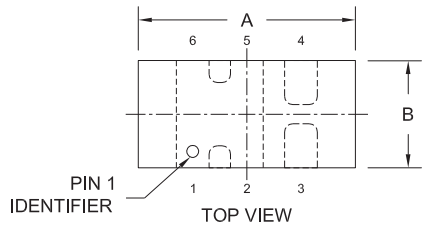
N-CHANNEL

ENHANCEMENT-MODE

SILICON MOSFET



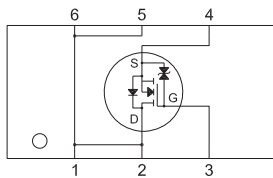
TLM621 CASE - MECHANICAL OUTLINE



R2

*Exposed pad P connects pins 1, 2, 5, and 6.

PIN CONFIGURATION

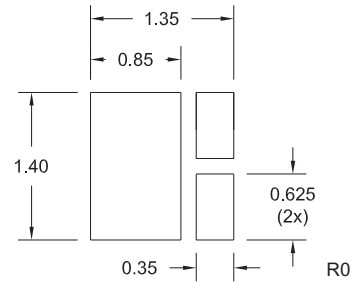


SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.073	0.085	1.850	2.150
B	0.033	0.045	0.850	1.150
C	0.028	0.031	0.700	0.800
D	0.006		0.150	
E	0.000	0.002	0.000	0.050
F	0.008		0.200	
G	0.010		0.250	
H	0.020		0.500	
J	0.020		0.500	
K	0.012	0.020	0.300	0.500
L	0.007	0.012	0.180	0.300
M	0.007	0.012	0.180	0.300
N	0.007	0.012	0.180	0.300

TLM621 (REV: R2)

SUGGESTED MOUNTING PADS

(Dimensions in mm)



LEAD CODE:

- 1) Drain
- 2) Drain
- 3) Gate
- 4) Source
- 5) Drain
- 6) Drain

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