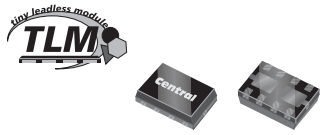
CTLDM7181-M832D

SURFACE MOUNT
N-CHANNEL AND P-CHANNEL
ENHANCEMENT-MODE
COMPLEMENTARY SILICON MOSFETS



Top View Bottom View

TLM832D CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7181-M832D is a Dual complementary N-Channel and P-Channel Enhancement-mode MOSFET, designed for high speed pulsed amplifier and driver applications. These MOSFETs offer Low $r_{DS(ON)}$ and Low Threshold Voltages.

MARKING CODE: CFK

• Device is ***Halogen Free*** by design

APPLICATIONS:

• Switching Circuits
• DC - DC Converters
• Battery powered portable devices

FEATURES:

• Dual complementary MOSFETs
• Low $r_{DS(ON)}$
• High current
• Logic level compatibility

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL	N-CH (Q1)	P-CH (Q2)	UNITS
Drain-Source Voltage	V_{DS}	20	20	V
Gate-Source Voltage	V_{GS}	8.0	8.0	V
Continuous Drain Current (Steady State)	I_D	1.0	0.86	A
Continuous Drain Current, t≤5.0s	I_D	-	0.95	A
Continuous Source Current (Body Diode)	I_S	-	0.36	A
Maximum Pulsed Drain Current, tp=10µs	I_{DM}	4.0	4.0	A
Maximum Pulsed Source Current, tp=10µs	I_{SM}	-	4.0	A
Power Dissipation (Note 1)	P_D	1.65		W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C
Thermal Resistance (Note 1)	Θ_{JA}	76		°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C)

		N-CH (Q1)			P-CH (Q2)			
SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=8.0V, V_{DS}=0	-	-	10	-	.001	.05	µA
I_{DSS}	V_{DS}=20V, V_{GS}=0	-	-	10	-	.005	0.5	µA
BV_{DSS}	V_{GS}=0, I_D=250µA	20	-	-	20	24	-	V
$V_{GS(th)}$	V_{DS}=10V, I_D=1.0mA	0.5	-	1.2	-	-	-	V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	-	-	-	0.45	0.76	1.0	V
V_{SD}	V_{GS}=0, I_S=1.0A	-	-	1.1	-	-	-	V
V_{SD}	V_{GS}=0, I_S=360mA	-	-	-	-	-	0.9	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=0.5A	-	.075	0.10	-	-	-	Ω
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=0.95A	-	-	-	-	.085	0.15	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=0.5A	-	0.10	0.14	-	-	-	Ω
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=0.77A	-	-	-	-	.085	0.142	Ω
$r_{DS(ON)}$	V_{GS}=1.5V, I_D=0.1A	-	0.17	0.25	-	-	-	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=0.67A	-	-	-	-	0.13	0.20	Ω
$r_{DS(ON)}$	V_{GS}=1.8V, I_D=0.2A	-	-	-	-	0.19	0.24	Ω
$Q_{g(tot)}$	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A	-	2.4	-	-	3.56	-	nC
Q_{gs}	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A	-	0.25	-	-	0.36	-	nC
Q_{gd}	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A	-	0.65	-	-	1.52	-	nC

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm^2.

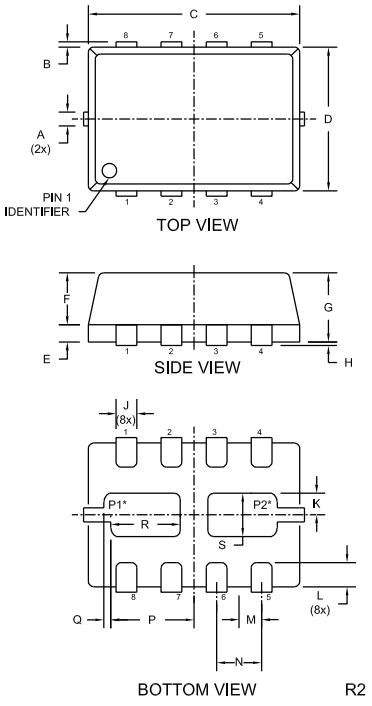
R2 (2-August 2011)

CTLDM7181-M832D

SURFACE MOUNT
N-CHANNEL AND P-CHANNEL
ENHANCEMENT-MODE
COMPLEMENTARY SILICON MOSFETS

ELECTRICAL CHARACTERISTICS - Continued:		N-CH (Q1)	P-CH (Q2)		
SYMBOL	TEST CONDITIONS	TYP	MIN	TYP	UNITS
g_{FS}	V_{DS}=10V, I_D=0.5A	4.2	-	-	S
g_{FS}	V_{DS}=10V, I_D=810mA	-	2.0	-	S
C_{rss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz	45	-	-	pF
C_{rss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz	-	-	80	pF
C_{iss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz	220	-	-	pF
C_{iss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz	-	-	200	pF
C_{oss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz	120	-	-	pF
C_{oss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz	-	-	60	pF
t_{on}	V_{DD}=10V, V_{GS}=5.0V, I_D=0.5A	25	-	-	ns
t_{on}	V_{DD}=10V, V_{GS}=4.5V, I_D=950mA, R_G=6.0Ω	-	-	20	ns
t_{off}	V_{DD}=10V, V_{GS}=5.0V, I_D=0.5A	140	-	-	ns
t_{off}	V_{DD}=10V, V_{GS}=4.5V, I_D=950mA, R_G=6.0Ω	-	-	25	ns

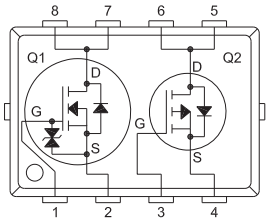
TLM832D CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

PIN CONFIGURATION



LEAD CODE:
1) Gate Q1
2) Source Q1
3) Gate Q2
4) Source Q2
5) Drain Q2
6) Drain Q2
7) Drain Q1
8) Drain Q1

MARKING CODE: CFK

* Note:
- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6

R2 (2-August 2011)