

**CMLDM7003E
CMLDM7003JE
ENHANCED SPECIFICATION**

**SURFACE MOUNT
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**

PICOmini™



**ENHANCED
E
SPECIFICATION**

SOT-563 CASE



www.centrasemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM7003E and CMLDM7003JE are Enhancement-mode N-Channel Field Effect Transistors, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003E utilizes the USA pinout configuration, while the CMLDM7003JE utilizes the Japanese pinout configuration. These special Dual Transistor devices offer low drain-source on state resistance ($r_{DS(ON)}$) and ESD protection up to 2kV.

**MARKING CODES: CMLDM7003E: C73
CMLDM7003JE: C7J**

FEATURES

- ESD protected up to 2kV

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage	
Drain-Gate Voltage	
Gate-Source Voltage	
Continuous Drain Current	
Maximum Pulsed Drain Current	
Power Dissipation (Note 1)	
Power Dissipation (Note 2)	
Power Dissipation (Note 3)	
Operating and Storage Junction Temperature	
Thermal Resistance	

SYMBOL

V_{DS}	50	V
V_{DG}	50	V
V_{GS}	12	V
I_D	280	mA
I_{DM}	1.5	A
P_D	350	mW
P_D	300	mW
P_D	150	mW
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	357	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
◆ I_{GSSF}, I_{GSSR}	$V_{GS}=5.0\text{V}$			50	nA
◆ I_{GSSF}, I_{GSSR}	$V_{GS}=10\text{V}$			0.5	μA
◆ I_{GSSF}, I_{GSSR}	$V_{GS}=12\text{V}$			1.0	μA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0$			50	nA
BV_{DSS}	$V_{GS}=0, I_D=10\mu\text{A}$	50			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.49		1.2	V
V_{SD}	$V_{GS}=0, I_S=115\text{mA}$			1.4	V
◆ $r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=50\text{mA}$		1.6	2.3	Ω
◆ $r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=50\text{mA}$		1.3	1.9	Ω
◆ $r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		1.1	1.5	Ω
g_{FS}	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			mS
C_{rss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			5.0	pF
C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			50	pF
C_{oss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			25	pF

- ◆ Enhanced specification

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm^2
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm^2
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm^2

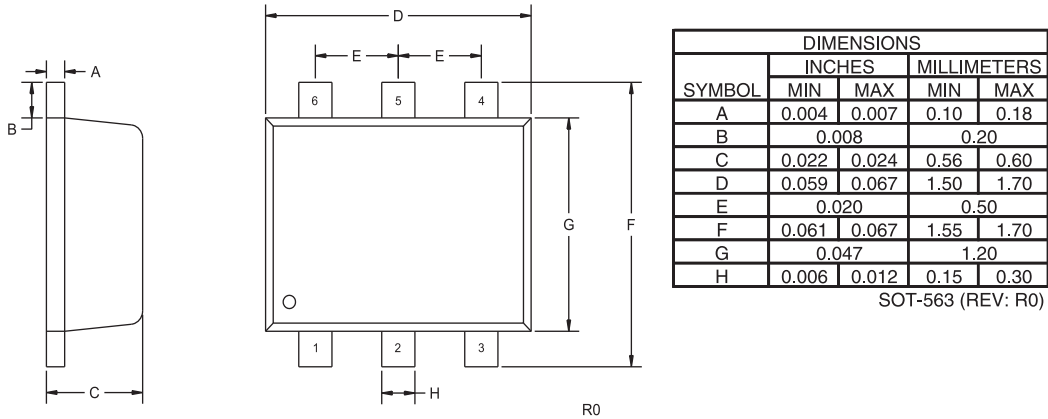
R2 (18-January 2010)

**CMLDM7003E
CMLDM7003JE
ENHANCED SPECIFICATION**

**SURFACE MOUNT
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**

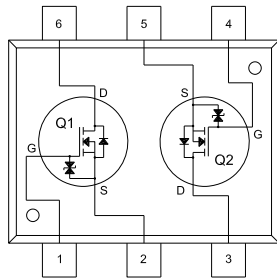


SOT-563 CASE - MECHANICAL OUTLINE



PIN CONFIGURATIONS

CMLDM7003E (USA Pinout)

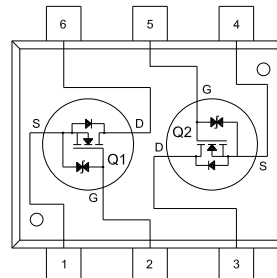


LEAD CODE:

- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

MARKING CODE: C73

CMLDM7003JE (Japanese Pinout)



LEAD CODE:

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

MARKING CODE: C7J

R2 (18-January 2010)