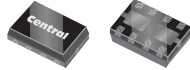


CTLT5551-M832D

**SURFACE MOUNT
DUAL, HIGH VOLTAGE
GENERAL PURPOSE
NPN SILICON TRANSISTORS**



Top View Bottom View

TLM832D CASE

- Device is **Halogen Free** by design

APPLICATIONS

- General purpose high voltage amplifier applications.

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

Collector-Base Voltage
Collector-Emitter Voltage
Emitter-Base Voltage
Continuous Collector Current
Power Dissipation (Note 1)
Operating and Storage Junction Temperature
Thermal Resistance



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DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLT5551-M832D is a Dual NPN General Purpose, High Voltage Amplifier Transistor packaged in the small, thermally efficient, 3x2mm Tiny Leadless Module (TLM™) surface mount case. These devices are designed for applications where small size, operational efficiency, and low energy consumption are the prime requirements.

MARKING CODE: CFS

FEATURES

- Dual High Voltage Transistors ($V_{CBO}=180\text{V MAX}$)
- Low Leakage Current ($I_{CBO}=50\text{nA MAX @ } V_{CB}=120\text{V}$)
- Low $V_{CE(SAT)}$ ($0.2\text{V MAX @ } I_C=50\text{mA}$)
- Small TLM 3x2mm Leadless Surface Mount Package

SYMBOL		UNITS
V_{CBO}	180	V
V_{CEO}	160	V
V_{EBO}	6.0	V
I_C	600	mA
P_D	1.65	W
T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$
θ_{JA}	76	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=120\text{V}$		50	nA
I_{CBO}	$V_{CB}=120\text{V}, T_A=100^{\circ}\text{C}$		50	μA
I_{EBO}	$V_{EB}=4.0\text{V}$		50	nA
BV_{CBO}	$I_C=100\mu\text{A}$	180		V
BV_{CEO}	$I_C=1.0\text{mA}$	160		V
BV_{EBO}	$I_E=10\mu\text{A}$	6.0		V
$V_{CE(SAT)}$	$I_C=10\text{mA}, I_B=1.0\text{mA}$		0.15	V
$V_{CE(SAT)}$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		0.20	V
$V_{BE(SAT)}$	$I_C=10\text{mA}, I_B=1.0\text{mA}$		1.00	V
$V_{BE(SAT)}$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		1.00	V
h_{FE}	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}$	80		
h_{FE}	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$	80	250	
h_{FE}	$V_{CE}=5.0\text{V}, I_C=50\text{mA}$	30		
f_T	$V_{CE}=10\text{V}, I_C=10\text{mA}, f=100\text{MHz}$	100	300	MHz

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm²

R2 (19-February 2010)

CTLT5551-M832D

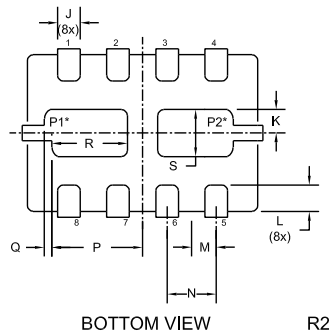
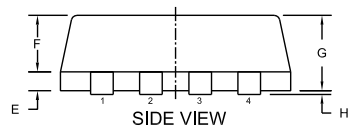
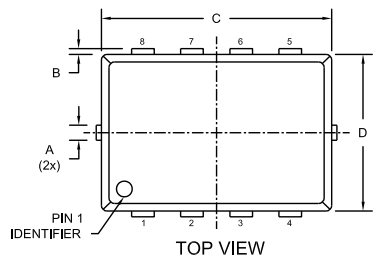
**SURFACE MOUNT
DUAL, HIGH VOLTAGE
GENERAL PURPOSE
NPN SILICON TRANSISTORS**



ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued:

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
C_{ob}	$V_{CB}=10V, I_E=0, f=1.0MHz$		6.0	pF
C_{ib}	$V_{EB}=0.5V, I_C=0, f=1.0MHz$		20	pF
h_{fe}	$V_{CE}=10V, I_C=1.0mA, f=1.0kHz$	50	200	
NF	$V_{CE}=5.0V, I_C=200\mu A, R_S=10\Omega,$ $f=10Hz \text{ to } 15.7kHz$		8.0	dB

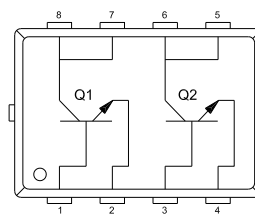
TLM832D CASE - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

PIN CONFIGURATION



LEAD CODE:

- 1) Base Q1
- 2) Emitter Q1
- 3) Base Q2
- 4) Emitter Q2
- 5) Collector Q2
- 6) Collector Q2
- 7) Collector Q1
- 8) Collector Q1

MARKING CODE: CFS

*** Note:**

- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6

R2 (19-February 2010)