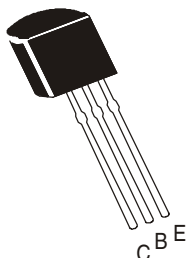


## NPN SILICON PLANAR EPITAXIAL TRANSISTORS

BC485, A, B, L  
BC487, A, B, L  
BC489, A, B, L

TO-92  
Plastic Package



### High Current Transistors

#### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ )

DESCRIPTION	SYMBOL	BC485	BC487	BC489	UNITS
Collector Emitter Voltage	$V_{CEO}$	45	60	80	V
Collector Base Voltage	$V_{CBO}$	45	60	80	V
Emitter Base Voltage	$V_{EBO}$	5.0			V
Collector Current Continuous	$I_C$	1.0			A
Power Dissipation at $T_a=25^\circ\text{C}$	$P_D$	625			W
Derate Above $25^\circ\text{C}$		5.0			mW/ $^\circ\text{C}$
Power Dissipation at $T_c=25^\circ\text{C}$	$P_D$	1.5			mW
Derate Above $25^\circ\text{C}$		12			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	- 55 to +150			$^\circ\text{C}$

#### THERMAL RESISTANCE

Junction to Case	$R_{th(j-c)}$	83.3	$^\circ\text{C/W}$
Junction to Ambient in free air	$R_{th(j-a)}$	200	$^\circ\text{C/W}$

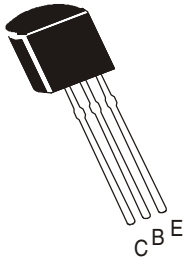
#### ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}$ unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	BC485	BC487	BC489	UNITS
Collector Emitter Voltage	$V_{CEO}$	$I_C=1\text{mA}, I_B=0$	>45	>60	>80	V
Collector Base Voltage	$V_{CBO}$	$I_C=100\mu\text{A}, I_E=0$	>45	>60	>80	V
Emitter Base Voltage	$V_{EBO}$	$I_E=10\mu\text{A}, I_C=0$	>5.0			V
Collector Cut Off Current	$I_{CBO}$	$V_{CB}=30\text{V}, I_E=0$	<100			nA
		$V_{CB}=40\text{V}, I_E=0$	<100			nA
		$V_{CB}=60\text{V}, I_E=0$	<100			nA
DC Current Gain	$h_{FE}$	$I_C=10\text{mA}, V_{CE}=2\text{V}$	>40			
		$I_C=100\text{mA}, V_{CE}=2\text{V}$				
		<b>BC485/487/489</b>	60 - 400			
		<b>BC485L/487L/489L</b>	60 - 150			
		<b>BC485A/487A/489A</b>	100 - 250			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=500\text{mA}, I_B=50\text{mA}$	<0.50			V
		$*I_C=1\text{A}, I_B=100\text{mA}$	TYP 0.30			V
Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=500\text{mA}, I_B=50\text{mA}$	<1.2			V
		$*I_C=1\text{A}, I_B=100\text{mA}$	TYP 0.9			V

\*Pulse test:- Pulse Width =300 $\mu\text{s}$ , Duty Cycle 2%

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NPN SILICON PLANAR EPITAXIAL TRANSISTORS



BC485, A, B, L  
BC487, A, B, L  
BC489, A, B, L

TO-92  
Plastic Package

ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C unless specified otherwise)

SMALL SIGNAL CHARACTERISTICS

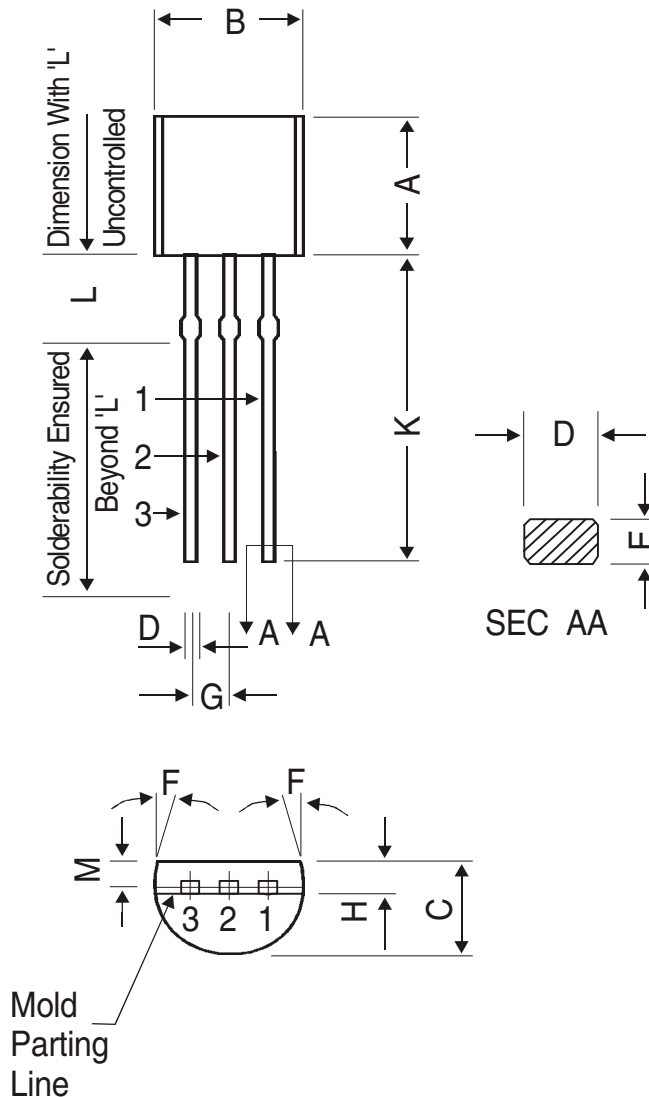
DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Transistors Frequency	f <sub>T</sub>	I <sub>C</sub> =50mA, V <sub>CE</sub> =2V, f=100MHz		200		MHz
Output Capacitance	C <sub>ob</sub>	V <sub>CB</sub> =10V, f=1MHz		7.0		pF
Input Capacitance	C <sub>ib</sub>	V <sub>EB</sub> =0.5V, f=1MHz		50		pF

BC487\_489Rev\_1 280306E

BC485, A, B, L  
BC487, A, B, L  
BC489, A, B, L

## TO-92 Plastic Package

### TO-92 Plastic Package

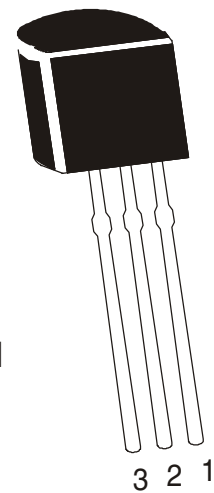


DIM	MIN.	MAX.
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5 DEG	
G	1.14	1.40
H	1.20	1.40
K	12.70	—
L	1.982	2.082
M	1.03	1.20

All dimensions are in mm

### PIN CONFIGURATION

1. EMITTER
2. BASE
3. COLLECTOR



The TO-92 Package , Tape and Ammo Pack drawings are correct as on the date of issue/revision of this Data Sheet.

The currently valid dimensions and information, may please be confirmed from the TO-92 Drawing in the Packages and Packing Section of the Product Catalogue.

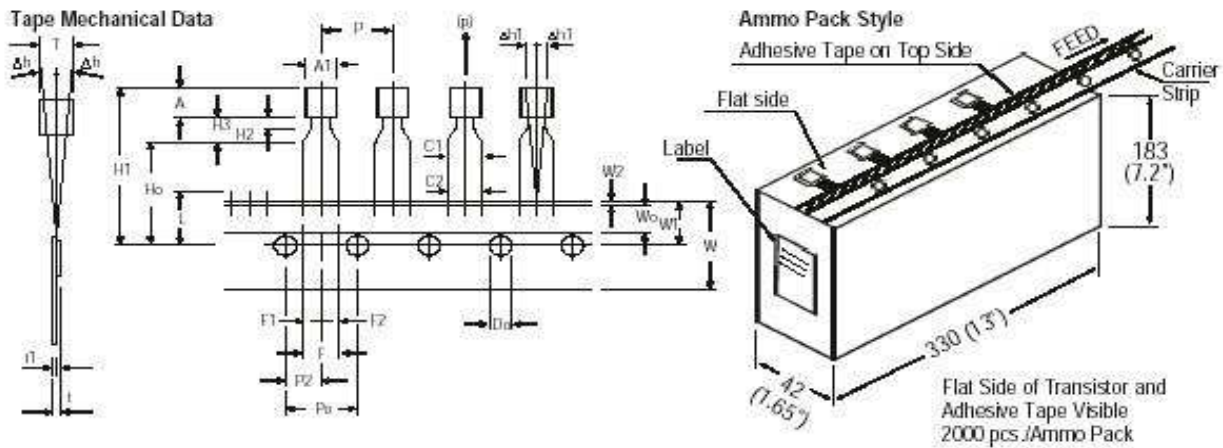
### Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/ Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5K	17" x 15" x 13.5"	80K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2K	17" x 15" x 13.5"	32K	12.5 kgs

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TO-92  
Plastic Package

TO-92 Tape and Ammo Pack



All dimensions are in mm

ITEM	SYMBOL	SPECIFICATION				
		MIN.	NOM.	MAX.	TOL.	
BODY WIDTH	A1	4.45		5.20		<b>NOTES</b> 1. Maximum alignment deviation between leads will not to be greater than 0.2mm. 2. Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches. 3. Holddown tape will not exceed beyond the edge(s) of carrier tape and there shall be no exposure of adhesive. 4. There will be no more than three (3) consecutive missing components in a tape. 5. A tape trailer, having at least three feed holes are provided after the last component in a tape. 6. Splices should not interfere with the sprocket feed holes.
BODY HEIGHT	A	4.32		5.33		
BODY THICKNESS	T	3.18		4.19		
PITCH OF COMPONENT	P		12.7		$\pm 1.0$	
*1 FEED HOLE PITCH	P0		12.7		$\pm 0.3$	
*2 FEED HOLE CENTRE TO COMPONENT CENTRE	P2		6.35		$\pm 0.4$	
DISTANCE BETWEEN OUTER LEADS	F		5.08		+0.6 -0.2	
*3 COMPONENT ALIGNMENT SIDE VIEW	$\Delta h$		0	1.0		
*4 COMPONENT ALIGNMENT FRONT VIEW	$\Delta h_1$		0	1.3		
TAPE WIDTH	W		18		$\pm 0.5$	
HOLD-DOWN TAPE WIDTH	W0		6		$\pm 0.2$	<b>REMARKS</b> *1 Cumulative pitch error 1.0 mm/20 pitch *2 To be measured at bottom of clinch *3 At top of body *4 At top of body *5 t1 0.3 – 0.6 mm
HOLE POSITION	W1		9		+0.7 -0.5	
HOLD-DOWN TAPE POSITION	W2	0.0		0.7		
LEAD WIRE CLINCH HEIGHT	H0		16		$\pm 0.5$	
COMPONENT HEIGHT	H1			24.0		
LENGTH OF SNIPPED LEADS	L			11.0		
FEED HOLE DIAMETER	Do		4		$\pm 0.2$	
*5 TOTAL TAPE THICKNESS	t			1.2		
LEAD - TO - LEAD DISTANCE	F1, F2	2.40		2.70	-0.1	
STAND OFF	H2	0.45		1.45		
CLINCH HEIGHT	H3			3.0		
LEAD PARALLELISM	C1 - C2			0.22		
PULL - OUT FORCE	(p)	6N				

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### **Disclaimer**

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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