

CH7512B DP to LVDS Monitor Controller

FEATURES

- Supports DisplayPort Specification version 1.1a
- Support 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate for notebook PC applications
- Supports input color depth 6, 8-bit per pixel in RGB format
- Supports Enhanced Framing Mode
- Support VESA and CEA timing standards up to 1920x1200 resolution in 8-bit input with 60Hz refresh rate
- HDCP engine compliant with HDCP 1.3 specification with internal HDCP Keys
- Support dynamic refresh rate switching
- Support Gamma correction
- Panel tuning methods including dithering and 6-bit + FRC
- Fast and full Link Training for DisplayPort system
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- Programmable LCD panel power sequence
- Support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS output interface
- Support both OpenLDI and SPWG bit mapping for LVDS application
- Support panel select by GPIO pins control or writing the chip registers.
- Flexible LVDS output pins swapping
- Blank panel during invalid input
- Supports PWM. Backlight luminance level control through AUX channel, PWM pin and BLUP/BLDN pin
- Support Dynamic Backlight Control
- Support OSD display when BLUP/BLDN pins control Backlight Luminance
- Hot Plug Detection
- Loads Boot ROM automatically upon power up
- Serial BOOT ROM data updated through I2C bus or AUX Channel
- Programmable power management
- EMI reduction capability for DP input and LVDS output. Spread spectrum control is available for transmitting LVDS signal
- Offered in a 68-pin QFN package

GENERAL DESCRIPTION

Chrontel's CH7512B is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the LVDS (Low-voltage Differential Signaling). This innovative DisplayPort receiver with an integrated LVDS transmitter is specially designed to target the All-In-One PC and the notebook market segments. Through the CH7512B's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized video data can be seamlessly converted to LVDS, a popular display technology for high-speed serial links in mid/large-sized LCD displays. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7512B is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7512B and the graphic chip.

The CH7512B is designed to meet the DisplayPort Specification 1.1a. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8 for LVDS output up to 1920x1200. To comply with GPU's new power saving scheme such as display frame rate reduction, the CH7512B is equipped with the Dynamic Refresh Rate switching method, which can automatically reduce to the low refresh rate supported by the LVDS panel.

The integrated LVDS transmitter supports the single port and the dual ports LVDS outputs to drive display resolution up to WUXGA (1920x1200). CH7512B supports panel select by GPIO[0:3] pins control or writing the chip registers. To reduce EMI emission, the CH7512B's LVDS encoder block has incorporated Spread Spectrum control and its spread percentage can be adjusted through the internal registers.

The Backlight On/Off and the PWM are two luminance control functions designed in the CH7512B LVDS power control module. The brightness control commands sent through AUX Channel can be dynamically translated by CH7512B and converted into LCD backlight control signal. The CH7512B will save the last setting of brightness level into the BOOT ROM and restore it upon power up. The CH7512B can dynamically adjust backlight brightness according to video stream to save power consumption and it supports OSD display in this way.

The CH7512B will immediately convert the DisplayPort signal to LVDS output after DisplayPort Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7512B's configuration settings in the serial BOOT ROM connected to the CH7512B. During system power-up and upon completion of the DisplayPort Link Training through AUX Channel, CH7512B will generate LVDS signal according to the panel power-up timing sequencing stored in the BOOT ROM.

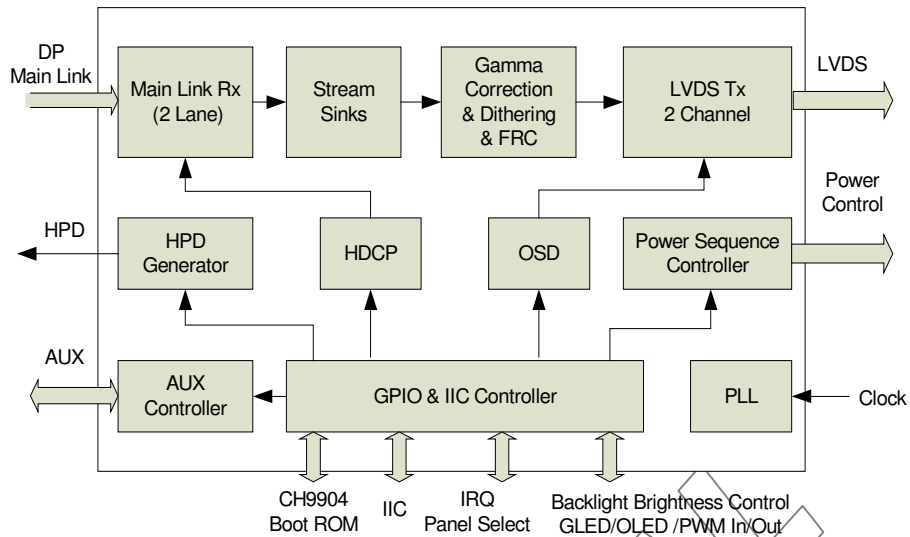


Figure 1: CH7512B Function Block Diagram

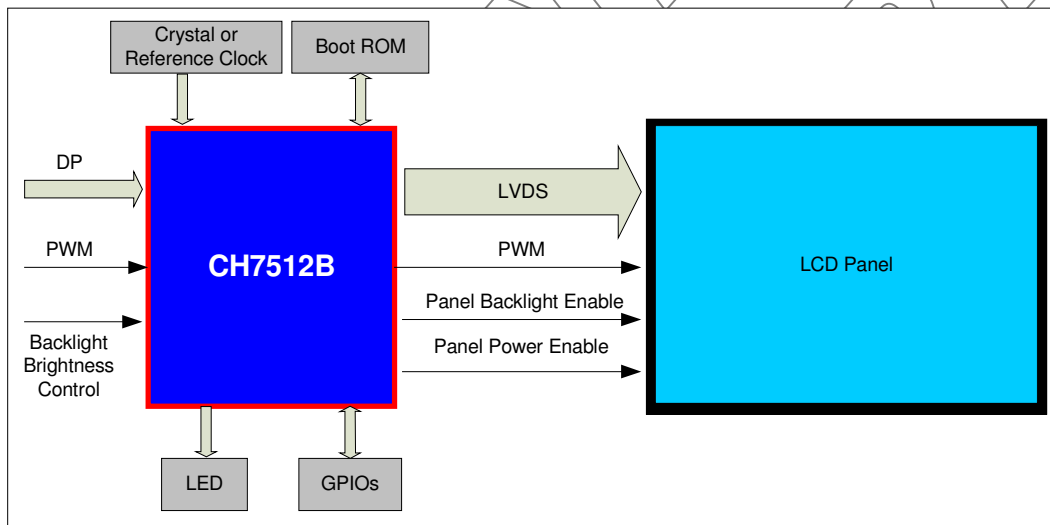


Figure 2: CH7512B Application Diagram

1.0 PIN ASSIGNMENT

1.1 Package Diagram

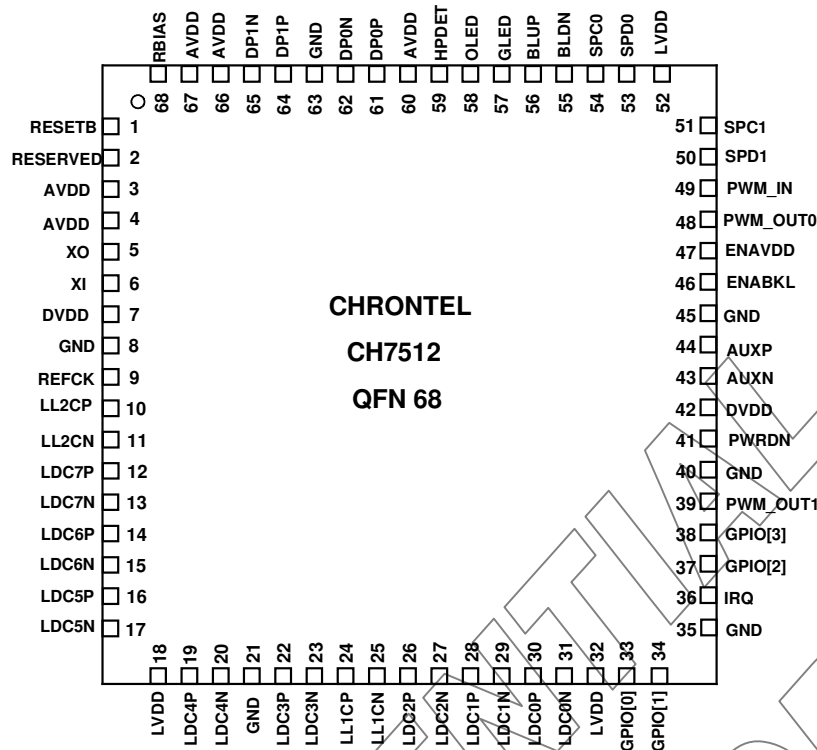


Figure 3: CH7512B 68-pin QFN pin out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	RESETB	Reset Input (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high (1.8V), reset is controlled through the serial port register. It should be pulled high to DVDD with a 10 KΩ resistor.
2		RESERVED	Reserved This pin should be left open in the application.
5	Out	XO	Crystal Output A parallel resonant 27MHz crystal (± 20 ppm) should be attached between this pin and XI. Note: 50ppm to pin XO
6	In	XI	Crystal Input A parallel resonant 27MHz crystal (± 20 ppm) should be attached between this pin and XO. Note: 50ppm to pin XI
9	In	REFCK	Reference Clock Input This pin is also used as clock input pin when injecting 27 MHz (3.3V) clock to CH7512B.
10~17, 19,20, 22~31	Out	LL1CP/N, LL2CP/N LDC [7:0] P/N	LVDS Output LDC7P/N ~ LDC0P/N can be configured to LVDS differential signals, which are used as A7M/P to A0M/P.

Pin #	Type	Symbol	Description
			LL1CP/N and LL2CP/N are used as CLK1 and CLK2 respectively.
33~34, 37~38	In	GPIO[3:0]	Panel Select Control Signals These pins could be pulled high (10 KΩ resistor to +3.3V) or low forming into 16 different combinations. Every combination can match with one panel type.
36	Out	IRQ	Programmable Interrupt output Output an interrupt signal while there's input from BLDN or BLUP.
39	Out	PWM_OUT1	PWM Output for Backlight Brightness Dimming PWM Duty Cycle Range: 30~100%(16 steps) The output Frequency from PWM_OUT1 can be up to 400KHz. Voltage level is 3.3V.
41	In	PWRDN	Power Down Control CH7512B enters/exit power down state when receiving active low pulse (0V) from this pin.
43,44	In/Out	AUXP, AUXN	AUX Channel Differential Input/Output These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
46	Out	ENABKL	LCD Panel Backlight Enable Enable backlight of LCD panel (3.3V)
47	Out	ENAVDD	LCD Panel VCC Enable Enable LCD panel VDD (3.3V)
48	Out	PWM_OUT0	PWM Output for Backlight Brightness Dimming / Bypass PWM_IN PWM Duty Cycle Range: 0~100%(16 steps) The output Frequency from PWM_OUT0 can be up to 400KHz. Voltage level is 3.3V. Bypass PWM input, and while in bypass mode, frequency of PWM_OUT0 can be up to 1MHz.
49	In	PWM_IN	Backlight brightness PWM input PWM_IN has two work modes: Bypass mode and Duty Cycle Multiplication with AUX CH mode. In bypass mode, the input frequency to PWM_IN can be up to 1MHz. In Duty Cycle Multiplication with AUX CH mode, the input frequency to PWM_IN can be up to 50KHz. Voltage level is 3.3V.
50	In/Out	SPD1	Serial Port Data Input/Output for Chip BOOT ROM/EDID This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4KΩ - 9 KΩ pull up resistor to 3.3V.
51	Out	SPC1	Serial Port Clock Output for Chip BOOT ROM/EDID This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4KΩ - 9KΩ pull up resistor to 3.3V.
53	In/Out	SPD0	Serial Port Data Input/Output for Register Map This pin is used to access CH7512B internal registers. It functions as the bi-directional data pin of the serial port and operates with input from 0 to 3.3V. Output is driven from 0 to 3.3V. This pin requires an external 6KΩ - 8 KΩ pull up resistor to 3.3V.
54	In	SPC0	Serial Port Clock Input for Register Map This pin is used to access CH7512B internal registers. It functions as the clock input of the serial port and operates with input from 0 to 3.3V. This pin requires an external 6KΩ - 8 KΩ pull up resistor to 3.3V.
55	In	BLDN	Decrement Backlight Brightness Input
56	In	BLUP	Increment Backlight Brightness Input
57	Out	GLED	Green LED Control This pin indicates CH7512B in normal power and mode status. Its output voltage is 3.3V.

Pin #	Type	Symbol	Description
58	Out	OLED	Orange LED Control This pin indicates CH7512B in abnormal power and mode status. Its output flickers from 0 or 3.3V.
59	Out	HPDET	Hot Plug Detect This output pin is used as the connection detection by a DisplayPort Source system. It generates interrupt pulse as defined by DisplayPort standard. The output voltage is 3.3V. A 100 kΩ resistor should be connected between this pin and GND. It should be linked to DisplayPort source.
61,62 64,65	In	DP[1:0]P/N	Main Link Lane Input These pins accept two AC-coupled differential pairs signals from the DisplayPort transmitter.
68	In	RBIAS	Band-gap Bias input A 10 KΩ(1%) resistor should be connected between this pin and GND.
3,4,60,66,6 7	Power	AVDD	Analog Power Supply (1.8V)
7,42	Power	DVDD	Digital Power Supply (1.8V)
18,32,52	Power	LVDD	LVDS Driver Power Supply and GPO Power Supply (3.3V)
8,21,35,40, 45,63, Thermal Exposed Pad	Power	GND	Power Ground

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2.0 PACKAGE DIMENSIONS

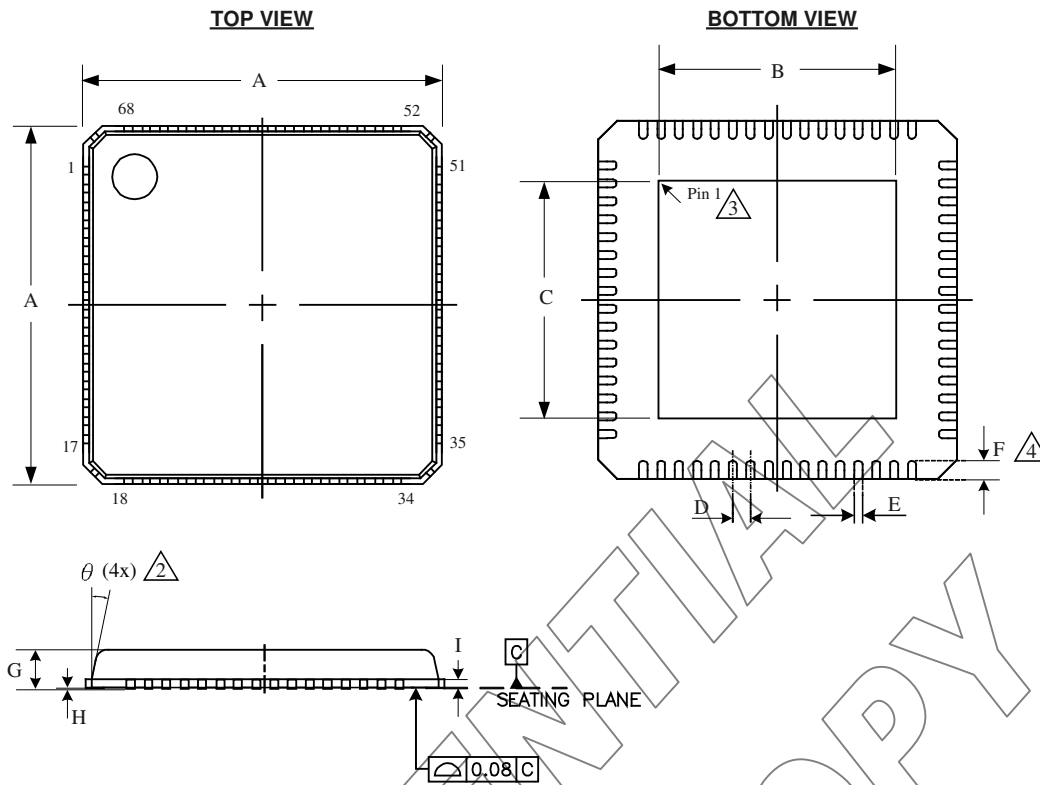


Figure 4: 68 Pin QFN Package (8 X 8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
68 (8 X 8 mm)		A	B	C	D	E	F	G	H	I
Milli- meters	MIN	7.90	5.45	5.45	0.40	0.15	0.30	0.80	0.00	0.20
	MAX	8.10	5.75	5.75	BSC	0.25	0.50	1.00	0.05	

Notes:

- Conforms to JEDEC standard JESD-30 MO-220.
- $\triangle 2$ Side of body may be square or curved.
- $\triangle 3$ Exposed pad may have chamfer in area of Pin 1.
- $\triangle 4$ Pins may protrude from edge of body by 0.05 mm.

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ORDERING INFORMATION			
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7512B-BF	68QFN, Lead-free	Commercial : -20 to 70°C	260/TRAY

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