CH7023/CH7024 TV Encoder

Features

- TV encoder targeting handheld and similar systems
- Support for NTSC, PAL
- Video output support for CVBS or S-video
- Macrovision™ 7.1.L1 copy protection support for SDTV (CH7023 only)
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supporting various RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) input data formats
- Support for input resolutions up to 720x480 and 720x576 (e.g. 220x176, 320x240, 640x480, 720x480, 720x576, etc.)
- Adjustable brightness, contrast, hue and saturation.
- Detect TV / Monitor connection
- Two high quality10-bit video DAC outputs
- Fully programmable through serial port
- Flexible pixel clock frequency from graphics controller (2.3MHz—64MHz)
- Flexible input clock on the crystal or oscillator (2.3MHz—64MHz)
- Flexible up and down scaling on the display
- Master and slave mode
- Offered in 48-pin LQFP and 49-pin TFBGA Package
- IO voltage and SPC/SPD from 1.2V to 3.3V
- Programmable power management
- Power down current less than 20uA typical
- Power consumption of <150mW for one CVBS output, single terminated and <350mW for two DAC outputs, double terminated.

General Description

The CH7023/CH7024 is a TV encoder device targeting handheld, portable video applications such as digital still cameras and similar portable embedded systems. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards.

Supported TV output formats are NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/A/I, PAL-M, PAL-N and PAL-60.

The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) via 24 bit/18 bit/15 bit /12 bit /8 bit multiplexed digital inputs. Most embedded controllers are supported. The I/O interface voltage between CH7023/CH7024 and digital video source controller can be selected by the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3V. The digital input voltage will follow the I/O supply voltage.

CH7023/CH7024 is offered in both 48-pin LQFP package (7 x 7 mm) and 49-pin TFBGA package (6 x 6 mm). CH7023/CH7024 48-pin LQFP package comes with fixed single serial port address while 49-pin TFBGA package provide two user selectable serial port addresses via AS pin pull up or pull down option. Refer to application note AN-98 for more information.

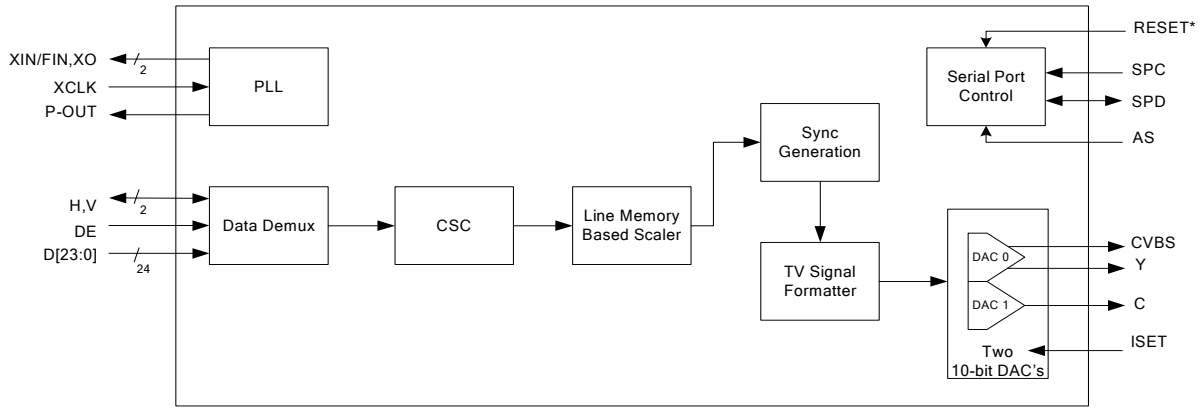

Figure 1: CH7023/CH7024 Block Diagram

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1.0 PIN-OUT

There are two major differences between CH7023/CH7024 48-pin LQFP and 49-pin TFBGA in pin-out: the video DACs output and the serial port address option using AS pin.

The CH7023/CH7024 48-pin LQFP comes with three video output pins, primary CVBS (pin 28), S-video Y (pin 27) and secondary CVBS or S-video C (pin 26). The CH7023/CH7024 49-pin TFBGA comes with two video outputs, primary CVBS or S-video Y (pin E5) and secondary CVBS or S-video C (pin F6).

The CH7023/CH7024 48-pin LQFP package comes with fixed single serial port address (76h – 7 bit address) while the CH7023/CH7024 49-pin TFBGA package provides two user selectable serial port addresses via AS pin pull up or pull down option.

1.1 Package Diagram

1.1.1 The 48-pin LQFP Package Diagram

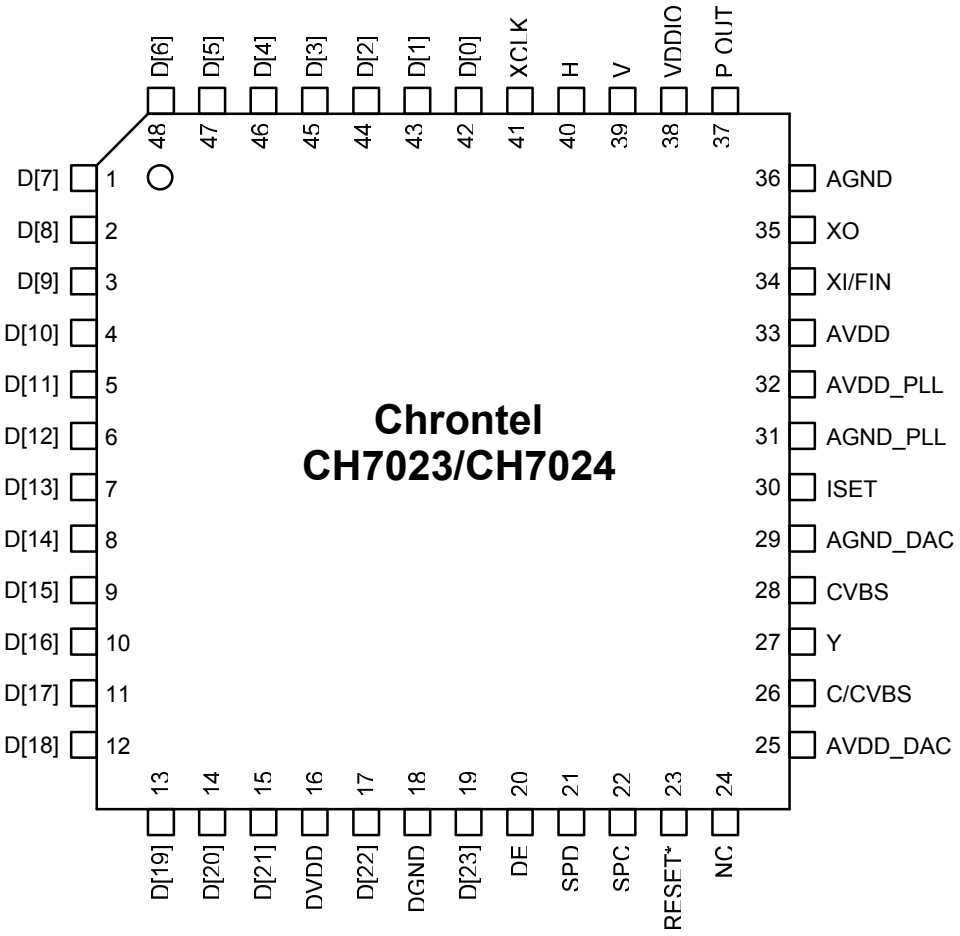

Figure 2: **48-LQFP Package (top view)**

1.1.2 The 49-pin TFBGA Package Diagram

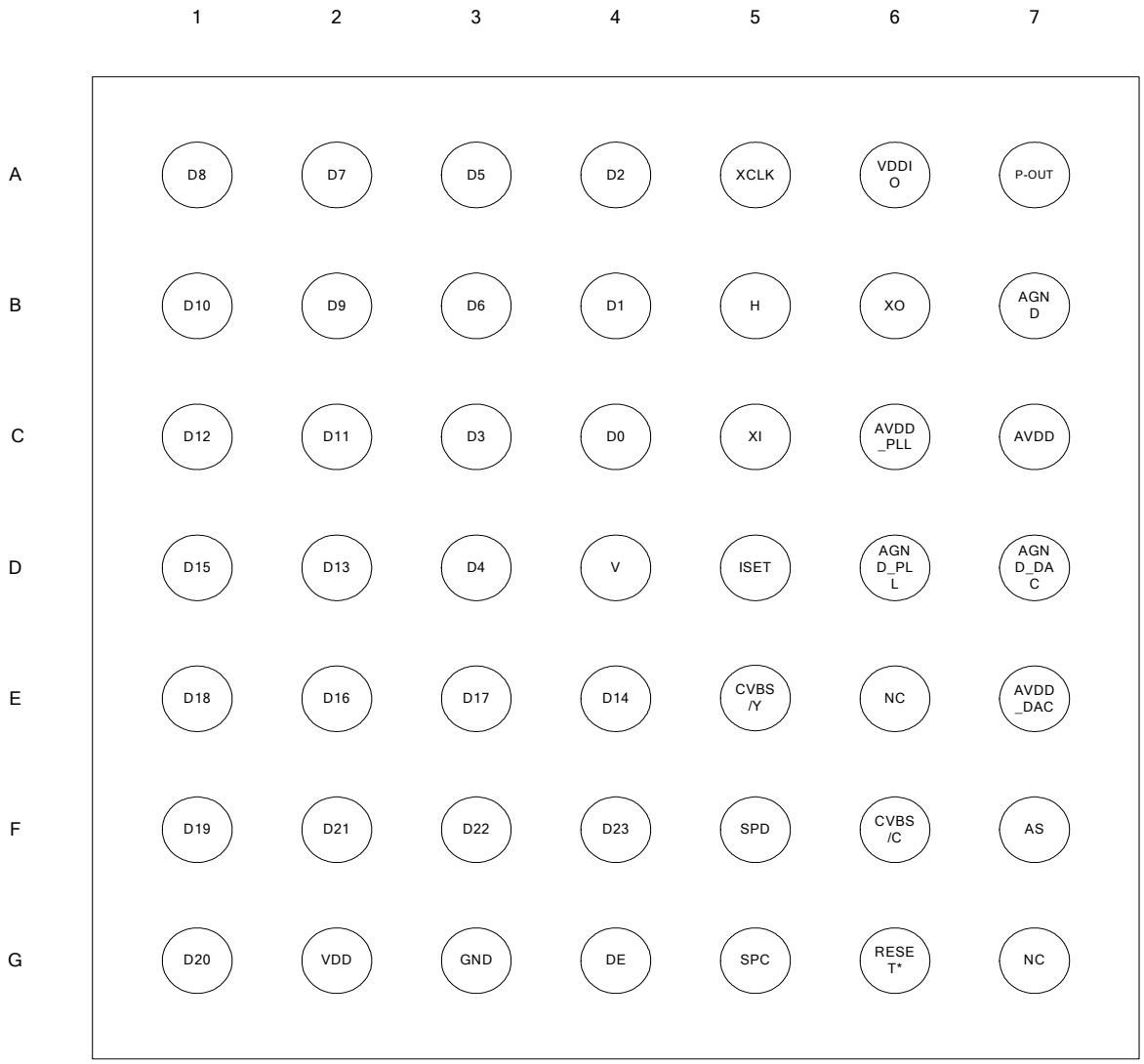

Figure 3: 49-Pin TFBGA Package (top view)

1.2 Pin Description

1.2.1 The 48-pin LQFP Pin Description

The 48-pin LQFP Package does not have AS pin to select second serial port address option. Refer to application note AN-98 for device address byte (DAB) details. The serial port device address for the read and write operation is fixed at ECh and EDh respectively.

It has internal switch to provide separate primary CVBS (pin 28) and S-video Y (pin27) outputs. Refer to section 2.3.2 Video DAC output and the Control Register 0Ah for the video DAC output control.

Table 1: Pin Description (48-pin LQFP)

Pin #	Type	Symbol	Description
42-48, 1-15, 17,19	In	D[0]-D[23]	Data[0] through Data[23] Inputs These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO.
40	In/Out	H	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The amplitude will be 0 to VDDIO.
39	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The amplitude will be 0 to VDDIO.
20	In	DE	Data Enable When the pin is high, the input data is active. When the pin is low, the input data is blanking.
24	–	NC	–
23	In	RESET*	Reset * Input This pin is internally pulled high. When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
21	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port and operates with input level from 0 to VDDIO. Outputs are driven from 0 to VDDIO.
22	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port and operates with input level from 0 to VDDIO.
28	Out	CVBS	Composite Video This is a primary composite vide output when S-video Y (pin 27) is not used. This output is turned off when S-video Y output is used.
27	Out	Y	Luma Output The output is S-video luminance when the primary CVBS output (pin 28) is not used.

Table 1: Pin Description (cont'd)

Pin #	Type	Symbol	Description
26	Out	C/CVBS	Chroma/CVBS Output The output is S-video chrominance when S-video is used. But, when dual CVBS outputs are needed, this out pin can be used for secondary CVBS output in addition to the primary CVBS output (pin 28).
30	In	ISET	Current Set Resistor This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin 29) using short and wide traces.
37	Out	P-Out	Pixel Clock Output This pin provides a clock signal to the graphics controller, which can be used as a reference frequency. The output driver is driven from the VDDIO supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
34	In	XI/FIN	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
35	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
41	In	XCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
38	Power	VDDIO	IO Supply Voltage (1.2-3.3V)
16	Power	DVDD	Digital Supply Voltage (1.8V)
18	Power	DGND	Digital Ground
25	Power	AVDD_DAC	DAC Supply Voltage (2.5-3.3V)
29	Power	AGND_DAC	DAC Ground
32	Power	AVDD_PLL	PLL Supply Voltage (1.8V)
31	Power	AGND_PLL	PLL Ground
33	Power	AVDD	Crystal Supply Voltage (2.5-3.3V)
36	Power	AGND	Crystal Ground

1.2.2 The 49-pin TFBGA Pin Description

The 49-pin TFBGA Package has AS pin to select second serial port address. Refer to application note AN-98 for device address byte (DAB). The device address for read operation can be either ECh or EAh based on external pull-down or pull-up with AS pin respectively. The device address for write operation can be either EDh or EBh.
It does not has internal switch to provide separate primary CVBS and S-video Y outputs. Instead, it has single or dual CVBSs or S-video C and Y output. Refer to section 2.3.2 Video DAC output and the Control Register 0Ah for the video DAC output control.

Table 2: Pin Description (49-pin TFBGA)

BGA Pin #	Type	Symbol	Description
A1-4,B1-B4,C1-C4,D1-D3,E1-E4, F1-F4,G1	In	D[0]-D[23]	Data[0] through Data[23] Inputs These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO.
B5	In/Out	H	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply.
D4	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
G4	In	DE	Data Enable When the pin is high, the input data is active. When the pin is low, the input data is blanking.
F7	In	AS	Serial Port Address Select This pin is internally pulled low. When AS is high, the address is 75h – 7 bit address. Otherwise, the address is 76h – 7 bit address.
G7	–	NC	–
G6	In	RESET*	Reset * Input This pin is internally pulled high. When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
F5	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port and operates with input level from 0 to VDDIO. Outputs are driven from 0 to VDDIO.
G5	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port and operates with input level from 0 to VDDIO.
E6	–	NC	–
E5	Out	CVBS/Y	Luma Output The output can be either a primary CVBS or S-video luminance.

Table 2: Pin Description (cont'd)

BGA Pin #	Type	Symbol	Description
F6	Out	CVBS/C	Chroma Output The output can be either secondary CVBS when dual CVBSs are needed or S-video chrominance when S-video is selected. In single CVBS output mode, this output is turned off to save power.
D5	Out	ISET	Current Set Resistor This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin D7) using short and wide traces.
A7	Out	P-Out	Pixel Clock Output This pin provides a clock signal to the graphics controller, which can be used as a reference frequency. The output driver is driven from the VDDIO supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
C5	In	XI/FIN	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XO. However, an external +3.3V CMOS compatible clock can drive the XI/FIN input.
B6	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
A5	In	XCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
A6	Power	VDDIO	IO Supply Voltage (1.2-3.3V)
G2	Power	VDD	Digital Supply Voltage (1.8V)
G3	Power	GND	Digital Ground
E7	Power	AVDD_DAC	DAC Supply Voltage (2.5-3.3V)
D7	Power	AGND_DAC	DAC Ground
C6	Power	AVDD_PLL	PLL Supply Voltage (1.8V)
D6	Power	AGND_PLL	PLL Ground
C7	Power	AVDD	Crystal Supply Voltage (2.5-3.3V)
B7	Power	AGND	Crystal Ground

2.0 FUNCTIONAL DESCRIPTION

2.1 Modes of Operation

Table 3: Operating Modes describes the possible operating modes for CH7023/CH7024 TV encoder. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Basically, CH7023/CH7024 can take non-interlaced data from graphics controller and encode it to analog NTSC and PAL waveforms. It can also take interlaced data from sources and perform SDTV encoding.

Table 3: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
Non-Interlaced	RGB / YCrCb	Interlaced	CVBS, S-video	SDTV encoder (NTSC / PAL) with non-interlaced input	2.1.1
Interlaced (480i, 576i)	RGB / YCrCb	Interlaced	CVBS, S-video	SDTV encoder (NTSC / PAL) with interlaced input	2.1.2

2.1.1 Graphics Controller to SDTV Encoder

CH7023/CH7024 is mainly designed as an SDTV encoder targeting handheld device market. In this mode, the graphics controller of the handheld system will send non-interlaced data, sync and clock signals to CH7023/CH7024. CH7023/CH7024 can run in clock master mode or clock slave mode. In clock master mode, an accurate (less than 20ppm) crystal is required between XI/FIN and XO pins or an accurate CMOS clock signal is needed on the XI/FIN pin. The frequency of the crystal or the clock has to be between 2.3MHz and 64MHz. CH7023/CH7024 will generate a reference clock signal (P-Out) according to the requirement of the graphics controller. However, the range of this clock reference signal is between 2.3MHz and 64MHz. In clock slave mode, no reference clock is output to the graphics controller. So, the crystal becomes may only be necessary for color sub-carrier generation in the slave mode. However, if the clock from the graphics controller cannot meet the requirement of color sub-carrier generation, the crystal is still required, which will discuss in the latter part of this document. Horizontal and vertical sync signals are normally sent to the device from the graphics controller, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. However, the DE signal is NOT generated inside. Data can be unitary or 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data will be scaled, scan converted and filtered, then encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-video and CVBS format. The graphics resolutions supported are from 220x176 to 720x576. The typical resolutions are shown in Table 4.

Table 4: Typical Input Resolution

Typical Input Resolution	220x176	320x240	512x384	640x400	640x480	720x400	720x480	720x576
TV Output Standard	NTSC,PAL							

2.1.2 ITU-R BT.601/656 TV Encoder

In interlaced data, sync and clock signals are input to the CH7023/CH7024 from a graphics controllers digital output port, or the output of an MPEG decoder device. The YCrCb data format is most commonly used in these modes. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals are normally sent to the CH7023/CH7024 from the graphics device, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. Data can be unitary or 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data bypasses the scaling, scan conversion and filtering blocks, is encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-video and CVBS format. The graphics resolutions supported for ITU-R BT.601/656 TV output are shown in Table 5 below. The CH7023 is capable of adding Macrovision™ encoding to the output signal. CH7024 is non-Macrovision™ part. The timing of the sync signals is shown in Figure 4 below. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7023/CH7024 to identify the correct field.

Table 5: ITU-R BT.601/656 TV Encoder Operating Modes

Input Resolution	TV Output Standard
720x480i	NTSC
720x576i	PAL

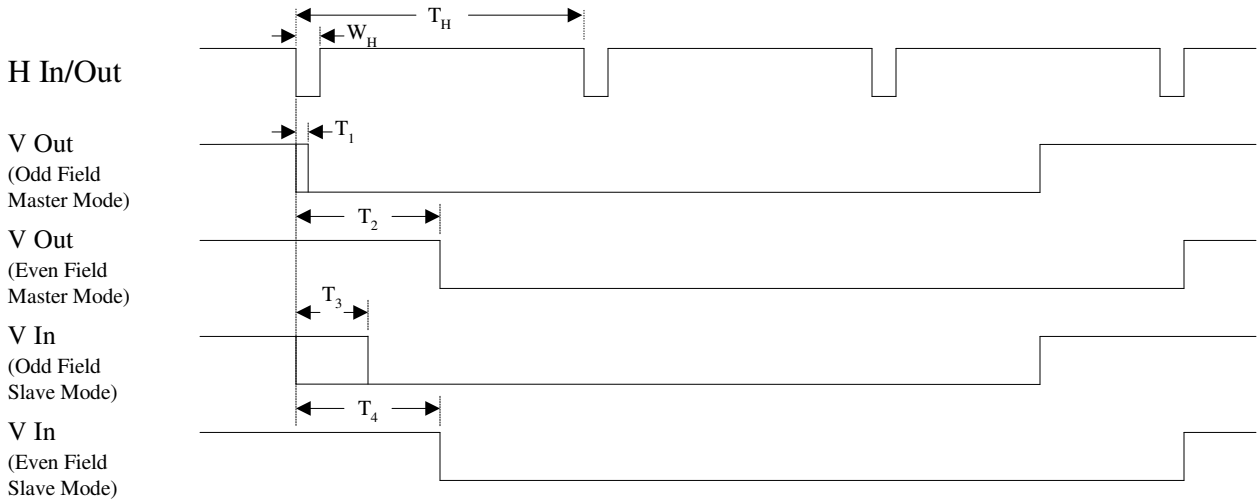

Figure 4: Interlaced Sync Input/Output Timing

Table 6: Interlaced Sync Input/Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{PCK}	Input clock period	6.73		47.62	us
T_H	Total Line Period SDTV	63.5		63.5	us
W_H	Hsync Width When output from CH7023/CH7024 When input to CH7023/CH7024	 1 1	 64 64		 Pixel clocks Pixel clocks
T_1	Odd Field (Field 1) V SYNC out to H SYNC out alignment		0		us
T_2	Even Field (Field 2) V SYNC out delay from H SYNC out		$0.5*T_H$		us
T_3	Odd Field (Field 1) V SYNC in to H SYNC in alignment	0		$W_H - T_{PCK}$	us
T_4	Even Field (Field 2) V SYNC in delay from H SYNC in	W_H		$T_H - T_{PCK}$	us

2.2 Input Interface

2.2.1 Overview

Three distinct methods of transferring data to the CH7023/CH7024 are described. They are:
Unitary data, clock input at 1X the pixel rate
Multiplexed data, clock input at 1X the pixel rate
Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7023/CH7024 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7023/CH7024 is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7023/CH7024 is latched with one edge of the clock .The polarity of the pixel clock can be reversed under serial port control.

2.2.2 Input Clock and Data Timing Diagram

Figure 5 below shows the timing diagram for input data and clocks. The first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in section 3.5.

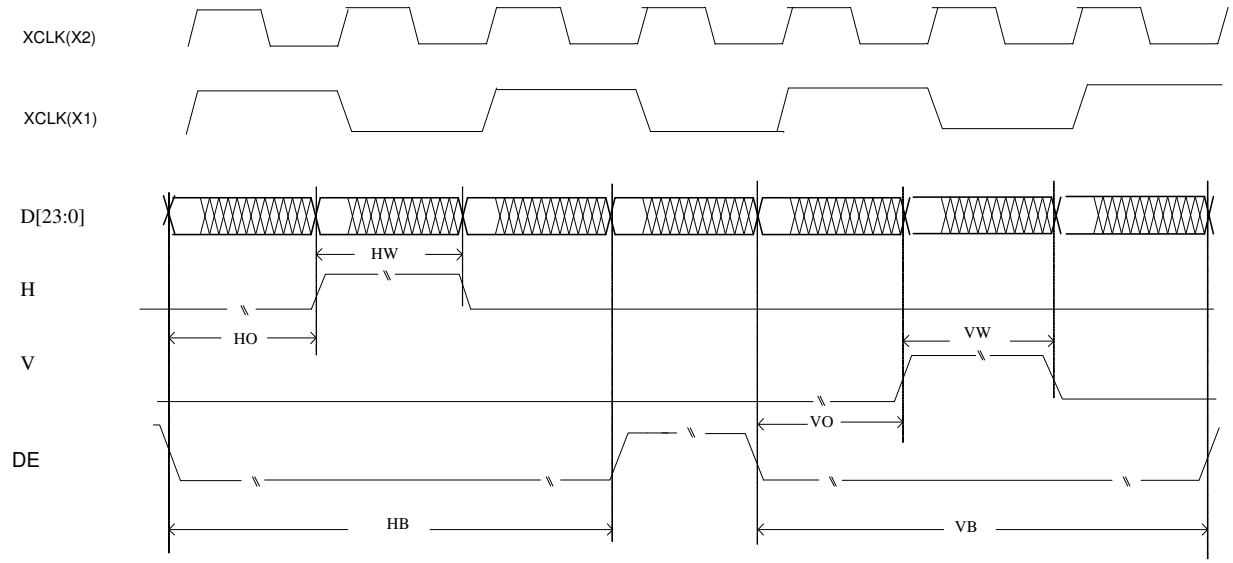

Figure 5: Clock, Data and Interface Timing

2.2.3 Input data voltage

The voltage level of input pins D[23:0], H, V, DE, SPC, SPD are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit DIFFEN(Control Register 0Eh) is high, the input is pseudo differential mode which use a reference voltage to compare with input voltage and decide input logic value. The pseudo differential mode can accept the wide range of the input voltage level from 1.2V to 3.3V, while the CMOS mode can accept 1.8V to 3.3V Input voltage.

2.2.4 Input data formats

The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) via 24 bit/18 bit/ 15 bit /12 bit / 8 bit multiplexed digital inputs to support most of existing industry Embedded controller to provide TV encoder solution.

CH7023/CH7024 Input Data Format (IDF) are grouped into two major group. These are unitary IDF modes and multiplexed IDF modes. In the unitary IDF mode (Control Register 0Ch, control bit MULTI = 0), all of control bits SWAP, REVERSE and HIGH bit of the control register 0Dh can be used. While, in the multiplexed IDF mode (Control Register 0Ch, control bit MULTI = 1), only REVERSE and HIGH bits are used for IDF5, YCrCb 4:2:2 mode.
For the unitary IDF mode, refer to Table 7 and note for more description or refer to Table 8 for the multiplexed IDF mode.

Table 7: Input Data Formats in single data rate mode (MULTI = 0, see Register 0Dh)

IDF= Format =	PIN	0 RGB888	1 DVO	2 RGB666	3 RGB565	4 RGB555	5 YCrCb4:2:2 (CBCRSW =0)		5 YCbCr4:2:2 (CBCRSW =1)		6 YCbCr4:4:4
Pixel#		P0	P0	P0	P0	P0	P0	P1	P0	P1	P0
Busdata	D[23]	R[7]	R[7]								Y[7]
	D[22]	R[6]	R[6]								Y[6]
	D[21]	R[5]	R[5]	R[5]							Y[5]
	D[20]	R[4]	R[4]	R[4]	R[4]	R[4]					Y[4]
	D[19]	R[3]	R[3]	R[3]	R[3]	R[3]					Y[3]
	D[18]	R[2]	G[7]	R[2]	R[2]	R[2]					Y[2]
	D[17]	R[1]	G[6]	R[1]	R[1]	R[1]					Y[1]
	D[16]	R[0]	G[5]	R[0]	R[0]	R[0]					Y[0]
	D[15]	G[7]	R[2]				Y0[7]	Y1[7]	Y0[7]	Y1[7]	Cr[7]
	D[14]	G[6]	R[1]				Y0[6]	Y1[6]	Y0[6]	Y1[6]	Cr[6]
	D[13]	G[5]	R[0]	G[5]	G[5]		Y0[5]	Y1[5]	Y0[5]	Y1[5]	Cr[5]
	D[12]	G[4]	G[1]	G[4]	G[4]	G[4]	Y0[4]	Y1[4]	Y0[4]	Y1[4]	Cr[4]
	D[11]	G[3]	G[4]	G[3]	G[3]	G[3]	Y0[3]	Y1[3]	Y0[3]	Y1[3]	Cr[3]
	D[10]	G[2]	G[3]	G[2]	G[2]	G[2]	Y0[2]	Y1[2]	Y0[2]	Y1[2]	Cr[2]
	D[9]	G[1]	G[2]	G[1]	G[1]	G[1]	Y0[1]	Y1[1]	Y0[1]	Y1[1]	Cr[1]
	D[8]	G[0]	B[7]	G[0]	G[0]	G[0]	Y0[0]	Y1[0]	Y0[0]	Y1[0]	Cr[0]
	D[7]	B[7]	B[6]				Cr0[7]	Cb0[7]	Cb0[7]	Cr0[7]	Cb[7]
	D[6]	B[6]	B[5]				Cr0[6]	Cb0[6]	Cb0[6]	Cr0[6]	Cb[6]
	D[5]	B[5]	B[4]	B[5]			Cr0[5]	Cb0[5]	Cb0[5]	Cr0[5]	Cb[5]
	D[4]	B[4]	B[3]	B[4]	B[4]	B[4]	Cr0[4]	Cb0[4]	Cb0[4]	Cr0[4]	Cb[4]
	D[3]	B[3]	G[0]	B[3]	B[3]	B[3]	Cr0[3]	Cb0[3]	Cb0[3]	Cr0[3]	Cb[3]
	D[2]	B[2]	B[2]	B[2]	B[2]	B[2]	Cr0[2]	Cb0[2]	Cb0[2]	Cr0[2]	Cb[2]
	D[1]	B[1]	B[1]	B[1]	B[1]	B[1]	Cr0[1]	Cb0[1]	Cb0[1]	Cr0[1]	Cb[1]
	D[0]	B[0]	B[0]	B[0]	B[0]	B[0]	Cr0[0]	Cb0[0]	Cb0[0]	Cr0[0]	Cb[0]

Note: In IDF = 0 mode, 24 bits digital inputs D[23:0]can be assigned to the CH7023/CH7024 internal RGB registers by either SWAP[2:0] or REVERSE bit via **Control Register** (**Address = 0Dh**) . SWAP controls R, G, B register byte order from the input D[23:0], while REVERSE bit controls reverse 7 bits assignment order within R,G, B registers.

For examples, If **REVERSE bit = 0 and SWAP[2:0] =** 000 , then D[23:0] = R[7:0]G[7:0]B[7:0],
else if **REVERSE bit = 1 and SWAP[2:0]** = 000 , then D[23:0] = R[0:7]G[0:7]B[0:7];
The **HIGH** control bit is used in the unitary mode only. For the **HIGH** bit usage , refer to IDF 2, 3, 4 in the unitary IDF mode.

1. In unitary IDF = 0 mode, RGB888 , from input D[23:0] to internal RGB register as shown below:

If **REVERSE bit = 0 and SWAP[2:0] =** 000 , then D[23:0] = R[7:0]G[7:0]B[7:0];
001 , then D[23:0] = R[7:0]B[7:0]G[7:0];
010 , then D[23:0] = G[7:0]R[7:0]B[7:0];
011 , then D[23:0] = G[7:0]B[7:0]R[7:0];
100 , then D[23:0] = B[7:0]R[7:0]G[7:0];
101 , then D[23:0] = B[7:0]G[7:0]R[7:0].

If **REVERSE bit = 1 and SWAP[2:0]** = 000 , then D[23:0] = R[0:7]G[0:7]B[0:7];
001 , then D[23:0] = R[0:7]B[0:7]G[0:7];
010 , then D[23:0] = G[0:7]R[0:7]B[0:7];
011 , then D[23:0] = G[0:7]B[0:7]R[0:7];
100 , then D[23:0] = B[0:7]R[0:7]G[0:7];
101 , then D[23:0] = B[0:7]G[0:7]R[0:7].

.

2. In unitary IDF = 1, DVO (see Control Register 0Dh)

{D[23:19],D[15:13],D[18:16],D[11:9],D[12],D[3],D[8:4],D[2:0]} = {R[7:0], G[7:0], B[7:0]}

3. In non-multiplexed IDF = 2, RGB666 (see Control Register 0Dh)

High bit of the Control Register (0Dh), controls insertion of logical value '1' into blank bit within R,G and B registers when input data bits width is less than 8 bit wide. When the High bit = 0, value '1' is inserted to bit 7 and bit 6 of internal R, G and B registers. If High bit = 1 is selected, value '1' is inserted to bit 1 and bit 0 of the CH7023/CH7024 internal R, G and B registers. (2'b11 means assign corresponding 2 bits with logical value 1 in binary number.)

SWAP: (see Control Register 0Dh)

000 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2b'11} = {R[7:0], G[7:0], B[7:0]};
001 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {R[7:0], B[7:0], G[7:0]};
010 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {G[7:0], R[7:0], B[7:0]};
011 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {G[7:0], B[7:0], R[7:0]};
100 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {B[7:0], R[7:0], G[7:0]};
101 , then {D[21:16],2'b11, D[13:8],2'b11, D[5:0],2'b11} = {B[7:0], G[7:0], R[7:0]}.
110: then {D[17:12],2'b11, D[11:6],2'b11, D[5:0],2'b11} = {R[7:0], G[7:0], B[7:0]};
111: then {D[21:16],2'b11, D[15:14],D[11:8],2'b11, D[5:0],2'b11} = {R[7:0]G[7:0]B[7:0]}.

REVERSE: (see Control Register 0Dh)

0: {D[21:16],2'b11,D[13:8],2'b11,D[5:0],2'b11} = {R[7:0],G[7:0],B[7:0]};
1: {2'b11, D[21:16],2'b11,D[13:8],2'b11,D[5:0]} ={R[0:7],G[0:7],B[0:7]};

HIGH: (see Control Register 0Dh)

0: {2'b11,D[21:16], 2'b11,D[13:8], 2'b11,D[5:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:18],2'b11,D[15:10],2'b11,D[7:2],2'b11} = {R[7:0], G[7:0], B[7:0]};

4. In unitary IDF = 3, RGB565 (see Control Register 0Dh)

(Note: 2'b11 means assign corresponding 2 bits with logical value 1 in binary number.
3'B111 means assign corresponding 3 bits with logical value 1 in binary number.)

SWAP: (see Control Register 0Dh)

000: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
001: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], B[7:0], G[7:0]};
010: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {G[7:0], R[7:0], B[7:0]};
011: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {G[7:0], B[7:0], R7:0]};
100: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {B[7:0], G[7:0], G[7:0]};
101: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {B[7:0], G[7:0], B[7:0]};
110: {D[15:11],3'b111,D[10:5],2'b11,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
111: {D[20:16],3'b111,D[15:14],D[11:8],2'b11,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]}.

REVERSE: (see Control Register 0Dh)
0: {D[20:16],3'b111, D[13:8],2'b11, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
1: {3'b111, D[20:16], 2'b11, D[13:8], 3'b111,D[4:0]} = {R[0:7], G[0:7], B[0:7]};

HIGH: (see Control Register 0Dh)
0: {3'b111,D[20:16], 3'b11,D[13:8], 3'b111,D[4:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:19],3'b111, D[15:10],2'b11, D[7:3],3'b111} = {R[7:0], G[7:0], B[7:0]};

5. In unitary IDF = 4, RGB555 (see Control Register 0Dh)
(3'B111 means assign corresponding 3 bits with logical value 1 in binary number.)
SWAP: (see Control Register 0Dh)
000: {D[20:16],3'b111, D[12:8],3'b111, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
001: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {R[7:0], B[7:0], G[7:0]};
010: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {G[7:0], R[7:0], B[7:0]};
011: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {G[7:0], B[7:0], R7:0]};
100: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {B[7:0], G[7:0], G[7:0]};
101: {D[20:16],3'b111, D[13:8],3'b111, D[4:0],3'b111} = {B[7:0], G[7:0], B[7:0]};
110: {D[14:10],3'b111, D[9:5],3'b111, D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
111: {D[20:16],3'b111, D[14],D[11:8],3'b111, D[4:0],3'b111} = {R[7:0],G[7:0],B[7:0]}.
REVERSE: (see Control Register 0Dh)
0: {D[20:16],3'b111,D[12:8],3'b111,D[4:0],3'b111} = {R[7:0], G[7:0], B[7:0]};
1: {3'b111,D[20:16], 3'b111,D[12:8], 3'b111,D[4:0]} = {R[0:7], G[0:7], B[0:7]};
HIGH: (see Control Register 0Dh)
0: {3'b111,D[20:16], 3'b111,D[12:8], 3'b111,D[4:0]} = {R[7:0], G[7:0], B[7:0]};
1: {D[23:19],3'b111, D[15:11],3'b111, D[7:3],3'b111} = {R[7:0], G[7:0], B[7:0]};

6. In unitary IDF = 5, YCbCr 4:2:2 (see Control Register 0Dh)
Note that only the SWAP[0] bit is used in this mode.
SWAP: (see Control Register 0Dh)
xx0: D[15:0] = Y[7:0]C[7:0];
xx1: D[15:0] = C[7:0]Y[7:0];
REVERSE: (see Control Register 0Dh)
0: D[15:0] = Y[7:0]C[7:0];
1: D[15:0] = Y[0:7]C[0:7];
HIGH: (see Control Register 0Dh)
0: D[15:0] = Y[7:0]C[7:0]; (non-multiplexed format only)
1: D[23:8] = Y[0:7]C[0:7]; (non-multiplexed format only)

7. In unitary IDF = 6, YCbCr 4:4:4 (see Control Register 0Dh)
SWAP: (see Control Register 0Dh)
000: D[23:0] = Y[7:0], Cr[7:0], Cb[7:0];
001: D[23:0] = Y[7:0], Cb[7:0], Cr[7:0];
010: D[23:0] = Cr[7:0], Y[7:0], Cb[7:0];
011: D[23:0] = Cr[7:0], Cb[7:0], Y[7:0];
100: D[23:0] = Cb[7:0], Y[7:0], Cr[7:0];
101: D[23:0] = Cb[7:0], Cr[7:0], Y[7:0];
REVERSE: (see Control Register 0Dh)
0 : D[23:0] = Y[7:0], Cr[7:0], Cb[7:0].
1 : D[23:0] = Y[0:7], Cr[0:7], Cb[0:7].

In RGB666, RGB565, RGB555, the RGB data are continuously distributed when SWAP[2:0] = 110 .

Table 8: Multiplexed Input Data Formats (MULTI = 1, see Register 0Dh)

IDF = Format =	PIN	0 12-bit RGB		1 DVO		5 YCrCb4:2:2 (CBCRSW =0)		5 YCbCr4:2:2 (CBCRSW =1)		6 12-bit YCbCr	
Pixel #		P0a	P0b	P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G[3]	R[7]	G[4]	R[7]					Y[3]	Cr[7]
	D[10]	G[2]	R[6]	G[3]	R[6]					Y[2]	Cr[6]
	D[9]	G[1]	R[5]	G[2]	R[5]					Y[1]	Cr[5]
	D[8]	G[0]	R[4]	B[7]	R[4]					Y[0]	Cr[4]
	D[7]	B[7]	R[3]	B[6]	R[3]	Cr0[7]	Y1[7]	Cb0[7]	Y0[7]	Cb[7]	Cr[3]
	D[6]	B[6]	R[2]	B[5]	G[7]	Cr0[6]	Y1[6]	Cb0[6]	Y0[6]	Cb[6]	Cr[2]
	D[5]	B[5]	R[1]	B[4]	G[6]	Cr0[5]	Y1[5]	Cb0[5]	Y0[5]	Cb[5]	Cr[1]
	D[4]	B[4]	R[0]	B[3]	G[5]	Cr0[4]	Y1[4]	Cb0[4]	Y0[4]	Cb[4]	Cr[0]
	D[3]	B[3]	G[7]	G[0]	R[2]	Cr0[3]	Y1[3]	Cb0[3]	Y0[3]	Cb[3]	Y[7]
	D[2]	B[2]	G[6]	B[2]	R[1]	Cr0[2]	Y1[2]	Cb0[2]	Y0[2]	Cb[2]	Y[6]
	D[1]	B[1]	G[5]	B[1]	R[0]	Cr0[1]	Y1[1]	Cb0[1]	Y0[1]	Cb[1]	Y[5]
	D[0]	B[0]	G[4]	B[0]	G[1]	Cr0[0]	Y1[0]	Cb0[0]	Y0[0]	Cb[0]	Y[4]

1. In multiplexed IDF = 5, YCbCr 4:2:2 (see Control Register 0Dh)

Note that only the SWAP[0] bit is used in this mode.

SWAP: (see Control Register 0Dh)

xx0: D[15:0] = Y[7:0]C[7:0];

xx1: D[15:0] = C[7:0]Y[7:0];

REVERSE: (see Control Register 0Dh)

0: D[7:0] = Y[7:0]/C[7:0];

1: D[7:0] = Y[0:7]/C[0:7];

The multiplexed input data format is shown in Figure 6 below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

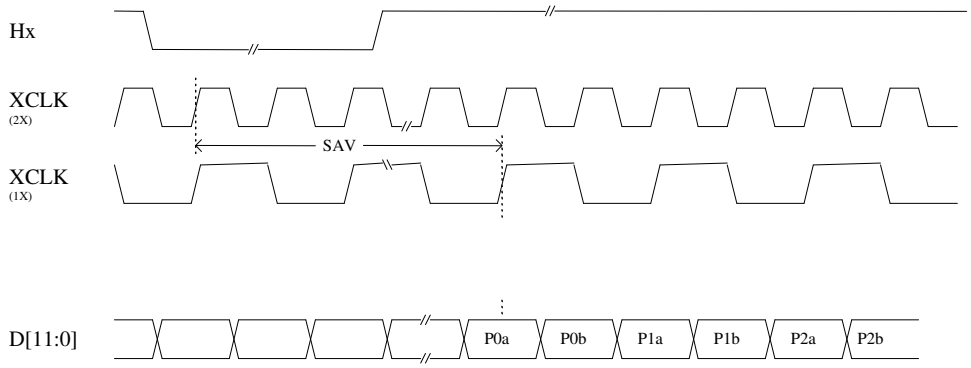

Figure 6: 12-bit Multiplexed Input Data Formats

In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connect error and correct it automatically, for example, if the input P14 and P15 are a group, but you take P13 and P14 as a group, the hardware can detect this error and correct it by run-in code.

2.3 TV Output

2.3.1 TV Output Format

The CH7023/CH7024 support the following output formats:

Table 9: Supported SDTV standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	50	864x625	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

2.3.2 Video DAC Outputs

Table 10 below lists the DAC output configurations of the CH7023/CH7024.

Table 10: Video DAC Configurations for CH7023/CH7024

Output Type of 48 pin LQFP	**DACA0=CVBS or DACA0=Y**	**DAC1-C/CVBS**
Single CVBS	CVBS	off
Dual CVBS	CVBS	CVBS
S-video	Y	C
Output Type of 49 pin BGA	**DACB0 =CVBS/Y**	**DAC1=CVBS/C**
Single CVBS	CVBS	off
Dual CVBS	CVBS	CVBS
S-video	Y	C

2.3.3 DAC single/double termination

The DAC output of CH7023/CH7024 can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. See also the description of SEL_R bit of the Control Register 63h

2.3.4 TV connection detect

CH7023/CH7024 support detecting the TV connection by setting the SENSEEN bit of the Control Register 62h**.** It can detect which DAC are connected, short to ground or not connected. So it can distinguish single CVBS connected with other connection, but it can not distinguish dual CVBS connected with S-video connected. See also the DUCVBS bit description of the Control Register 0Ch and the SVD/DDAC bit description of the Control Register 0Ah.

2.3.5 TV picture adjustment

The CH7023/CH7024 has the capability of vertical and horizontal output picture position adjustment. The CH7023/CH7024 will automatically put the picture in the display center, and the position is also programmable through user input. The CH7023/CH7024 also provides brightness/sharpness/contrast, hue and saturation adjustments.

2.3.6 TV reference clock output

The CH7023/CH7024 support operating in Clock Master Mode. The CH7023/CH7024 integrates the low jitter PLL to generate a reference clock for the graphics controller for reference.

2.3.7 Color Sub-carrier Generation

The CH7023/CH7024 has two ways to generate the color sub-carrier frequency. If the XCLK from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the XCLK. However, since even a ±0.01% sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7023/CH7024 has the ability to generate the sub-carrier frequency from the crystal when the XCLK from the graphics device cannot meet the requirement. In this case, the crystal has to be present. In other words, the only configuration where the off-chip crystal can be removed is when slave mode is used and the graphics controller provides XCLK with required characteristics.

In addition, the CH7023/CH7024 has the capability to genlock the color sub-carrier with Vsync. Also, CH7023/CH7024 has the ability to operate in a “stop dot crawl” mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.3.8 ITU-R BT.470 Compliance

The CH7023/CH7024 is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of XCLK from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the filter selection.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
VDD18	All 1.8V power supplies relative to GND	-0.5		2.5	V
VDD33	All 3.3V power supplies relative to GND	-0.5		5.0	V
VDDIO	Input voltage of all digital pins (see note)	GND – 0.5		VDDIO+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-55		125	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 seconds)			260	°C
	Vapor phase soldering (11 seconds)			245	°C
	Vapor phase soldering (60 seconds)			225	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the recommended operating condition of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V may cause permanent damage to the device.

The digital input voltage will follow the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3V

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	3.1	3.3	3.5	V
AVDD_DAC	DACs Power Supply Voltage	3.1 2.5①	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.1		3.5	V
RL1	Output load to DAC Current Reference Pin ISET		1.2k		Ω
RL2	Output load to DAC Outputs, Pins CVBS, Y, and C		37.5 75②		Ω
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	3.1③	3.3	3.5	V
	Ambient operating temperature	0		70	°C

Note①: TFBGA package only.
Note②: Single terminated.
Note③: Except otherwise indicated.

3.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33=3.3V± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		34		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		32		mA
I_{VDD33}	Total VDD33 supply current (3.3V supplies) (See Note)		25		mA
I_{PD}	Total Power Down Current		< 20		uA

Note: The VDD33 supply current is 18mA for one DAC single 75-Ohm termination. The current will be 35mA for one DAC double 75-Ohm termination (37.5Ohm). For two DACs, the current will be doubled according to different termination.

3.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data Input High Voltage (see Note 1)		VDDIO/2+0.25		VDDIO + 0.5	V
V_{DATAIL}	Data Input Low Voltage		GND-0.5		VDDIO/2-0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (see Note 2)		2.7		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage		GND-0.5		0.6	V
I_{MISCPU}	Miscellaneous input Pull Up Current	V_{IN} = 0V	0.5		5.0	uA
$V_{P-OUTOH}$	P-OUT Output High Voltage	I_{OH} = - 0.4mA	VDD18-0.2			V
$V_{P-OUTOL}$	P-OUT Output Low Voltage	I_{OL} = 4 mA			0.2	V

Note :

1. Data input means the following pins: D[23:0], XCLK, H, V and DE. VDDIO is the I/O supply voltage. The range is from 1.2V to 3.3V.
2. Vmisc means the following pins: AS, RESET*.

3.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency		2.3		64	MHz
f_{XCLK}	Input (XCLK) frequency		2.3		64	MHz
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[23:0], H, V and DE to XCLK	XCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to XCLK	D[23:0], H, V, DE = Vref to XCLK	0.5			ns
t_R	Pout, Output Rise Time (20% - 80%)	15pF load VDD33= 3.3V, VDD18=1.8V			1.50	ns
t_F	Pout Output Fall Time (20% - 80%)	15pF load VDD33=3.3V, VDD18=1.8V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

3.6 ESD Rating

2KV HBM per JEDEC standard JESD22-A114C.

4.0 PACKAGE DIMENSIONS

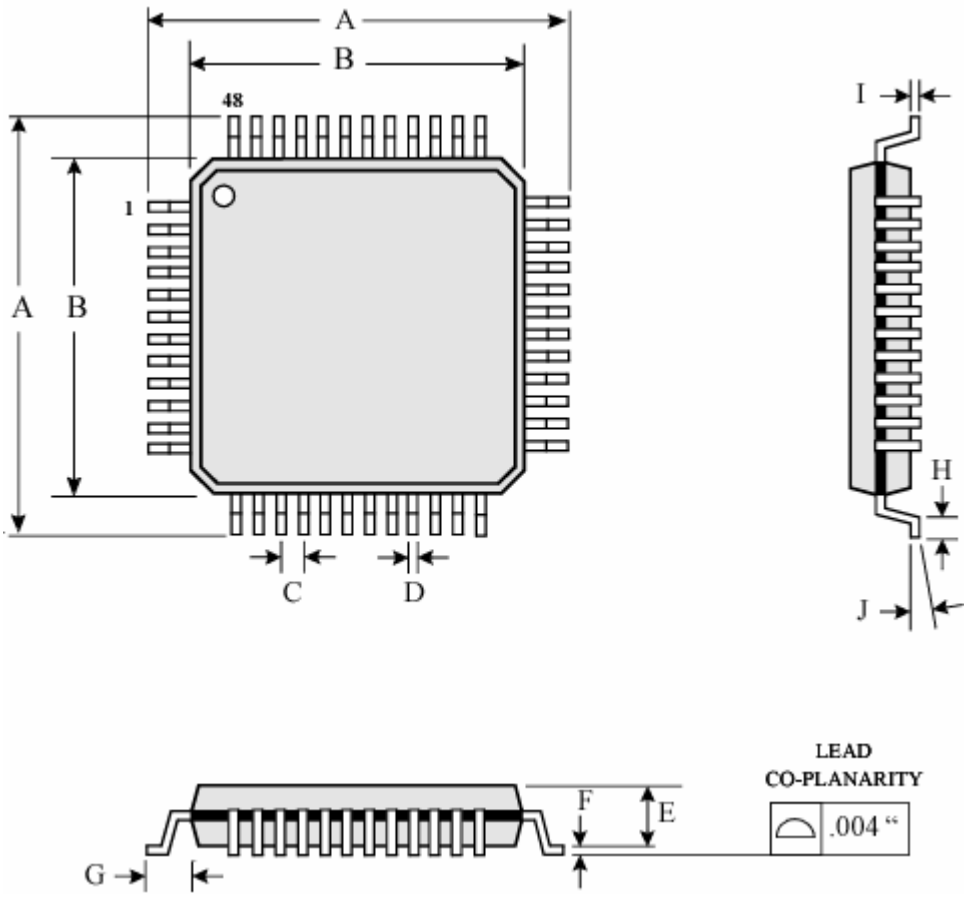

Figure 7: 48 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	9	7	0.5	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

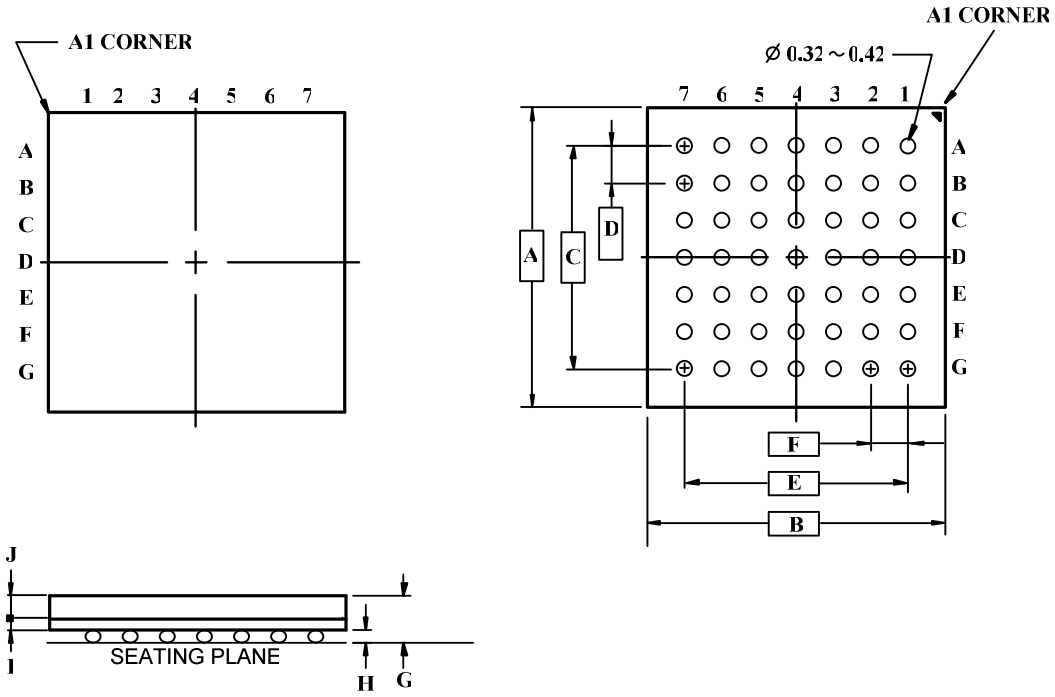

Figure 8: 49 Pin TFBGA Package

Table of Dimensions

No. of Leads		SYMBOL									
49 (6 X 6 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	6.00	6.00	4.80	0.80	4.80	0.80		0.22	0.26	0.53
	MAX							1.20	0.32		

Notes:

1. All dimensions conform to JEDEC standard MO-216.

5.0 REVISION HISTORY

Rev. #	Date	Section	Description
1.0	6/6/2006	-	Official release.
1.1	12/15/2006	1.2.1, 1.2.2	Updated Pin Description.
1.11	1/15/2007	4.1, 4.2	Updated Section 4.1 and 4.2
1.12	2/8/2007	3.3.1	Corrected Register 0Fh YCV[1] and Register 1Ch BSTADJ bit corrected to Bits[3:1].
1.13	4/25/2007	5.0	Updated Figure 8, 49-Pin TFBGA package drawing.
1.14	6/8/2007	2.2.4	Corrected Table 8: Multiplexed Input Data Formats (MULTI = 1, see Register 0Dh).

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ORDERING INFORMATION

Part Number	Package Type	Copy Protection	Output Video Switch	Shipping Format
CH7023B-GF	49TFBGA, Lead-free	Macrovision™	No	Tray, 4290 per dry pack bag
CH7023B-GF-TR	49TFBGA, Lead-free, Tape & reel	Macrovision™	No	T&R, 2000 per dry pack bag
CH7023B-DF	48LQFP, Lead-free	Macrovision™	Yes	Tray, 2500 per dry pack bag
CH7023B-DF-TR	48LQFP, Lead-free, Tape & reel	Macrovision™	Yes	T&R, 1000 per dry pack bag
CH7024B-GF	49TFBGA, Lead-free	None	No	Tray, 4290 per dry pack bag
CH7024B-GF-TR	49TFBGA, Lead-free, Tape & reel	None	No	T&R, 2000 per dry pack bag
CH7024B-DF	48LQFP, Lead-free	None	Yes	Tray, 2500 per dry pack bag
CH7024B-DF-TR	48LQFP, Lead-free, Tape & reel	None	Yes	T&R, 1000 per dry pack bag

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