CH7010 DVI / TV Output Device

1. FEATURES

- DVI Transmitter up to 165M pixels/second
- DVI low jitter PLL
- DVI hot plug detection
- TV output supporting graphics resolutions up to 1024 x768 pixels
- Programmable digital interface supports RGB and YCrCb
- True scale rendering engine supports underscan in all TV output resolutions
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering
- Support for all NTSC and PAL formats
- Provides CVBS, S-Video and SCART (RGB) outputs
- TV connection detection
- Programmable power management
- 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 64-pin LQFP package

2. GENERAL DESCRIPTION

The CH7010 is a display controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI (DFP can also be supported) or TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data formats including RGB and YCrCb.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit data. The CH7010 comes in versions able to drive a DVI display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

The TV-Out processor performs non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for RGB bypass mode which enables driving a VGA CRT with the input data.

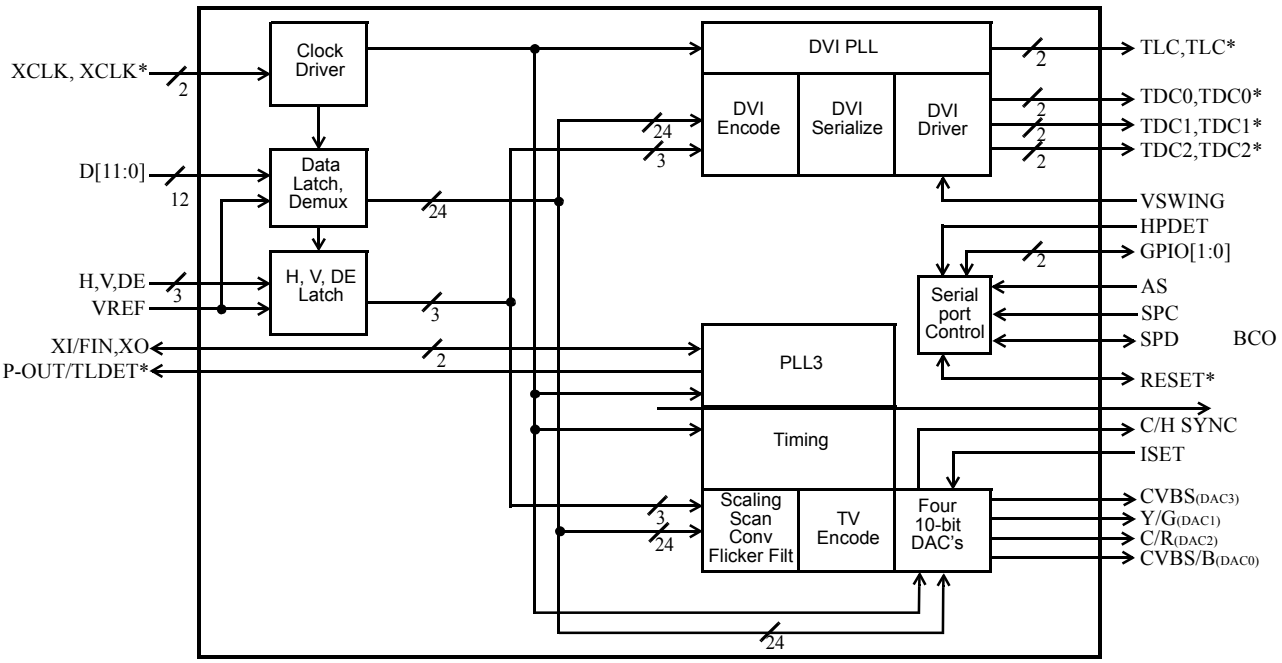

Figure 1. Functional Block Diagram

3. PIN DESCRIPTIONS

3.1 Package Diagram

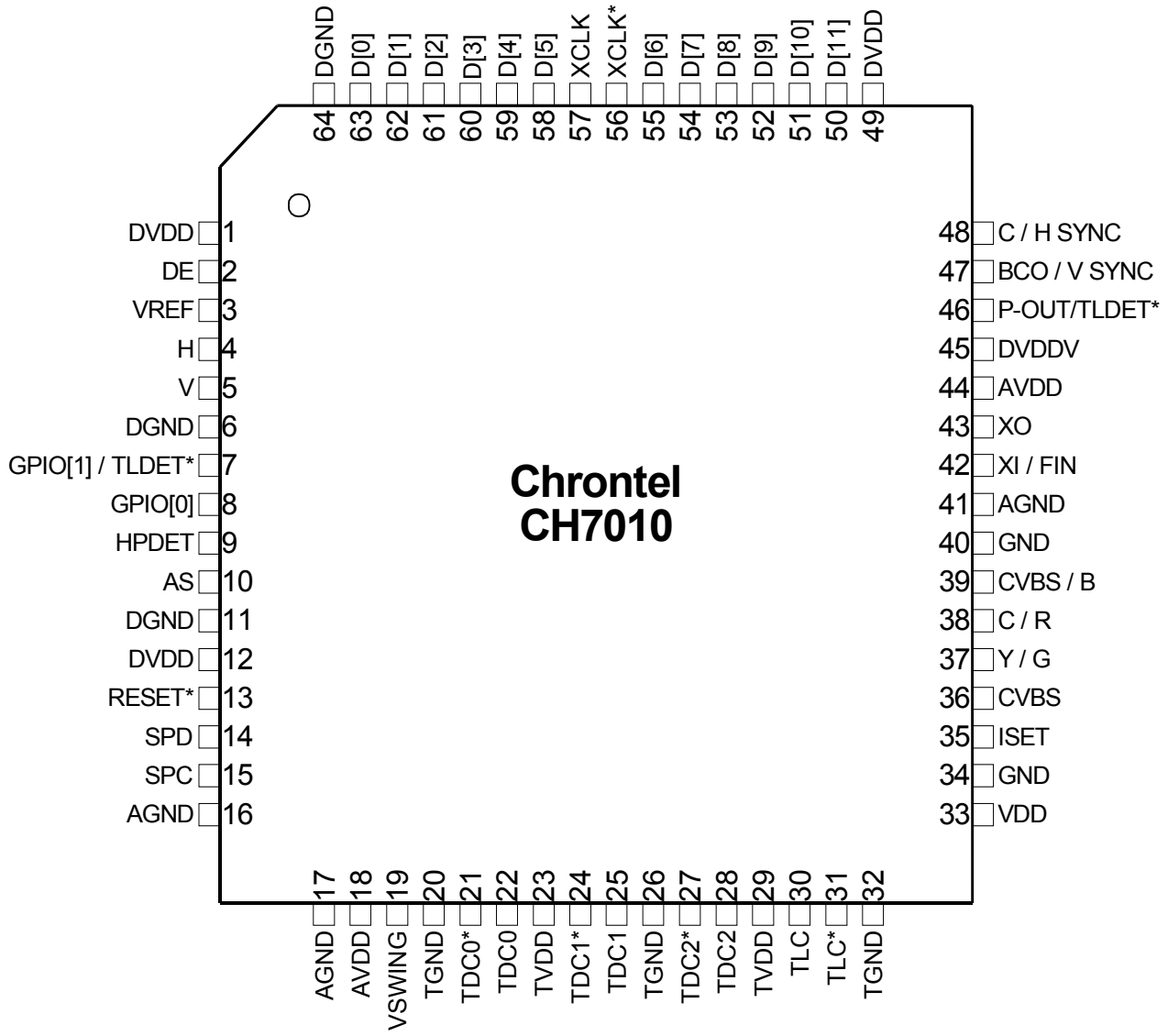

Figure 2. 64-Pin LQFP

3.2 Pin Description

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
2	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level. This input is used by the DVI. The TV-Out function uses H and V sync signals as reference to active video.
3	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of DVDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs.
4	1	In/Out	H	**Horizontal Sync Input / Output** When the SYO bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to DVDDV, and the VREF signal is used as the threshold level. When the SYO bit is high, the device will output a horizontal sync pulse, 64 pixels wide. The output is driven from the DVDD. This output is only for use with the TV-Out function.
5	1	In/Out	V	**Vertical Sync Input / Output** When the SYO bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to DVDDV, and the VREF signal is used as the threshold level. When the SYO bit is high, the device will output a vertical sync pulse one line wide. The output is driven from the DVDD supply. This output is only for use with the TV-Out function.
7	2	In/Out	GPIO[1] / TLDET*	**General Purpose Input - Output[1] /** **DVI Detect Output** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port. When the GPIO[1] pin is configured as an output, this pin can be used to output the DVI detect signal (pulls low when a termination change has been detected on the input). This is an open drain output. The output is released through serial port control.
8	2	In/Out	GPIO[0]	**General Purpose Input - Output[0]** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up.
9	1	In	HPDET	**Hot Plug Detect** (internal pull-down) This input pin determines whether the DVI is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the P-OUT/TLDET* or GPIO[1]/TLDET* pin pulling low. When the HPDET is pulled low, the DVI output driver will be shut down.
10	1	In	AS	**Address Select** (Internal pull-up) This pin determines the serial port address of the device (1,1,1,0,1,AS*,AS).

Table 1. Pin Description *(continued)*

64-Pin LQFP	# Pins	Type	Symbol	Description
13	1	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the serial port data pin of the serial port interface, and uses the DVDD supply.
15	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port interface, and uses the DVDD supply.
19	1	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces.
22, 21	2	Out	TDC0, TDC0*	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0 (blue).
25, 24	2	Out	TDC1, TDC1*	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1 (green).
28, 27	2	Out	TDC2, TDC2*	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2 (red).
30, 31	2	Out	TLC, TLC*	**DVI Clock Outputs** These pins provide the differential clock output for the DVI interface corresponding to data on the TDC[0:2] outputs.
35	1	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (DAC ground) using short and wide traces.
36	1	Out	CVBS	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load.
37	1	Out	Y/G	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green.
38	1	Out	C/R	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red.
39	1	Out	CVBS/B	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue.
42	1	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal ($\pm$ 20 ppm) should be attached between this pin and XO. However, an external clock can drive the XI/FIN input.
64-Pin LQFP	**# Pins**	**Type**	**Symbol**	**Description**

Table 1. Pin Description *(continued)*

43	1	In	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
46	1	Out	P-OUT / TLDET*	**Pixel Clock Output / DVI Detect Output** When the CH7010 is operating as a VGA to TV encoder in master clock mode, this pin provides a pixel clock signal to the VGA controller which is used as a reference frequency. The output is selectable between 1X or 2X of the pixel clock frequency. The output driver is driven from the DVDDV supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum. When the CH7010 is operating as a DVI transmitter, this pin provides an open drain output which pulls low when a termination change has been detected on the HPDET input. The output is released through serial port control.
47	1	Out	BCO/ V SYNC	**Buffered Clock Output / Vertical Sync Output** This output pin provides a buffered clock output, driven by the DVDD supply. The output clock can be selected using the BCO register. This pin can also be used as VSYNC output.
48	1	Out	C/H SYNC	**Composite / Horizontal Sync Output** This pin can be selected to output a TV composite sync, TV horizontal sync, or a buffered version of the VGA horizontal sync. The output is driven from the DVDD supply.
50 – 55, 58 – 63	12	In / Out	D[11] - D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level.
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the CH7010 for use with the H, V, DE and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The output clocks from this pad cell are able to have their polarities reversed under the control of the MCP bit (in register 1Ch).
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage (3.3V-3.6V)**
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	DVDDV	**I/O Supply Voltage (3.3V to 1.1V)**
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage (3.3V-3.6V)**
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**
18, 44	2	Power	AVDD	**PLL Supply Voltage (3.3V-3.6V)**
16, 17, 41	3	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage (3.3V-3.6V)**
34, 40	2	Power	GND	**DAC Ground**

4. MODES OF OPERATION

The CH7010 is capable of being operated as a single DVI output, or as a VGA to TV encoder. The two modes of operation cannot be used simultaneously. Descriptions of each of the operating modes, with a block diagram of the data flow within the device is shown below.

4.1 DVI Output

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7010 from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table below, and a block diagram of the CH7010 is shown on the following page. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any value of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. In the block diagram, all blocks are shown. Those blocks which are non-active are shown as shaded. The clock and data paths which are in use are highlighted. Although the block diagram does not show this path as being active, the data input can be selected to be output by the DACs as a VGA type output. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

Table 2. DVI Output

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	XCLK Frequency (MHz)	DVI Frequency (MHz)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
720x480[1]	4:3	9:8	59.94	27	270
720x576[2]	4:3	15:12	50	27	270
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<60	<67	<670
1280x1024	4:3	1:1	<85	<158	<1580
1600x1200	4:3	1:1	<60	<165	<1650
1920x1080	16:9	1:1	<30[2]	<140	<1400

[1] These DVD compatible modes are input in a non-interlaced RGB data format.

[2] 30Hz in progressive scan modes, 60Hz in interlaced modes.

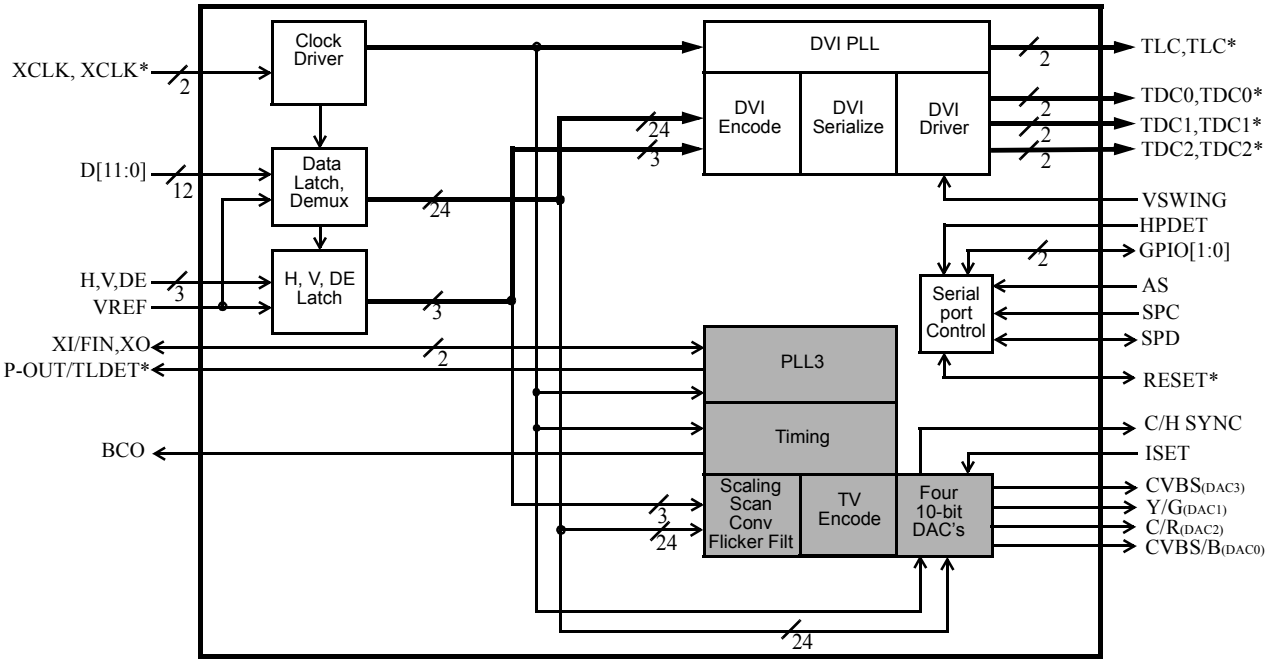

Figure 3. DVI Output

4.2 TV Output

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7010 from the graphics controller's digital output port. A P-OUT clock can be output as a frequency reference to the graphics controller, **which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7010 from the graphics controller**, but can be output to the graphics controller as an option. This method should not be used for pixel frequencies above 50 MHz. Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DAC's. The modes supported for TV output are shown in the table below, and a block diagram of the CH7010 is shown on the following page. In the block diagram, all blocks are shown. Those blocks which are non-active are shown as shaded. The clock and data paths which are in use are highlighted.

Table 3. TV Output Modes

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480[1]	4:3	9:8	NTSC	1/1
720x480[2]	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576[1]	4:3	15:12	PAL	1/1
720x576[2]	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

[1] These DVD modes operate with interlaced input, scan conversion and flicker filter are bypassed.

[2] These DVD modes operate with non-interlaced input, scan conversion is not bypassed.

In order to minimize the hazard of ESD, a set of protection diodes MUST BE used for each DAC connecting to TV (Refer to AN-38 for details).

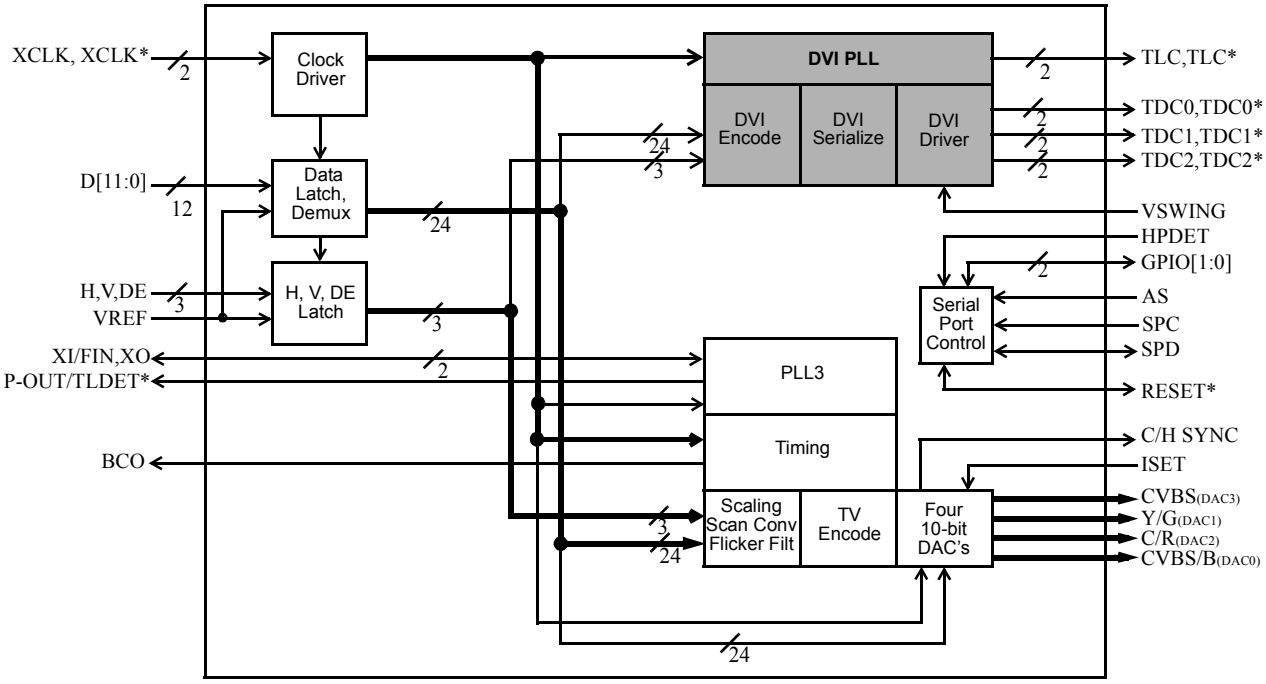

Figure 4. TV Output Modes

5. INPUT INTERFACE

Two distinct methods of transferring data to the CH7010 are described. They are:

- Multiplexed data, clock input at 1X pixel rate
- Multiplexed data, clock input at 2X pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7010 is latched with both edges of the clock (also referred to as dual-edge transfer mode). For the multiplexed data, clock at 2X pixel rate, the data applied to the CH7010 is latched with one edge of the clock. The polarity of the pixel clock can be reversed under serial port control.

5.1 Input Clock and Data Timing Diagram

The figure below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 2X pixel rate method. The second XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 1X pixel rate method.

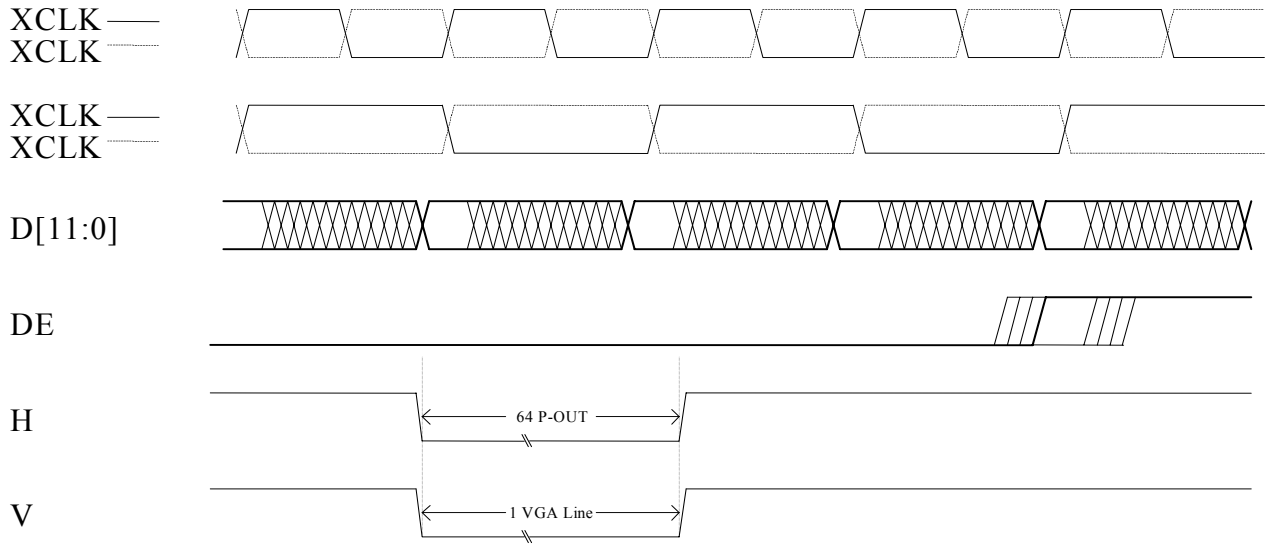

Figure 5. Interface Timing

Regarding the CH7010 timing specifications, please see **Figure 18** - **Figure 20** for details.

5.2 Input Clock and Data Formats

The 12 data inputs support 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge. The data received by the CH7010 can be used to drive the DVI output, the VGA to TV encoder, or directly drive the DAC's. The multiplexed input data formats are (IDF[2:0]):

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB2 input (24-bit color), (multiplex scheme 2)
2	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)

For multiplexed input data formats, either both transitions of the XCLK/XCLK* clock pair, or each rising or falling edge of the clock pair (depending upon MCP bit, rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal) will latch data from the graphics chip. The multiplexed input data formats are shown in the figures below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (eg; P0a and P0b) will contain a complete pixel encoded as shown in the tables below. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

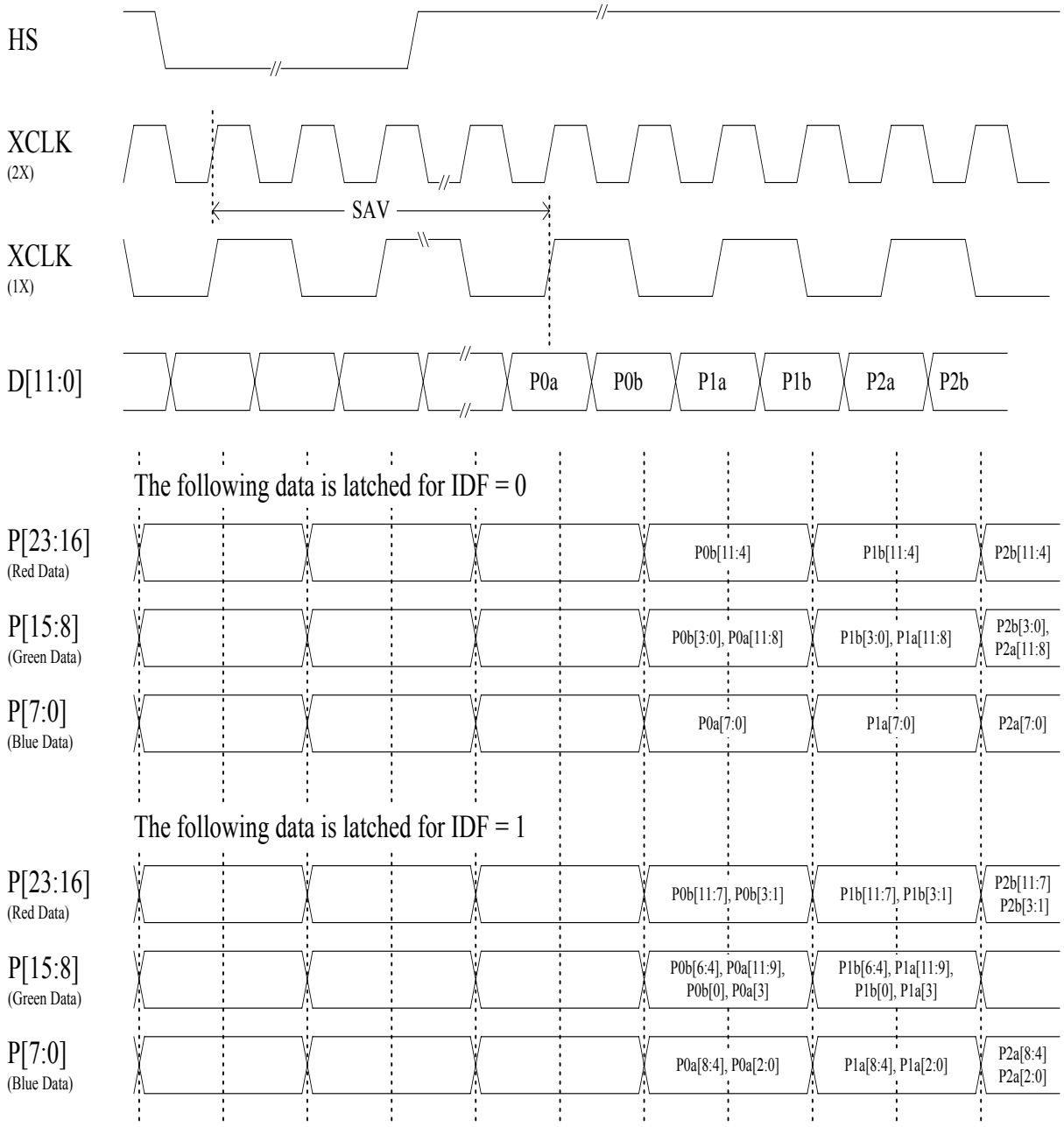

Figure 6. Multiplexed Input Data Formats (IDF = 0, 1)

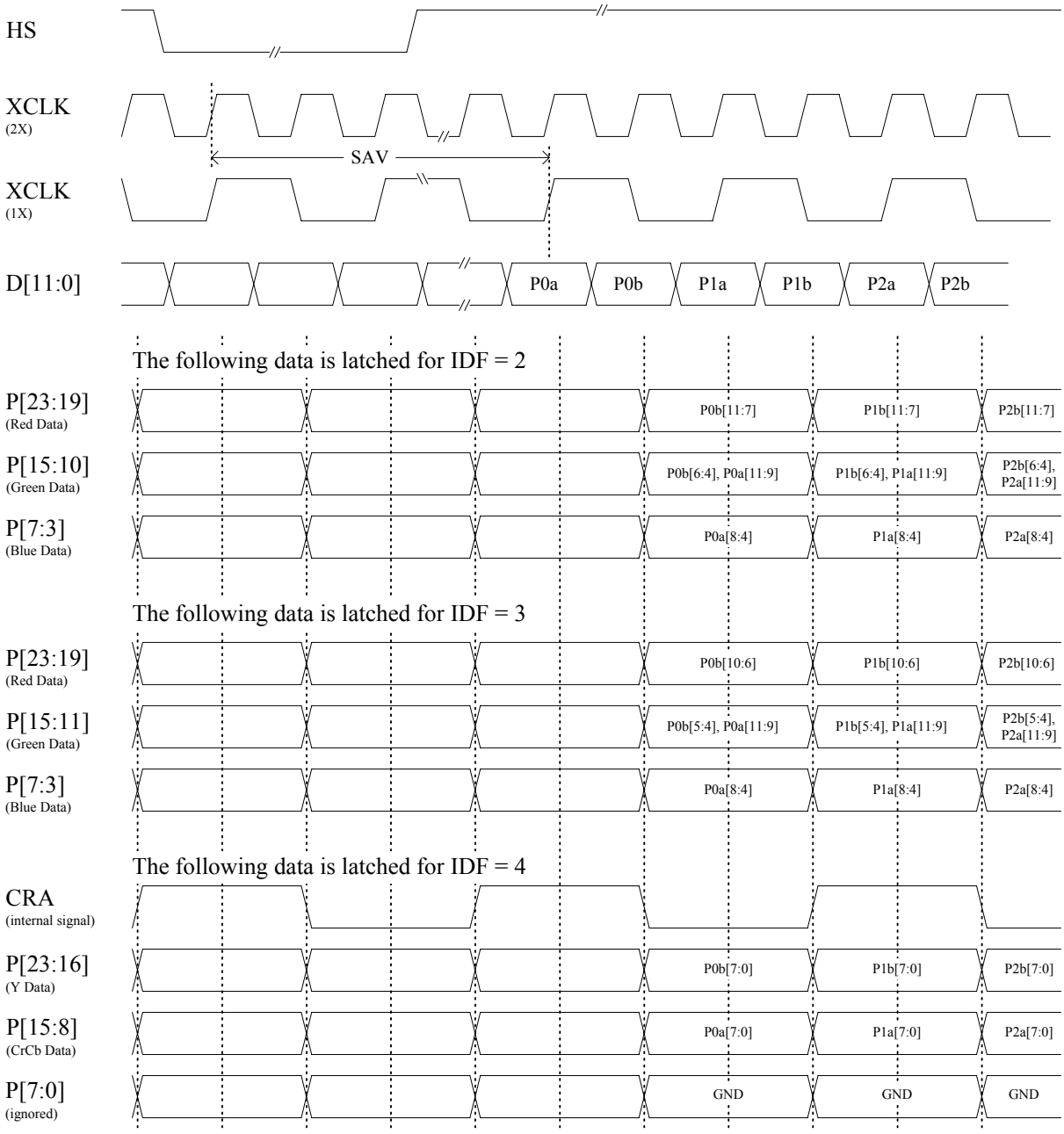

Figure 7. Multiplexed Input Data Formats (IDF = 2, 3, 4)

Table 4. Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB (12-12)				1 12-bit RGB (12-12)			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 5. Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 6. Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

When IDF = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

Table 7. Embedded Sync

IDF = Format =		4 YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	FF	00	00	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	FF	00	00	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	FF	00	00	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	FF	00	00	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	FF	00	00	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	FF	00	00	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	FF	00	00	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	FF	00	00	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7..0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1

S[5] = V = 1 during field blanking, 0 elsewhere

S[4] = H = 1 during EAV (synchronization reference at the end of active video)

0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3..0] are ignored.

5.3 NTSC and PAL Operation

Composite and S-Video outputs are supported in either NTSC or PAL format. The general parameters used to characterize these outputs are listed in **Table 9** and shown in **Figure 8**. (See **Figures 11** through **16** for illustrations of composite and S-Video output waveforms).

Table 8. NTSC/PAL Composite Output Timing Parameters (in ms)

Symbol	Description	Level (mV)		Duration (uS)	
A		**NTSC**	**PAL**	**NTSC**	**PAL**
A	Front Porch	287	300	1.49 - 1.51	1.48 - 1.51
B	Horizontal Sync	0	0	4.69 - 4.72	4.69 - 4.71
C	Breezeway	287	300	0.59 - 0.61	0.88 - 0.92
D	Color Burst	287	300	2.50 - 2.53	2.24 - 2.26
E	Back Porch	287	300	1.55 - 1.61	2.62 - 2.71
F	Black	340	300	0.00 - 7.50	0.00 - 8.67
G	Active Video	340	300	37.66 - 52.67	34.68 - 52.01
H	Black	340	300	0.00 - 7.50	0.00 - 8.67

1. Durations vary slightly in different modes due to the different clock frequencies used.
2. Active video and black (F, G, H) times vary greatly due to different scaling ratios used in different modes.
3. Black times (F and H) vary with position controls.

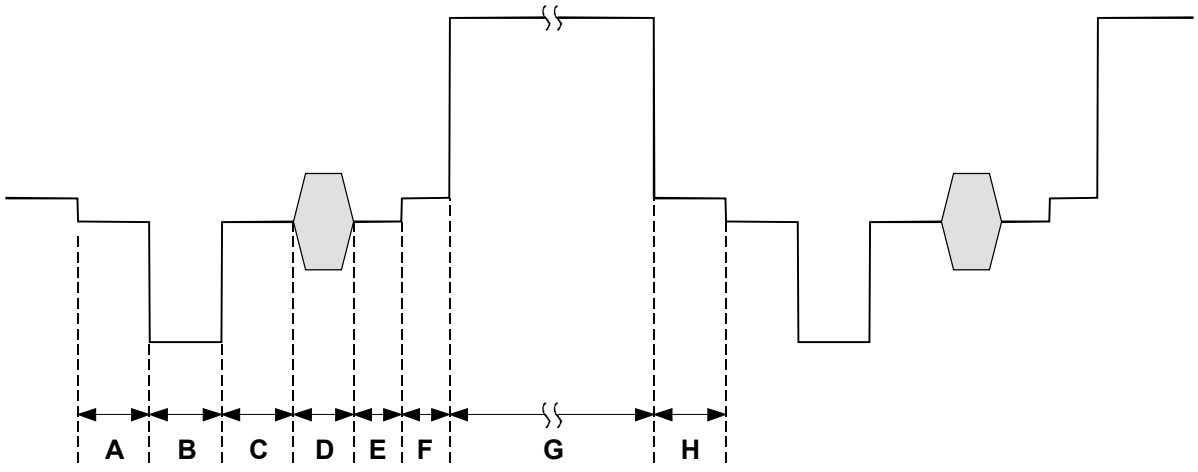

Figure 8. NTSC / PAL Composite Output

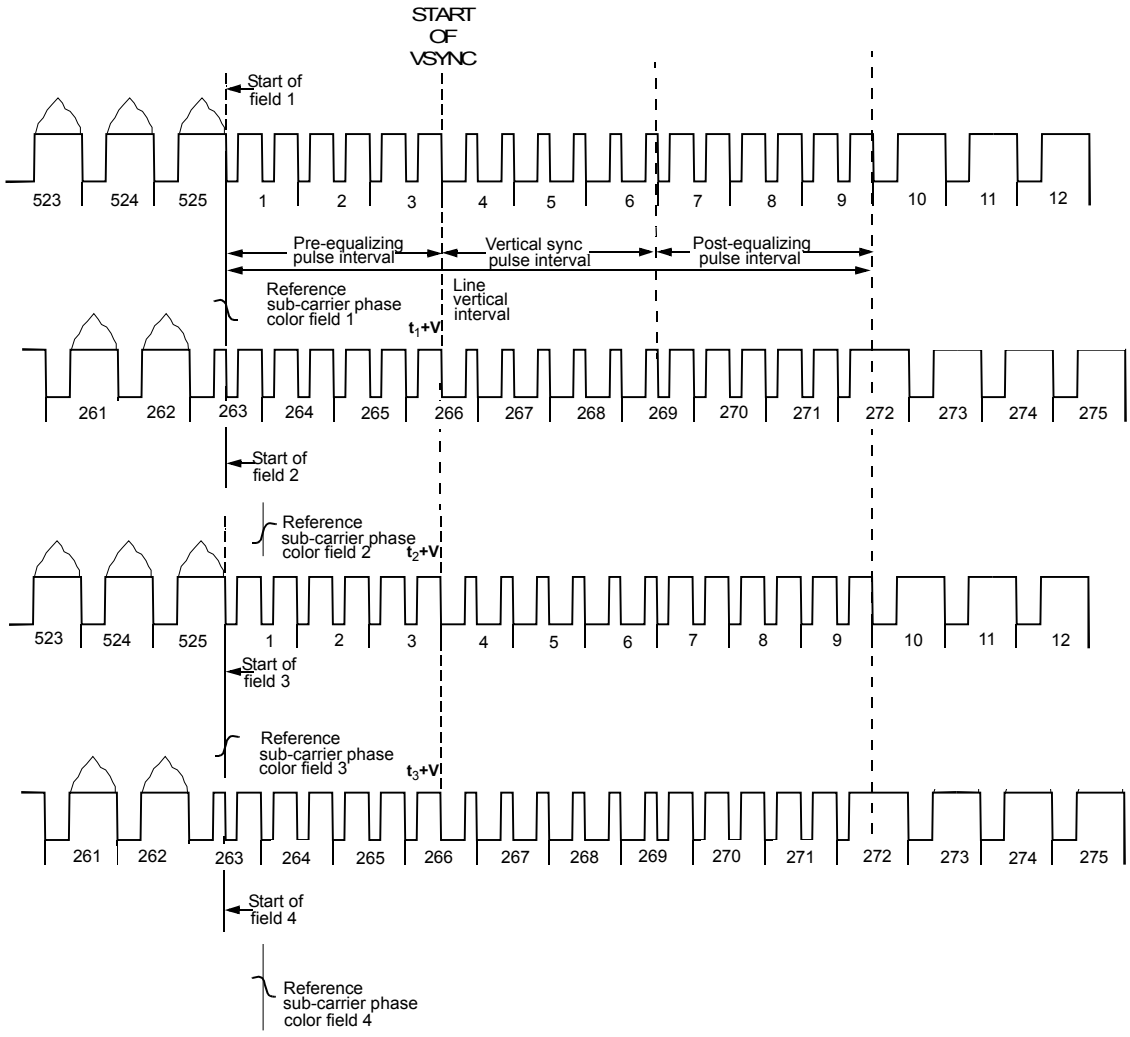

Figure 9. Interlaced NTSC Video Timing

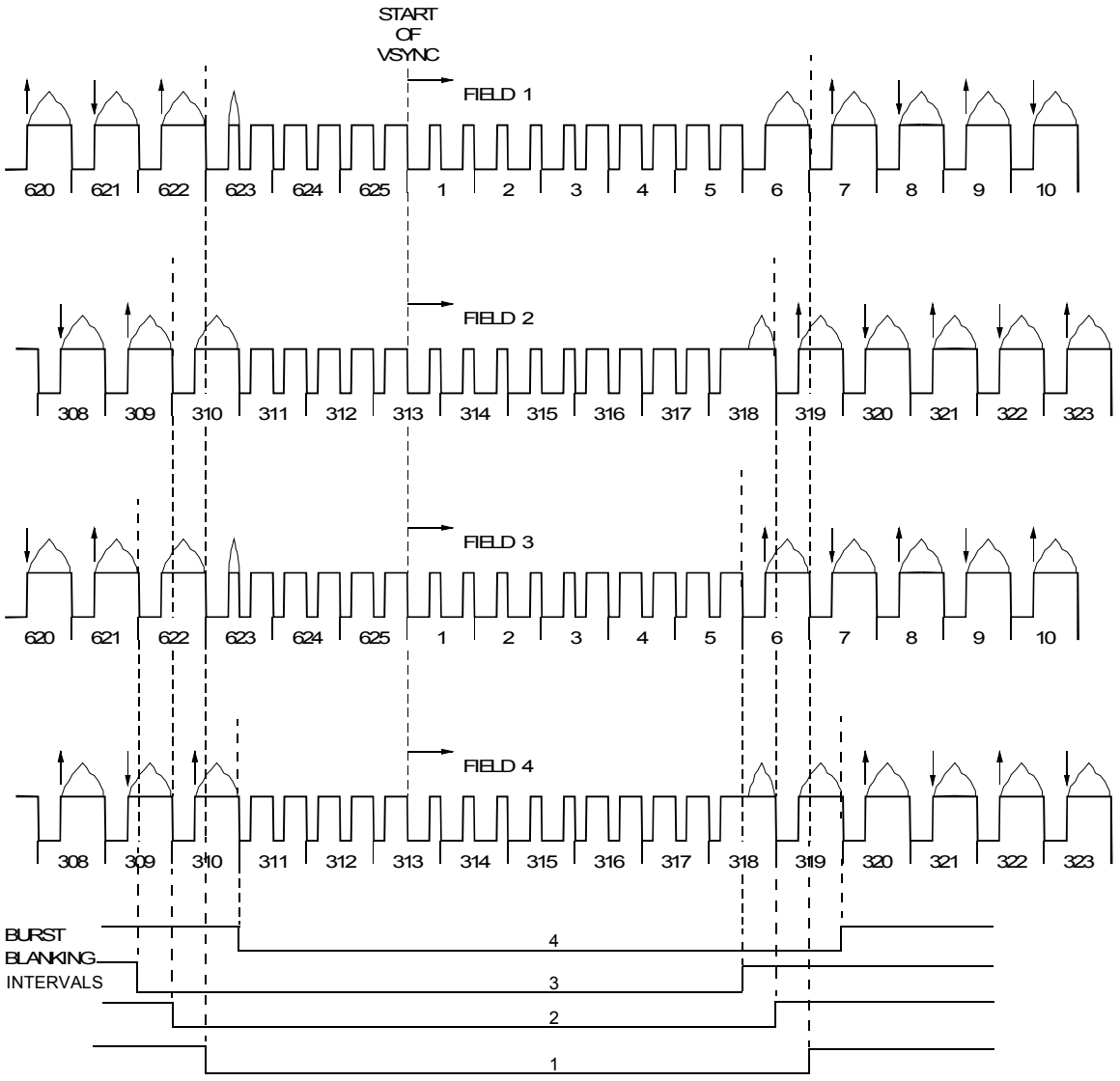

Figure 10. Interlaced PAL Video Timing

Color/Level	mA	V
White	26.66	1.000
Yellow	24.66	0.925
Cyan	21.37	0.801
Green	19.37	0.726
Magenta	16.22	0.608
Red	14.22	0.533
Blue	11.08	0.415
Black	9.08	0.340
Blank	7.65	0.287
Sync	0.00	0.000

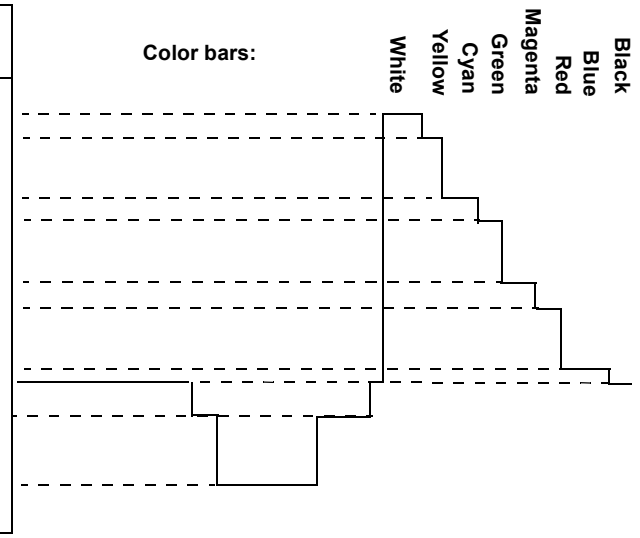

Figure 11. NTSC Y (Luminance) Output Waveform (DACG = 0)

Color/Level	mA	V
White	26.75	1.003
Yellow	24.62	0.923
Cyan	21.11	0.792
Green	18.98	0.712
Magenta	15.62	0.586
Red	13.49	0.506
Blue	10.14	0.380
Blank/ Black	8.00	0.300
Sync	0.00	0.000

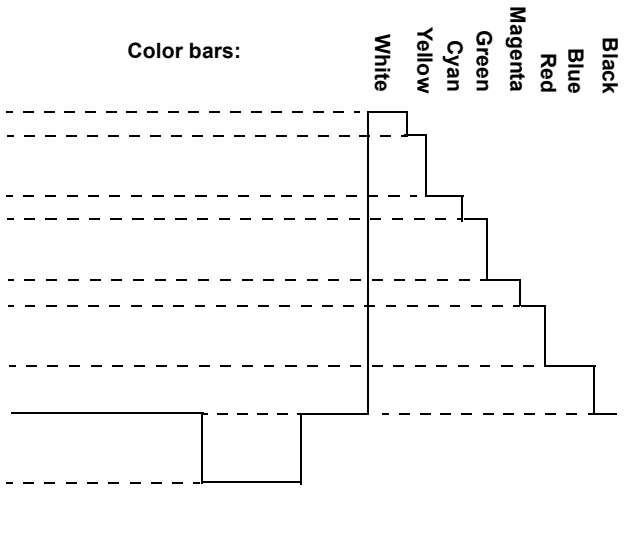

Figure 12. PAL Y (Luminance) Video Output Waveform (DACG = 1)

Color/Level	mA	V
Cyan/Red	25.80	0.968
Green/Magenta	25.01	0.938
Yellow/Blue	22.44	0.842
Peak Burst	18.08	0.678
Blank	14.29	0.536
Peak Burst	10.51	0.394
Yellow/Blue	6.15	0.230
Green/Magenta	3.57	0.134
Cyan/Red	2.79	0.105

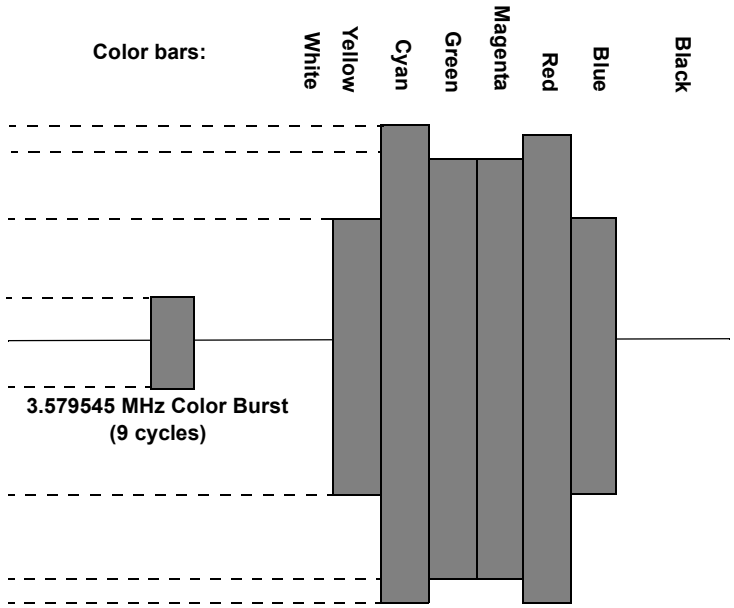

Figure 13. NTSC C (Chrominance) Video Output Waveform (DACG = 0)

Color/Level	mA	V
Cyan/Red	27.51	1.032
Green/Magenta	26.68	1.000
Yellow/Blue	23.93	0.897
Peak Burst	19.21	0.720
Blank	15.24	0.572
Peak Burst	11.28	0.423
Yellow/Blue	6.56	0.246
Green/Magenta	3.81	0.143
Cyan/Red	2.97	0.111

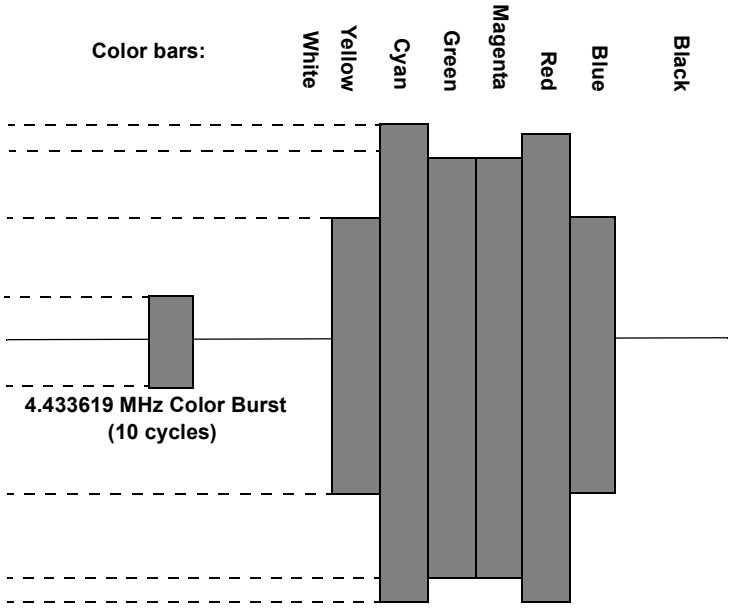

Figure 14. PAL C (Chrominance) Video Output Waveform (DACG = 1)

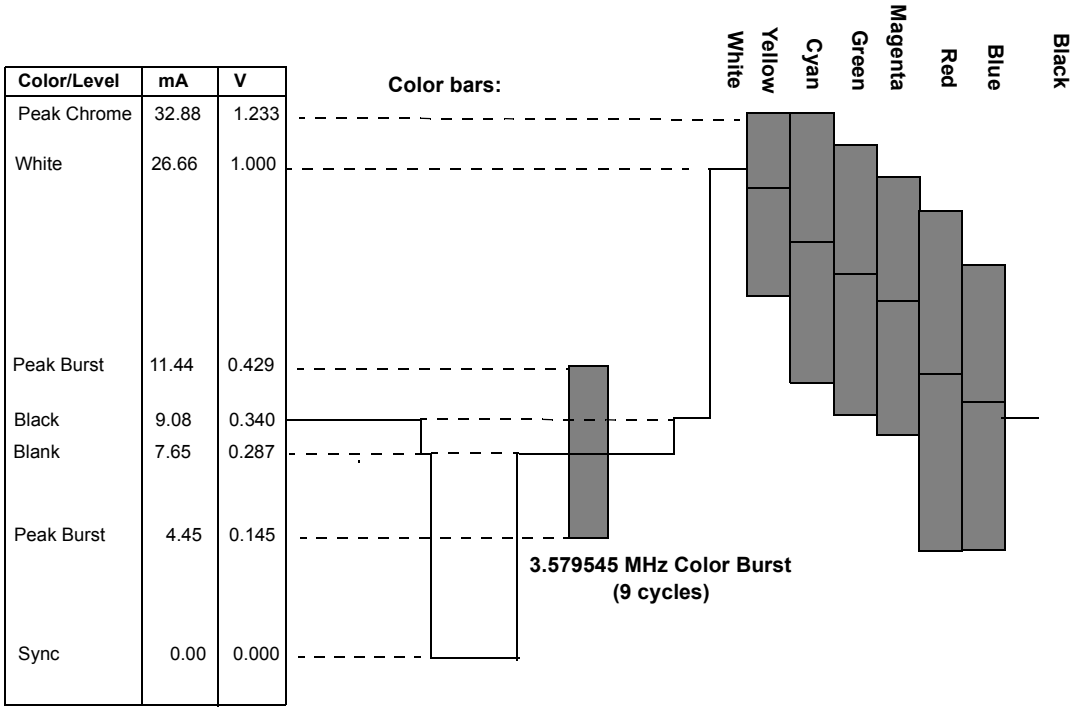

Figure 15. Composite NTSC Video Output Waveform (DACG = 0)

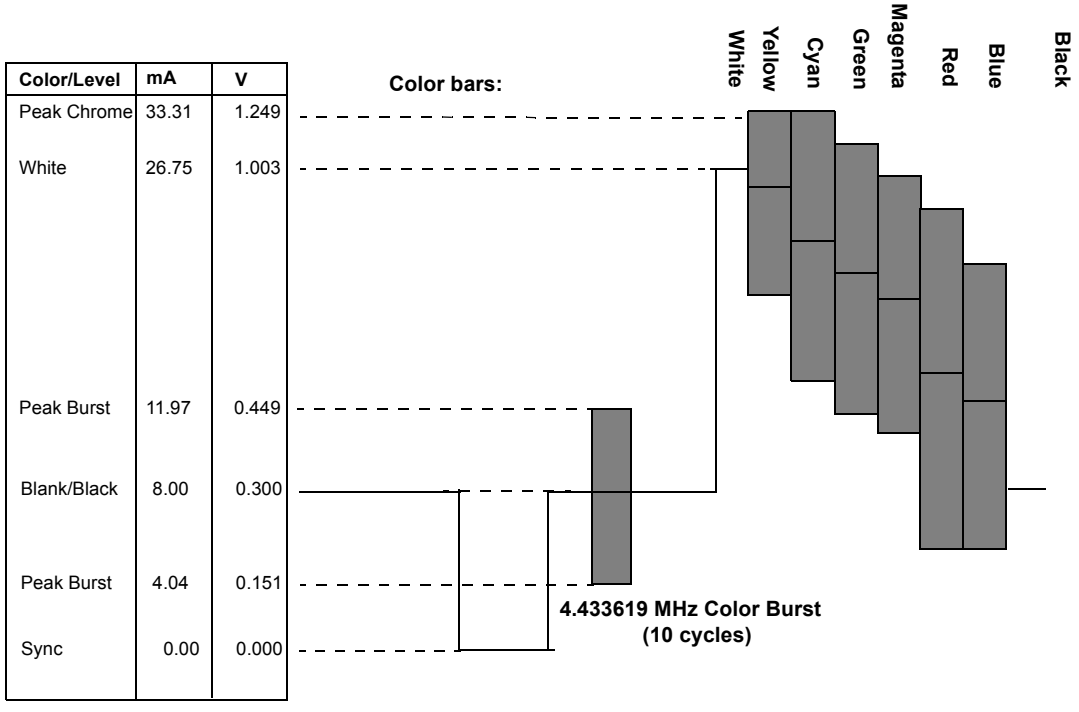

Figure 16. Composite PAL Video Output Waveform (DACG = 1)

5.4 Hot Plug Detection

The CH7010 has the capability of signaling to the graphics controller when the termination of the DVI outputs has changed. The operation of this circuit is as follows. The HPDET input pin of the CH7010 should be connected to pin 16 of the DVI connector. When a DVI monitor is connected to the DVI connector, this pin will be pulled high (above 2.4 volts). When a DVI monitor is not connected to the DVI connector, the internal pull-down on the HPDET pin will pull low. When the HPDET is low, the DVI output driver will be shut down. The CH7010 will detect any transition at the HPDET pin. When the HPIE (Hot Plug Interrupt Enable) bit in serial port register 1Eh is high, the CH7010 will pull low on the P-OUT / TLDET* pin. When the HPIE2 (Hot Plug Interrupt Enable 2) bit in serial port register 20h is high, the CH7010 will pull low on the GPIO[1] / TLDET* pin. This should signal the driver to read the DVIT bit in register 20h to determine the state of the HPDET pin. The P-OUT / TLDET pin will continue to pull low until the driver sets the HPIR (Hot Plug Interrupt Reset) bit in register 1Eh high. The driver should then set the HPIR bit low. In order to reset the HPIR bit high, DVIP and DVIL bits of register 49h[7:6] must first be set to '11'.

6. REGISTER CONTROL

The CH7010 is controlled via a serial port. The serial port bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device retains all register states.
The CH7010 contains a total of 37 registers for user control. A listing of non-Macrovision control bits is given below with a brief description of each.

6.1 Non-Macrovision Control Registers Map

The non-Macrovision controls are listed below, divided into four sections: general controls, input / output controls, DVI controls, and VGA to TV controls. A register map and register description follows.

• General Controls

ResetIB	Software serial reset
ResetDB	Software datapath reset
PD[7:0]	Power down controls (DVIP, DVIL, , TVD, DACPD[1:0], Full, Partial)
VID[7:0]	Version ID register
DID[7:0]	Device ID register
TSTP[1:0]	Enable/select test pattern generation (color bar, ramp)

• Input/Output Controls

XCM	XCLK 1X, 2X select
XCMD[7:0]	Delay adjust between XCLK and D[11:0]
MCP	XCLK polarity control
PCM	P-OUT 1X, 2X select
POUTP	P-OUT clock polarity
POUTE	P-OUT enable
HPIE, HPIE2	Hot plug detect interrupt enable
HPIR	Hot plug detect interrupt reset
IDF[2:0]	Input data format
IBS	Input buffer select
DES	Decode embedded sync (TV-Out data only)
SYO	H/V sync direction control (for TV-Out modes only)
VSP	V sync polarity control (sync polarity to DVI is not changed)
HSP	H sync polarity control (sync polarity to DVI is not changed)
TERM[5:0]	Termination detect/check (DVI, DACT3, DACT2, DACT1, DACT0, SENSE)
BCOEN	Enable BCO Output
BCO[2:0]	Select output signal for BCO pin
BCOP	BCO polarity
GPIOL[1:0]	Read or write level for GPIO pins
GOENB[1:0]	Direction control for GPIO pins
SYNCO[1:0]	Enables/selects sync output for Scart and bypass modes
DACG[1:0]	DAC gain control
DACBP	DAC bypass
XOSC[2:0]	Crystal oscillator adjustments

• DVI Controls

TPPD[2:0]	DVI PLL phase detector trim
TPCP[1:0]	DVI PLL charge pump trim
TPVT[5:0]	DVI PLL VDD trim
TPVCO[10:0]	DVI PLL VCO trim
TPD[5:0]	DVI PLL divider
TLPF[3:0]	DVI PLL low pass filter
DVID[3:0]	DVI transmitter drive strength
CTL[3:0]	DVI control inputs
TERM [2]	DVI hot plug detection

• TV-Out Controls

IR[2:0]	Input data resolution (when used for TV-Out)
VOS[1:0]	TV-Out video standard
SR[2:0]	TV-Out scaling ratio
CFF[1:0]	Chroma flicker filter setting
YFFT[1:0]	Luma text enhancement flicker filter setting
YFFNT[1:0]	Luma flicker filter setting (Non-text)
CVBWB	CVBS DAC receives black&white (S-Video luminance) signal
CBW	Chroma video bandwidth
YSV[1:0]	S-Video luma bandwidth
YCV[1:0]	Composite video luma bandwidth
TE[2:0]	Text enhancement (sharpness)
CFRB	Chroma sub-carrier free run (bar) control
M/S*	TV-Out PLL reference input control
SAV [8:0]	Horizontal start of active video (delay from leading edge of H sync to active video)
BLCK[7:0]	TV-Out Black level control
HP[8:0]	TV-Out horizontal position control
VP[8:0]	TV-Out vertical position control
VOF	TV-Out video format (s-video & composite, RGB)
CE[2:0]	TV-Out contrast enhancement
PLLTVM[8:0]	TV-Out PLL M divider
PLLTVN[9:0]	TV-Out PLL N divider
FSCI[32:0]	Sub-carrier generation increment value (when ACIV=0)
CIVEN	Calculated sub-carrier enable (was called ACIV)
CIVC[1:0]	Calculated sub-carrier control (hysteresis,
CIV[25:0]	Calculated sub-carrier increment value read out
CIVPN	Select PAL-Nc (Argentina) when in a CIV mode
MEM[2:0]	Memory sense amp reference adjust
VBID	Vertical blanking interval defeat
PLLCPI	TV-Out PLL charge pump current control
PLLCAP	TV-Out PLL capacitor control

6.2 Registers Read/Write

Regarding the CH7010 registers read/write operation, please see applications note AN-41 for details.

6.3 Non-Macrovision Control Registers Description

Table 9. Serial Port Register Map w/o Macrovision

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
01h		VOF0	CFF1	CFF0	YFFT1	YFFT0	YFFNT1	YFFNT0
02h	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
03h			SAV8	HP8	VP8	TE2	TE1	TE0
04h	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
05h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
06h	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
07h	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08h						CE2	CE1	CE0
09h	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
0Ah	M7	M6	M5	M4	M3	M2	M1	M0
0Bh	N7	N6	N5	N4	N3	N2	N1	N0
0Ch	FSCI31	FSCI30	FSCI29	FSCI28	FSCI27	FSCI26	FSCI25	FSCI24
0Dh	FSCI23	FSCI22	FSCI21	FSCI20	FSCI19	FSCI18	FSCI17	FSCI16
0Eh	FSCI15	FSCI14	FSCI13	FSCI12	FSCI11	FSCI10	FSCI9	FSCI8
0Fh	FSCI7	FSCI6	FSCI5	FSCI4	FSCI3	FSCI2	FSCI1	FSCI0
10h			CIV25	CIV24	CIVC1	CIVC0	PALN	CIVEN
11h	CIV23	CIV22	CIV21	CIV20	CIV19	CIV18	CIV17	CIV16
12h	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8
13h	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0
1Ch					M/S*	MCP	PCM	XCM
1Dh					XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	HPIE	POUTE	POUTP
1Fh	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
20h	HPIE2	XOSC2	DVIT	DACT3	DACT2	DACT1	DACT0	SENSE
21h	XOSC1	XOSC0		SYNCO1	SYNCO0	DACG1	DACG0	DACBP
22h	SHF2	SHF1	SHF0	BCOEN	BCOP	BCO2	BCO1	BCO0
23h						HPDD		
31h	TPPD3	TPPD2	TPPD1	TPPD0	CTL3	CTL2	CTL1	CTL0
32h	TPVCO7	TPVCO6	TPVCO5	TPVCO4	TPVCO3	TPVCO2	TPVCO1	TPVCO0
33h	DVID2	DVID1	DVID0		TPPSD1	TPPSD0	TPCP1	TPCP0
34h			TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
35h			TPVT5	TPVT4	TPVT3	TPVT2	TPVT1	TPVT0
36h	TPLPF3	TPLPF2	TPLPF1	TPLPF0				
37h	TPVCO10	TPVCO9	TPVCO8					
48h				ResetIB	ResetDB			
49h	DVIP	DVIL	TV	DACPD3	DACPD2	DACPD1	DACPD0	FPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

All register bits not defined in the register map are reserved bits, and should be left at the default value.

Table 9 shows the CH7010 non-Macrovision register map. The details are described as follows:

Display Mode Register

Symbol: **DM**

Address: **00h**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	0	1	0	1	0

Register DM provides programmable control of the CH7010 VGA to TV display mode, including input resolution (IR[2:0]), video output standard (VOS[1:0]), and scaling ratio (SR[2:0]). The mode of operation is determined according to **Table 10** below. For entries in which the output standard is shown as PAL, PAL-B,D,G,H,I,N,N_C can be supported through proper selection of the chroma sub-carrier. For entries in which the output standard is shown as NTSC, NTSC-M, J and PAL-M can be supported through proper selection of VOS[1:0] and chroma sub-carrier.

Table 10. Display Mode

Mode	IR[2:0]	VOS [1:0]	SR[2:0]	Input Data Format (Active Video)	Total Pixels/Line x Total Lines/Frame	Output Standard [TV Standard]	Scaling	Percent Overscan	Pixel Clock (MHz)
0	000	00	000	512x384	840x500	PAL	5/4	-17	21.000000
1	000	00	001	512x384	840x625	PAL	1/1	-33	26.250000
2	000	01	000	512x384	800x420	NTSC	5/4	0	20.139860
3	000	01	001	512x384	784x525	NTSC	1/1	-20	24.671329
4	001	00	000	720x400	1125x500	PAL	5/4	-13	28.125000
5	001	00	001	720x400	1152x625	PAL	1/1	-30	36.000000
6	001	01	000	720x400	945x420	NTSC	5/4	+4	23.790210
7	001	01	001	720x400	936x525	NTSC	1/1	-16	29.454545
8	010	00	000	640x400	1000x500	PAL	5/4	-13	25.000000
9	010	00	001	640x400	1008x625	PAL	1/1	-30	31.500000
10	010	01	000	640x400	840x420	NTSC	5/4	+4	21.146854
11	010	01	001	640x400	832x525	NTSC	1/1	-17	26.181819
12	010	01	010	640x400	840x600	NTSC	7/8	-27	30.209791
13	011	00	000	640x480	840x500	PAL	5/4	+4	21.000000
14	011	00	001	640x480	840x625	PAL	1/1	-17	26.250000
15	011	00	011	640x480	840x750	PAL	5/6	-30	31.500000
16	011	01	001	640x480	784x525	NTSC	1/1	0	24.671329
17	011	01	010	640x480	784x600	NTSC	7/8	-13	28.195805
18	011	01	011	640x480	800x630	NTSC	5/6	-18	30.209790
19	100	01	001	720x480	882x525	NTSC	1/1	0	27.755245
20	100	01	010	720x480	882x600	NTSC	7/8	-13	31.720280
21	100	01	011	720x480	900x630	NTSC	5/6	-18	33.986015
22	101	00	001	720x576	882x625	PAL	1/1	0	27.562500
23	101	00	011	720x576	900x750	PAL	5/6	-18	33.750000
24	101	00	100	720x576	900x875	PAL	5/7	-30	39.375000
25	110	00	001	800x600	944x625	PAL	1/1	+4	29.500000
26	110	00	011	800x600	960x750	PAL	5/6	-14	36.000000
27	110	00	100	800x600	960x875	PAL	5/7	-27	42.000000
28	110	01	110	800x600	1040x700	NTSC	3/4	-6	43.636364
29	110	01	111	800x600	1064x750	NTSC	7/10	-14	47.832169
30	110	01	101	800x600	1040x840	NTSC	5/8	-22	52.363637
31	111	00	100	1024x768	1400x875	PAL	5/7	-4	61.250000
32	111	00	101	1024x768	1400x1000	PAL	5/8	-16	70.000000
33	111	00	110	1024x768	1400x1125	PAL	5/9	-25	78.750000
34	111	01	101	1024x768	1160x840	NTSC	5/8	0	58.405595
35	111	01	110	1024x768	1160x945	NTSC	5/9	-10	65.706295
36	111	01	111	1024x768	1168x1050	NTSC	1/2	-20	73.510491
37	101	00	000	720x576	864x625	PAL	1/1	0	13.500000
38	100	01	000	720x480	858x525	NTSC	1/1	0	13.500000

Table 11. Video Output Standard Selection

VOS[1:0]	00	01	10	11
Output Format	PAL	NTSC	PAL-M	NTSC-J

Flicker Filter Register

Symbol: **FF**

Address: **01h**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL		VOF	CFF1	CFF0	YFFT1	YFFT0	YFFNT1	YFFNT0
TYPE		R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT		0	1	0	0	1	1	1

Bits 1-0 of register FF control the filter used in the scaling and flicker reduction block applied to the non-text portion of the luminance signal as shown in **Table 12** below.

Bits 3-2 of register FF control the filter used in the scaling and flicker reduction block applied to the text portion of the luminance signal as shown in **Table 12** below.

Bits 5-4 of register FF control the filter used in the scaling and flicker reduction block applied to the chrominance signal as shown in **Table 13** below. A setting of '11' applies a dot crawl reduction filter which can reduce the 'hanging dots' effect of an NTSC composite video signal when displayed on a TV with a comb filter.

Table 12. Luma Flicker Filter Control

	YFFT and YFFNT Flicker Filter Settings (lines)			
Scaling Ratio	00	01	10	11
5/4	2	3	3	3
1/1, 7/8, 5/6, 3/4, 5/7, 7/10	2	3	4	5
5/8	2	3	4	6
5/9	3	4	5	6
1/2	3	5	5	7

Table 13. Chroma Flicker Filter Control

	CFF Flicker Filter Settings (lines)			
Scaling Ratio	00	01	10	11
5/4	2	3	3	3
1/1, 7/8, 5/6, 3/4, 5/7, 7/10	2	3	4	5
5/8	2	3	4	5
5/9	3	4	5	6
1/2	3	5	5	7

Bit 6 of register FF controls the video output format. A value of '0' generates composite and S-Video outputs. A value of '1' generates RGB outputs.

Video Bandwidth Register

Symbol: **VBW**

Address: **02h**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	1	1	1	1	0

YCV[1:0] (bits 1-0) of register VBW control the filter used to limit the bandwidth of the luma signal in the CVBS output signal. A table of –3dB bandwidth values is given below.

YSV[1:0] (bits 3-2) of register VBW control the filter used to limit the bandwidth of the luma signal in the S-Video output signal. A table of –3dB bandwidth values is given below.

CBW (bit 4) of register VBW controls the filter used to limit the bandwidth of the chroma signal in the CVBS and S-Video output signals. A table of –3dB bandwidth values is given below.

Bit 5 of register VBW controls the signal output on the CVBS signal. CVBW = '0' disables the chroma signal being added to the CVBS signal, CVBW = '1' enables the chroma signal being added to the CVBS signal.

Table 14. Video Bandwidth

Mode	CBW		YSV[1:0] and YCV[1:0]			
	0	1	00	01	10	11
0	0.620	0.856	2.300	2.690	3.540	5.880
1	0.775	1.070	2.880	3.360	4.430	7.350
2	0.529	0.730	1.960	2.290	3.020	5.010
3	0.648	0.894	2.410	2.810	3.700	6.140
4	0.831	1.150	3.080	3.600	4.750	7.870
5	1.060	1.470	3.950	4.610	6.080	10.100
6	0.703	0.970	2.610	3.040	4.010	6.660
7	0.870	1.200	3.230	3.770	4.970	8.240
8	0.738	1.020	2.740	3.200	4.220	7.000
9	0.930	1.280	3.460	4.030	5.320	8.820
10	0.624	0.862	2.320	2.710	3.570	5.920
11	0.773	1.070	2.870	3.350	4.420	7.330
12	0.892	1.230	3.310	3.870	5.100	8.450
13	0.620	0.856	2.300	2.690	3.540	5.880
14	0.775	1.070	2.880	3.360	4.430	7.350
15	0.930	1.280	3.460	4.030	5.320	8.820
16	0.648	0.894	2.410	2.810	3.700	6.140
17	0.740	1.020	2.750	3.210	4.230	7.010
18	0.793	1.100	2.950	3.440	4.530	7.510
19	0.729	1.010	2.710	3.160	4.160	6.900
20	0.833	1.150	3.090	3.610	4.760	7.890
21	0.892	1.230	3.310	3.870	5.100	8.450
22	0.724	0.999	2.690	3.140	4.130	6.860
23	0.886	1.220	3.290	3.840	5.060	8.400
24	1.030	1.430	3.840	4.480	5.910	9.790
25	0.774	1.070	2.880	3.360	4.430	7.340
26	0.945	1.310	3.510	4.100	5.400	8.960
27	1.100	1.520	4.100	4.780	6.300	10.400
28	0.859	1.190	3.190	3.720	4.910	8.140
29	0.942	1.300	3.500	4.080	5.380	8.920
30	1.030	1.420	3.830	4.470	5.890	9.770
31	0.804	1.110	2.990	3.480	4.590	7.620
32	0.919	1.270	3.410	3.980	5.250	8.710
33	1.030	1.430	3.840	4.480	5.910	9.790
34	0.767	1.060	2.850	3.320	4.380	7.260
35	0.862	1.190	3.200	3.740	4.930	8.170
36	0.965	1.330	3.580	4.180	5.510	9.140
37	0.709	0.979	2.630	3.070	4.050	6.720
38	0.466	0.643	1.730	2.020	2.660	4.410

Bit 6 of register VBW controls whether the chroma sub-carrier free-runs, or is locked to the video signal. A '1' causes the sub-carrier to lock to the TV vertical rate, and should be used when the CIVEN bit (register 10h) is set to '0'. A '0' causes the sub-carrier to free-run, and should be used when the CIVEN bit is set to '1'.

Bit 7 of register VBW controls the vertical blanking interval defeat function. A '1' in this register location forces the flicker filter to minimum filtering during the vertical blanking interval. A '0' in this location causes the flicker filter to

remain at the same setting inside and outside of the vertical blanking interval.

Text Enhancement Register

Symbol: **TE**
Address: **03h**
Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL			SAV8	HP8	VP8	TE2	TE1	TE0
TYPE			R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT			0	0	0	1	0	1

Bits 2-0 of register TE control the text enhancement circuitry within the CH7010. A value of '000' minimizes the enhancement feature, while a value of '111' maximizes the enhancement.

Bits 5-3 of register TE contain the MSB values for the start of active video, horizontal position and vertical position controls. They are described in detail in the SAV, HP and VP register descriptions.

Start of Active Video Register

Symbol: **SAV**
Address: **04h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	1	0	0	0	0

Register SAV controls the delay, in pixel increments, from leading edge of horizontal sync to start of active video. The entire bit field SAV[8:0] is comprised of this register SAV[7:0], plus the MSB value contained in the Text Enhancement register, bit SAV8. This is decoded as a whole number of pixels, which can be set anywhere between 0 and 511 pixels. Therefore, in any 2X clock mode the number of 2X clocks from the leading edge of sync to the first active data must be a multiple of two clocks.

Horizontal Position Register

Symbol: **HP**
Address: **05h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	0	1	0	0	0	0

Register HP is used to shift the displayed TV image in a horizontal direction (left or right) to achieve a horizontally centered image on screen. The entire bit field, HP[8:0], is comprised of this register HP[7:0] plus the MSB value contained in the Text Enhancement register, bit HP8. Increasing values move the displayed image position right, and decreasing values move the image position left.

Vertical Position Register

Symbol: **VP**
Address: **06h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Register VP is used to shift the displayed TV image in a vertical direction (up or down) to achieve a vertically centered image on screen. The entire bit field, VP[8:0], is comprised of this register HP[7:0] plus the MSB value contained in the Text Enhancement register, bit VP8. The value represents the TV line number (relative to the VGA vertical sync) used to initiate the generation and insertion of the TV vertical interval (i.e. the first sequence of equalizing pulses). Increasing values delay the output of the TV vertical sync, causing the image position to move up on the TV screen. Decreasing values, therefore, move the image position DOWN. Each increment moves the image position by one TV lines (approximately 2 input lines). The maximum value that should be programmed into the VP[8:0] value is the number of TV lines per field minus one half (262 or 312). When panning the image up, the number should be increased until (TVLPF-1/2) is reached, the next step should be to reset the register to zero. When panning the image down the screen, decrement the VP[8:0] value until the value zero is reached. The next step should set the register to TVLPF-1/2, and then decrement for further changes.

Black Level Register

Symbol: **BL**

Address: **07h**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	1	1

Register BL controls the black level. The luminance data is added to this black level, which must be set between 51 and 208. When the input data format is zero through three the default values are 131 for NTSC and PAL-M, 110 for PAL and 102 for NTSC-J. When the input data format is four the default values are 112 for NTSC and PAL-M, 94 for PAL and 88 for NTSC-J.

Contrast Enhancement Register

Symbol: **CE**

Address: **08h**

Bits: **3**

BIT	7	6	5	4	3	2	1	0
SYMBOL						CE2	CE1	CE0
TYPE						R/W	R/W	R/W
DEFAULT						0	1	1

Bits 2-0 of register CE control contrast enhancement feature of the CH7010, according to the figure below. A setting of '0' results in reduced contrast, a setting of '1' leaves the image contrast unchanged, and values beyond '1' result in increased contrast.

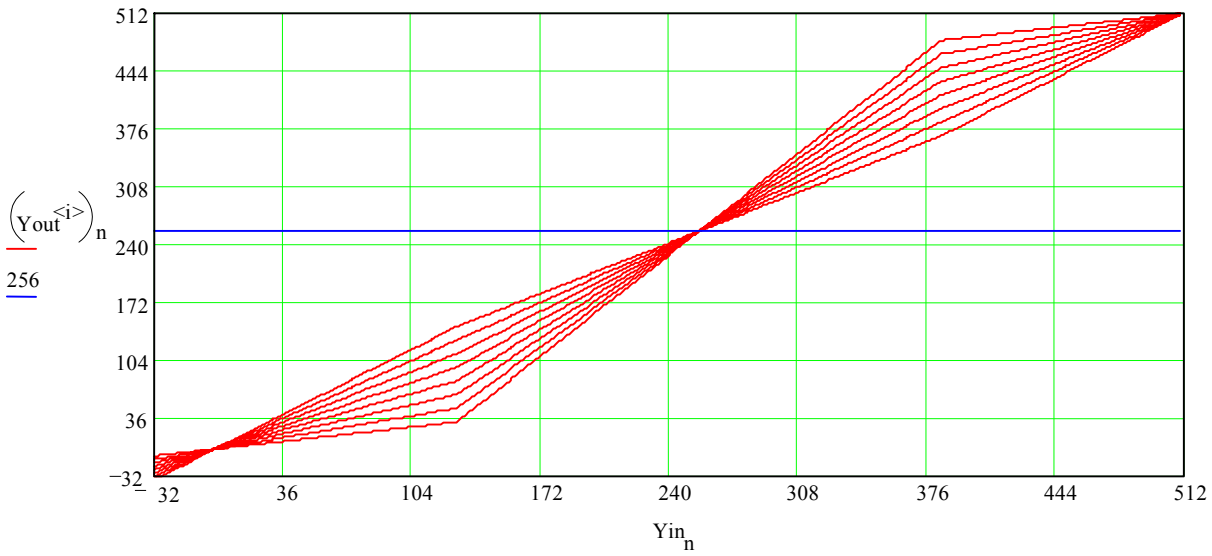

Figure 17. Contrast Enhancement diagram

TV PLL Control Register

Symbol: **TPC**

Address: **09h**

Bits: **5**

BIT	7	6	5	4	3	2	1	0
SYMBOL	MEM2	MEM1	IBI	N9	N8	M8	PLLCPI	PLLCAP
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bit 0 of register TPC controls the TV PLL loop filter capacitor. A recommended listing of PLLCAP setting versus mode is listed in **Table 15** below.

Table 15. PLLCAP setting vs Display Mode

Mode	PLLCAP Value	Mode	PLLCAP Value
0	1	20	0
1	1	21	0
2	0	22	1
3	0	23	1
4	1	24	1
5	1	25	0
6	0	26	1
7	1	27	1
8	0	28	1
9	1	29	0
10	0	30	1
11	1	31	1
12	0	32	1
13	1	33	1
14	1	34	0
15	1	35	0
16	0	36	0
17	0	37	1
18	0	38	1
19	0		

Bit 1 of register TPC should be left at the default value.

Bits 4-2 of register TPC contain the MSB values for the TV PLL divider ratio's. These controls are described in detail in the PLLM and PLLN register descriptions.

Bit 5 of register TPC controls the input latch bias current. The default value is recommended.

Bits 7-6 of register TPC control the memory sense amp reference level. The default value is recommended.

TV PLL M Value Register

Symbol: **PLLM**

Address: **0Ah**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	M7	M6	M5	M4	M3	M2	M1	M0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	1	1	1	1

Register PLLM controls the division factor applied to the 14.31818MHz frequency reference clock before it is input to the TV PLL phase detector when the CH7010 is operating in master clock mode. The entire bit field, M[8:0], is comprised of this register M[7:0] plus the MSB value contained in the TV PLL Control register, bit M8. In slave clock mode, an external pixel clock is used instead of the 14.31818MHz frequency reference, and the division factor is determined by the XCM value in register 1Dh. A table of values versus display mode is given following the PLLN register description.

TV PLL N Value Register

Symbol: **PLLN**

Address: **0Bh**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	N7	N6	N5	N4	N3	N2	N1	N0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	1	1	1	1	0

Register PLLN controls the division factor applied to the VCO output before being applied to the PLL phase detector, when the CH7010 is operating in master clock mode. The entire bit field, N[9:0], is comprised of this register N[7:0] plus N[9:8] contained in the TV PLL Control register (09h, bits 3 and 4). In slave clock mode, the value of 'N' is internally set to 1. The pixel clock generated in clock master modes is calculated according to the equation Fpixel = Fref * [(N+2) / (M+2)]. When using a 14.31818MHz frequency reference, the required M and N values for each mode are shown in **Table 16** below:

Table 16. TV PLL M and N values vs Display Mode

Mode	VGA Resolution, TV Standard, Scaling Ratio	N 10-bits	M 9-bits	Mode	VGA Resolution, TV Standard, Scaling Ratio	N 10-bits	M 9-bits
0	512x384, PAL, 5:4	20	13	20	720x480, NTSC, 7:8	142	63
1	512x384, PAL, 1:1	9	4	21	720x480, NTSC, 5:6	214	89
2	512x384, NTSC, 5:4	126	89	22	720x480, PAL, 1:1	75	38
3	512x384, NTSC, 1:1	110	63	23	720x480, PAL, 5:6	31	12
4	720x400, PAL, 5:4	53	26	24	720x480, PAL, 5:7	9	2
5	720x400, PAL, 1:1	86	33	25	800x600, PAL, 1:1	647	313
6	720x400, NTSC, 5:4	106	63	26	800x600, PAL, 5:6	86	33
7	720x400, NTSC, 1:1	70	33	27	800x600, PAL, 5:7	42	13
8	640x400, PAL, 5:4	108	61	28	800x600, NTSC, 3:4	62	19
9	640x400, PAL, 1:1	9	3	29	800x600, NTSC, 7:10	302	89
10	640x400, NTSC, 5:4	94	63	30	800x600, NTSC, 5/8	126	33
11	640x400, NTSC, 1:1	62	33	31	1024x768, PAL, 5:7	75	16
12	640x400, NTSC, 7:8	190	89	32	1024x768, PAL, 5:8	42	7
13	640x480, PAL, 5:4	20	13	33	1024x768, PAL, 5:9	20	2
14	640x480, PAL, 1:1	9	4	34	1024x768, NTSC, 5:8	565	137
15	640x480, PAL, 5:6	9	3	35	1024x768, NTSC, 5:9	333	71
16	640x480, NTSC, 1:1	110	63	36	1024x768, NTSC, 1:2	917	177
17	640x480, NTSC, 7:8	126	63	37	720x576, PAL, 1:1	31	33
18	640x480, NTSC, 5:6	190	89	38	720x480, NTSC, 1:1	31	33
19	720x480, NTSC, 1:1	124	63				

Sub-carrier Value Register

Symbol: **FSCI**
Address: **0Ch – 0Fh**
Bits: **8 each**

BIT	7	6	5	4	3	2	1	0
SYMBOL	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT								

Registers FSCI contain a 32-bit value which is used as an increment value for the ROM address generation circuitry when CIVEN=0. The bit locations are specified as follows:

Register	Contents
0Ch	FSCI[31:24]
0Dh	FSCI[23:16]
0Eh	FSCI[15:8]
0Fh	FSCI[7:0]

When the CH7010 is used in the master clock mode, the tables below should be used to set the FSCI registers. When using these values, the CIVEN bit in register 10h should be set to '0', and the CFRB bit in register 02h should be set to '1'.

Table 17. FSCI Values (525-Line TV-Out Modes)

Mode	NTSC **"Normal Dot Crawl"**	NTSC **"No Dot Crawl"**	PAL-M **"Normal Dot Crawl"**
2	763,363,328	763,366,524	762,524,467
3	623,153,737	623,156,346	622,468,953
6	574,429,782	574,432,187	573,798,541
7	463,962,517	463,964,459	463,452,668
10	646,233,505	646,236,211	645,523,358
11	521,957,831	521,960,019	521,384,251
12	452,363,454	452,365,347	451,866,351
16	623,153,737	623,156,346	622,468,953
17	545,259,520	545,261,803	544,660,334
18	508,908,885	508,911,016	508,349,645
19	553,914,433	553,916,752	553,305,736
20	484,675,129	484,677,158	484,142,519
21	452,363,454	452,365,347	451,866,351
28	469,762,048	469,764,015	469,245,826
29	428,554,851	428,556,645	428,083,911
30	391,468,373	391,470,012	391,038,188
34	526,457,468	526,459,671	525,878,943
35	467,962,193	467,964,152	467,447,949
36	418,281,276	418,283,027	417,821,626
38	569,408,543	569,410,927	568,782,819

Table 18. FSCI Values (625-Line TV-Out Modes)

Mode	PAL **"Normal Dot Crawl"**	PAL-Nc (Argentina) **"Normal Dot Crawl"**
0	806,021,060	651,209,077
1	644,816,848	520,967,262
4	601,829,058	486,236,111
5	470,178,951	379,871,962
8	677,057,690	547,015,625
9	537,347,373	434,139,385
13	806,021,060	651,209,077
14	644,816,848	520,967,262
15	537,347,373	434,139,385
22	690,875,194	558,179,209
23	564,214,742	455,846,354
24	483,612,636	390,725,446
25	645,499,916	521,519,134
26	528,951,320	427,355,957
27	453,386,846	366,305,106
31	621,787,675	502,361,288
32	544,064,215	439,566,127
33	483,612,636	390,725,446
37	705,268,427	569,807,942

CIV Control Register

Symbol: **CIVC**

Address: **10h**

Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL			CIV25	CIV24	CIVC1	CIVC0	PALN	CIVEN
TYPE			R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT			0	0	0	0	0	1

Bit 0 of register CIVC controls whether the FSCI value is used to set the sub-carrier frequency, or the automatically calculated (CIV) value. When the CIVEN value is 1, the number calculated and present at the CIV registers will automatically be used as the increment value for sub-carrier generation. Whenever this bit is set to 1, the CFRB bit should be set to 0. It is recommended to use the FSCI registers, and not the CIVEN mode for Macrovision applications.

Bit 1 of register CIVC forces the CIV algorithm to generate the PAL-Nc (Argentina) sub-carrier frequency when it is set to '1'. When this bit is set to '0', the VOS[1:0] value is used by the CIV algorithm to determine which sub-carrier frequency to generate.

Bits 3-2 of register CIVC control the hysteresis circuit which is used to calculate the CIV value. The default value should be used.

Bits 5-4 of register CIVC contain the MSB values for the calculated increment value (CIV) readout. This is described in detail in the CIV register description.

Calculated Increment Value Register

Symbol: **CIV**
Address: **11h – 13h**
Bits: **8 each**

BIT	7	6	5	4	3	2	1	0
SYMBOL	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#
TYPE	R	R	R	R	R	R	R	R
DEFAULT	X	X	X	X	X	X	X	X

Registers CIV contain the value that was calculated by the CH7010 as the sub-carrier increment value. The entire bit field, CIV[25:0], is comprised of these three registers plus the MSB values contained in the CIV Control register, bits CIV25 and CIV24. This value is used when the CIVEN bit is set to '1'. The bit locations are specified below. CIV registers are Read Only.

Register Contents

10hCIV[25:24]

11hCIV[23:16]

12hCIV[15:8]

13hCIV[7:0]

Clock Mode Register

Symbol: **CM**
Address: **1Ch**
Bits: **4**

BIT	7	6	5	4	3	2	1	0
SYMBOL					M/S*	MCP	PCM	XCM
TYPE					R/W	R/W	R/W	R/W
DEFAULT					0	0	0	0

Bit 0 of register CM signifies the XCLK frequency. A value of '0' is used when the XCLK is at the pixel frequency (dual edge clocking mode) and a value of '1' is used when the XCLK is twice the pixel frequency (single edge clocking mode).

Bit 1 of register CM controls the P-OUT clock frequency. A value of '0' generates a clock output at the pixel frequency, while a value of '1' generates a clock at twice the pixel frequency.

Bit 2 of register CM controls the phase of the XCLK clock input to the CH7010. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

Bit 3 of register CM controls whether the device operates in master or slave clock mode. In master mode (M/S* = '1'), the 14.31818MHz clock is used as a frequency reference in the TV PLL, and the M and N values are used to determine the TV PLL's operating frequency. In slave mode (M/S* = '0') the XCLK input is used as a reference to the TV PLL. The M and N TV PLL divider values are forced to one.

Input Clock Register

Symbol: **IC**
Address: **1Dh**
Bits: **4**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	1	0	0	0

Bits 3-0 of register IC controls the delay applied to the XCLK signal before latching input data D[11:0] per the following table.

Table 19. Delay applied to XCLK before latching input data D[11:0]

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data
1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

GPIO Control Register

Symbol: **GPIO**
Address: **1Eh**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	HPIE	POUTE	POUTP
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	0	0	0	0	0	0

Bit 0 of register GPIO controls the polarity of the P-OUT signal. A value of '0' does not invert the clock at the output pad.

Bit 1 of register GPIO enables the P-OUT signal. A value of '1' drives the P-OUT clock signal out of the P-OUT / TLDET* pin. A value of '0' disables the P-OUT signal.

Bit 2 of register GPIO enables the hot plug interrupt detection signal to be output from the P-OUT pin. A value of '1' allows the hot plug detect circuit to pull the P-OUT / TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal. The two control bits HPIE and POUTE should not be enabled (set to '1') at the same time.

Bit 3 of register GPIO resets the hot plug detection circuitry. A value of '1' causes the CH7010 to release the P-OUT / TLDET* pin. When a hot plug interrupt is asserted by the CH7010 (P-OUT / TLDET*) the CH7010 driver should read register 20h to determine the state of the DVI termination. After having read this register, the HPIR bit should be set high to reset the circuitry, and then set low again.

Bits 5-4 of register GPIO control the GPIO pins. When the corresponding GOENB bits are low, these register values are driven out of the corresponding GPIO pins. When the corresponding GOENB bits are high, these register values can be read to determine the level forced into the corresponding GPIO pins.

Bits 7-6 of register GPIO control the direction of the GPIO pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to an output.

Input Data Format Register

Symbol: **IDF**
Address: **1Fh**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits 2-0 of register IDF select the input data format. See Input Interface on page 10 for a listing of available formats.

Bit 3 of register IDF controls the horizontal sync polarity. A value of '0' defines the horizontal sync to be active low, and a value of '1' defines the horizontal sync to be active high.

Bit 4 of register IDF controls the vertical sync polarity. A value of '0' defines the vertical sync to be active low, and a value of '1' defines the vertical sync to be active high.

Bit 5 of register IDF controls the sync direction. A value of '0' defines sync to be input to the CH7010, and a value of '1' defines sync to be output from the CH7010. The CH7010 can only output sync signals when operating as a VGA to TV encoder, not when operating as a DVI transmitter.

Bit 6 of register IDF signifies when the CH7010 is to decode embedded sync signals present in the input data stream instead of using the H and V pins. This feature is only available for input data format four. A value of '0' selects the H and V pins to be used as the sync inputs, and a value of '1' selects the embedded sync signal.

Bit 7 of register IDF selects the input buffer used for the data, sync and clock input pins.

Connection Detect Register

Symbol: **CD**
Address: **20h**
Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL	HPIE2	Reserved	DVIT	DACT3	DACT2	DACT1	DACT0	SENSE
TYPE	R/W	R/W	R	R	R	R	R	R/W
DEFAULT	0	0	0	X	X	X	X	0

The Connection Detect Register provides a means to sense the connection of a TV to the four DAC outputs, and to determine the status of the DVI hot plug detect pin. The status bits, DACT[3:0] correspond to the termination of the four DAC outputs. However, the values contained in these STATUS BITS ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register to enable all DAC's.

2) Set the SENSE bit to a 1. This forces a constant output from the DAC's. Note that during SENSE = 1, these 4 analog outputs are at steady state and no TV synchronization pulses are asserted.

3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the four status bits corresponding to individual DAC outputs will be set if they are CONNECTED.

4) Read the status bits. The status bits, DACT[3:0] now contain valid information which can be read to determine which outputs are connected to a TV. Again, a "1" indicates a valid connection, a "0" indicates an unconnected output.

Bit 5 of register CD can be read at any time to determine the level of the hot plug detect pin. When the hot plug detect pin changes state, and the DVI output is selected, the P-OUT / TLDET* output pin will be pulled low signifying a change in the DVI termination. At this point, the HPIR bit in register 1Eh should be set high, then low to reset the hot plug detect circuit.

Bit 6 of register CD contains the MSB value for the crystal oscillator adjustment. This control is described in detail in the DC register description (register 21h).

Bit 7 of register CD enables the hot plug interrupt detection signal output from the GPIO[1] pin. A value of '1' allows the hot plug detect circuit to pull the GPIO[1] / TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal. The GOENB1 control bit in register 1Eh should be set to '1' when HPIE2 is set to '1'.

DAC Control Register

Symbol: **DC**
Address: **21h**
Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL	XOSC1	XOSC0		SYNCO1	SYNCO0	DACG1	DACG0	DACBP
TYPE	R/W	R/W		R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0		0	0	0	0	0

Bit 0 of register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[2:0] outputs.

Bits 2-1 of register DC control the DAC gain. DACG0 should be set low for NTSC and PAL-M video standards, and high for PAL and NTSC-J video standards. DACG1 should be low when the input data format is RGB (IDF = 0-3), and high when the input data format is YCrCb (IDF = 4).

Bits 4-3 of register DC select the signal to be output from the C/H Sync pin according to **Table 20** below.

Table 20. Composite / Horizontal Sync Output

SYNCO[1:0]	C/H Sync Output
00	No Output
01	VGA Horizontal Sync
10	TV Composite Sync
11	TV Horizontal Sync

Bits 7-6 of register DC controls the crystal oscillator. The default value is recommended.

Buffered Clock Output Register

Symbol: **BCO**
Address: **22h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	SHF2	SHF1	SHF0	BCOEN	BCOP	BCO2	BCO1	BCO0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits 2-0 of register BCO select the signal output at the BCO pin, according to **Table 21** below:

Table 21. BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	The 14MHz crystal	100	(for test use only)
001	(for test use only)	101	(for test use only)
010	VCO divided by K3	110	VGA Vertical Sync
011	Field ID	111	TV Vertical Sync

Bit 3 of register BCO selects the polarity of the BCO output. A value of '1' does not invert the signal at the output pad.

Bit 4 of register BCO enables the BCO output. When BCOEN is high, the BCO pin will output the selected signal. When BCOEN is low, the BCO pin will be held in tri-state mode.

Bits 7-5 of register BCO select the K3 divider, according to **Table 22** below.

Table 22. K3 Selection

SHF[2:0]	K3
000	2.5
001	3.0
010	3.5
011	4.0
100	4.5
101	5.0
110	6.0
111	7.0

Termination Register

Symbol: **TERM**
Address: **23h**
Bits: **1**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

HPDD (bit 2) of register TERM disables the hardware hot plug detection function. This function (default on) tri-states the DVI outputs when the hot plug detect pin (HPDET) is pulled low in accordance with the DVI specification, revision 1.0. This function is independent of the hot plug interrupt function (HPIE, register 1Eh, bit 2 and HPIE2, register 20h, bit 7) controlled via the SPP interface.
HPDD = 0 => hardware hot plug interrupt is enabled
= 1 => hardware hot plug interrupt is disabled

DVI Control Input Register

Symbol: **TCTL**
Address: **31h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	TPPD3	TPPD 2	TPPD 1	TPPD 0	CTL3	CTL2	CTL1	CTL0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	0	0	0	0	0	0

Bits 3-0 of register TCTL set the DVI control inputs applied to the green and red channels during sync intervals. It is recommended to leave these controls at the default value.

Bits 7-4 of register TCTL control the DVI PLL phase detector. The default value is recommended.

DVI PLL VCO Control Register

Symbol: **TVCO**
Address: **32h**

Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	TPVCO7	TPVCO6	TPVCO5	TPVCO4	TPVCO3	TPVCO2	TPVCO1	TPVCO0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	0	1	0	0	0	0	0

Register TVCO controls the state of the DVI PLL VCO, and should be set according to **Table 23**.

DVI PLL Charge Pump Control Register

Symbol: **TPCP**

Address: **33h**

Bits: **7**

BIT	7	6	5	4	3	2	1	0
SYMBOL	DVID2	DVID1	DVID0	Reserved	TPPSD1	TPPSD0	TPCP1	TPCP0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	0	0	1	0	0

Bits 1-0 of register TPCP control the DVI PLL charge pump. The default value shown on **Table 23** is recommended.

Bits 3-2 of register TPCP control the DVI PLL post scale divider. (see **Table 23**).

Bits 7-5 of register TPCP control the DVI transmitter output drive level. The default value shown on **Table 23** is recommended.

DVI PLL Divider Register

Symbol: **TPD**

Address: **34h**

Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	1	1	0

Bits 3-0 of register TPD control the DVI PLL feedback divider. (see table 22).

Bits 5-4 of register TPD control the DVI PLL feed forward divider. (see table 22).

DVI PLL Supply Control Register

Symbol: **TPVT**

Address: **35h**

Bits: **6**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	TPVT5	TPVT4	TPVT3	TPVT2	TPVT1	TPVT0
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	0	0	0	0

Bits 5-0 of register TPVT control the DVI PLL supply voltage. (see Table 22).

Bits 7-6 of register TPVT are reserved bits, and should be left at the default value.

Please see **Table 23** for the default values in terms of the frequency ranges.

DVI PLL Filter Register

Symbol: TLPF
Address: 36h
Bits: 4

BIT	7	6	5	4	3	2	1	0
SYMBOL	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits 3-0 of register TPT are reserved bits, and should be left at the default value.

Bits 7-4 of register TPT control the DVI PLL low pass filter. The default value is recommended.

DVI PLL VCO Control Overflow Register

Symbol: TCT
Address: 37h
Bits: 3

BIT	7	6	5	4	3	2	1	0
SYMBOL	TPVCO10	TPVCO9	TPVCO8	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bits 4-0 of register TCT are reserved bits, and should be left at the default value.

Bits 7-5 of register TCT contain the MSB values for the DVI PLL VCO control. (see Table 22).

Table 23. The Registers Default Settings In Terms Of The Frequency Ranges

Register		50MHz +/- 25MHz	100MHz +/- 25MHz	140MHz +/- 25MHz
31h	TCTL	0x00	0x00	0x00
32h	TVCO	0x23	0x23	0x2D
33h	TPCP	0x08	0x04	0x07
34h	TPD	0x16	0x26	0x26
35h	TPVT	0x30	0x30	0x30
36h	TPF	0x60	0x60	0xE0
37h	TVCOO	0x00	0x00	0x00

Reset Register

Symbol: **RES**
Address: **48h**
Bits: **2**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	Reserved	Reserved
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	1	0	0	0

Bit 3 of register RES controls the datapath reset signal. A value of '0' holds the datapath in a reset condition, while a value of '1', places the datapath in normal mode. The datapath is also reset at power on by an internally generated power on reset signal.

Bit 4 of register RES resets all control registers (addresses page 0:00h - 7Fh and page 1:00h - 61h). A value of '0' holds the serial port registers in a reset condition, while a value of '1', places the serial port registers in normal mode. The serial port registers are also reset at power on by an internally generated power on reset signal.

Power Management Register

Symbol: **PM**
Address: **49h**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	DVIP	DVIL	TV	DACPD3	DACPD2	DACPD1	DACPD0	FPD
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	1

FPD (bit0) of register PM controls power down of the entire chip except the serial port.

DACPD[3:0] (bits 4-1) of register PM control DAC0 through DAC3 Power Down. DAC0 through DAC3 will be turned on only if FPD bit is set to '0'. If FPD bit is set to '1', then DAC0 through DAC3 will be in power down state regardless of DACPD0 through DACPD3 state.

TV (bit 5) of the PM register enables the TV path.

DVIP and DVIL (bits 7-6) of the PM register controls the DVI path.

Register PM controls which circuitry within the CH7010 is operating, according to **Table 24** below.

Table 24. Power Management

DVIP	DVIL	TV	DACPD[3:0]	FPD	Operating State	Functional Description
X	X	1	1001	0	Composite Off, S-video on	Composite DACs are off
X	X	1	0111or	0	Composite On/S-video off	S-Video DACs are off
			1110			Either pin 39 CVBS/B or pin 36
						CVBS can be used for composite out
X	X	1	0000	0	Normal (On)	Both composite and s-video are on
X	X	0	XXXX	0	VGA to TV Encoder Off	TV off
1	1	X	XXXX	0	DVI Encode, Serialize, Transmitter, and PLL on	DVI is in normal function
X	X	X	XXXX	1	Full Power Down	All circuitry is powered down except serial port

Version ID Register

Symbol: **VID**
Address: **4Ah**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	1	0	1

Register VID is a read only register containing the version ID number of the CH7010.

Device ID Register

Symbol: **DID**
Address: **4Bh**
Bits: **8**

BIT	7	6	5	4	3	2	1	0
SYMBOL	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	1	0	1	1	0

Register DID is a read only register containing the device ID number of the CH7010.

7. ELECTRICAL SPECIFICATIONS

Table 25. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	DVDD, AVDD, TVDD, VDD relative to GND	- 0.5		5.0	V
	Input voltage of all digital pins[1]	GND - 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
TSTOR	Storage temperature	- 65		150	°C
TJ	Junction temperature			150	°C
TVPS	Vapor phase soldering (5 seconds)			260	°C
TVPS	Vapor phase soldering (11 seconds)			245	°C
TVPS	Vapor phase soldering (60 seconds)			225	°C

Notes:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latch.

Table 26. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	DAC power supply voltage	3.1	3.3	3.6	V
AVDD	Analog supply voltage	3.1	3.3	3.6	V
DVDD, TVDD	Digital supply voltage	3.1	3.3	3.6	V
DVDDV	Digital supply voltage (P-OUT pin)	1.1	1.8	3.6	V
RL	Output load to DAC outputs		37.5		Ω

Table 27. Electrical Characteristics (Operating Conditions: $T_A = 0^oC - 70^oC$, VDD, AVDD, DVDD, TVDD = 3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A resolution	10	10	10	Bits
	Full scale output current		33.9		mA
	Video level error			10	%
I_{VDD}	4 DAC's Enabled		130	145	mA
I_{VDD}	3 DAC's Enabled		100	110	mA
I_{AVDD}	DVI PLL Disabled		5	7	mA
I_{AVDD}	DVI PLL Enabled (85 MHz Pixel Clock)		17	22	mA
I_{DVDD}	TV-Out Enabled, DVI Disabled		85	150	mA
I_{DVDD}	TV-Out Disbled, DVI Enabled (85 MHz Pixel Clock)		50	70	mA
I_{TVDD}	Pixel Clock = 85 MHz		70	90	mA
	DVDDV (1.8V) curent (15pF load)		4		mA

Table 28. DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		2.7		DVDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		1.4	V
V_{DATAIH}	D[0-11] Input High Voltage		Vref+0.25		DVDD + 0.5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, AS, RESET*, HPDET Input High Voltage	DVDD=3.3V	2.7		DVDD + 0.5	V
V_{MISCIL}	GPIO, AS, RESET*, HPDET Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, AS, RESET*)	V_{IN} = 0V	0.5		5	uA
I_{MISCPD}	Pull Down Current (HPDET)	V_{IN} = 3.3V	0.5		5	uA
$V_{MISCAOH}$	GPIO, C/HSYNC, BCO, H, V Output High Voltage	I_{OH} = -400 uA	DVDD-0.2			V
$V_{MISCAOL}$	GPIO, C/HSYNC, BCO, H, V Output Low Voltage	I_{OL} = 3.2mA			0.2	V
$V_{MISCBOH}$	P-OUT Output High Voltage	I_{OH} = - 400 uA	DVDDV-0.2			V
$V_{MISCBOL}$	P-OUT Output Low Voltage	I_{OL} = 3.2 mA			0.2	V
V_H	DVI Single Ended Output High voltage	TVDD = 3.3V +/- 5% R_{TERM} 50 ohm +/- 1% R_{SWING} 2400 ohm +/- 1%	TVDD - 0.01		TVDD + 0.01	V
V_L	DVI Single Ended Output Low Voltage		TVDD - 0.6		TVDD - 0.4	V
V_{SWING}	DVI Single Ended Output Swing Voltage		400		600	mVp-p
V_{OFF}	DVI Single Ended Standby Output Voltage		TVDD - 0.01		TVDD + 0.01	V

Note:

V_{DATA} - refers to all digital data (D[11:0]), clock (XCLK, XCLK*), sync (H, V) and DE inputs. V_{MISCA} - refers to GPIOx, RESET*, AS and HPDET inputs and GPIOx, BCO/VSYNC, CHSYNC and H, V when configured as outputs (SYO=1). V_{MISCB} - refers to P-OUT.

Table 29: AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance	f_{XCLK} = 75MHz		2		ns
t_{DVIR}	DVI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{DVIF}	DVI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	DVI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	DVI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
t_{DVIJIT}	DVI Output Clock Jitter	f_{XCLK} = 165MHz			150	ps
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.5			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.5			ns
t_R	Pout, H and V (when configured as outputs) Output Rise Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_F	Pout, H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

8. TIMING INFORMATION

8.1 Clock - Master, Sync - Master Mode

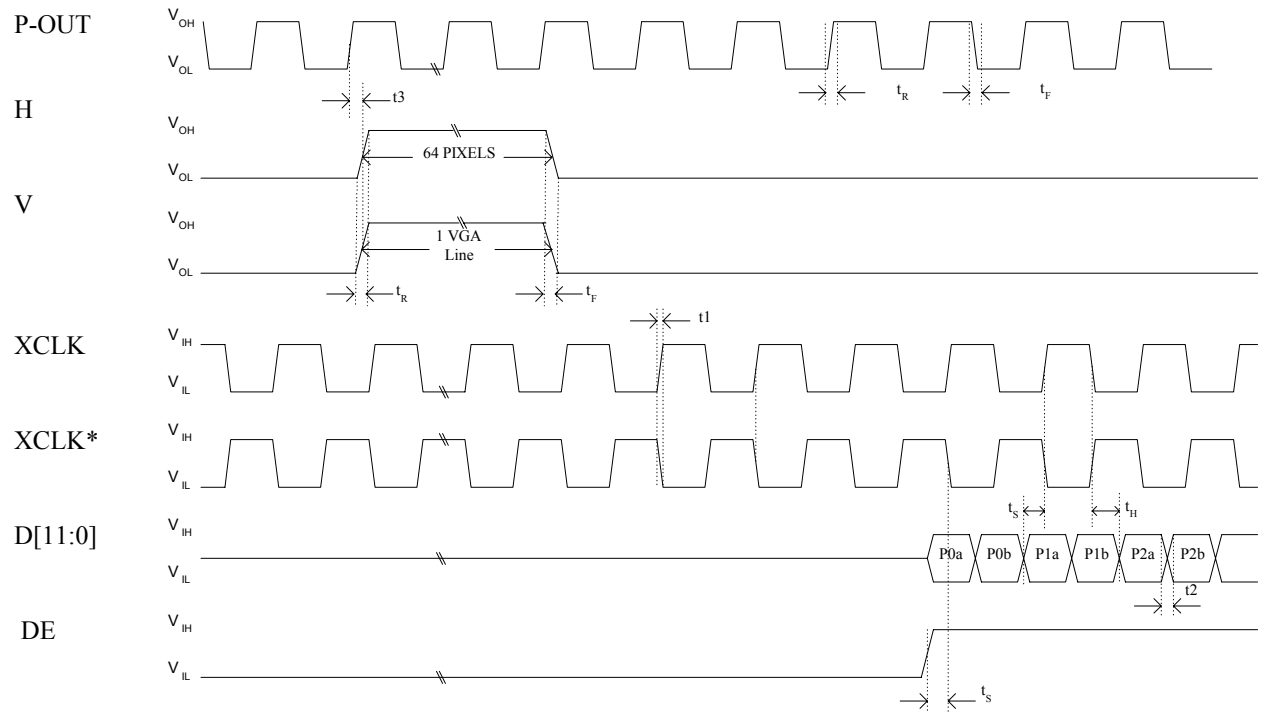

Figure 18: Timing for Clock - Master, Sync - Master Mode

Table 30. Timing and Voltage Levels for Clock - Master, Sync - Master Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t_R	Pout, H, V (when configured as outputs) Output Rise Time	see **Table 29**			
t_F	Pout, H, V (when configured as outputs) Output Fall Time	see **Table 29**			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0] & DE rise/fall time w/15pF load		1		ns
t3	Hold time: P-OUT to HSYNC, VSYNC delay		1.5		ns

8.2 Clock - Slave, Sync - Slave Mode

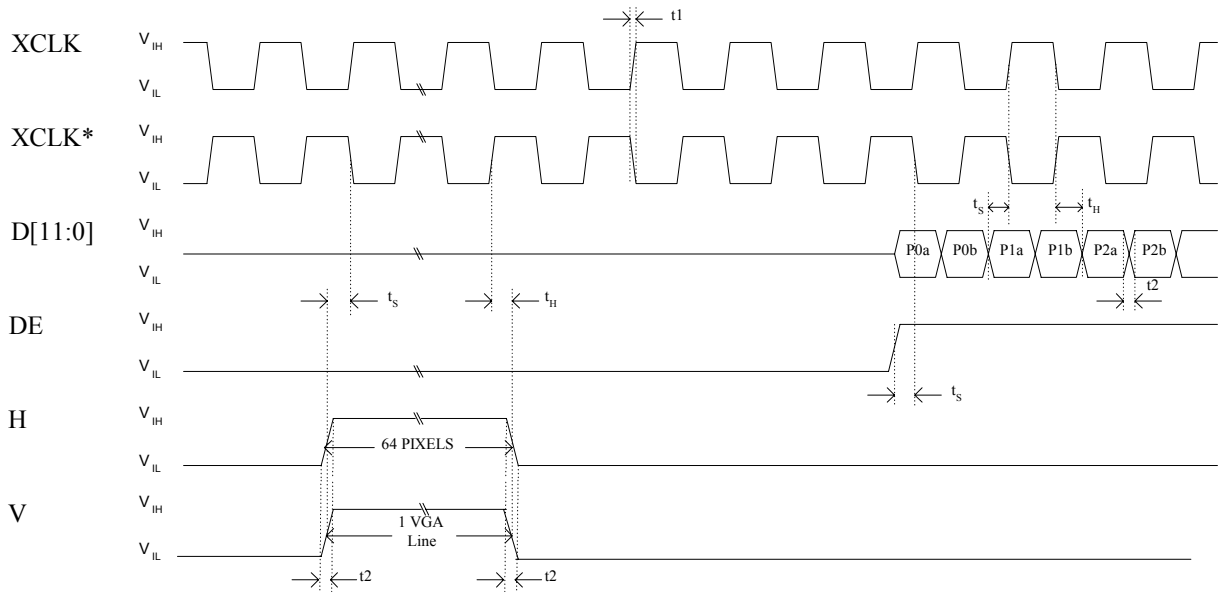

Figure 19: Timing for Clock - Slave, Sync - Slave Mode

Table 31: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V & DE rise/fall time w/ 15pF load		1		ns

8.3 Clock - Master, Sync - Slave Mode

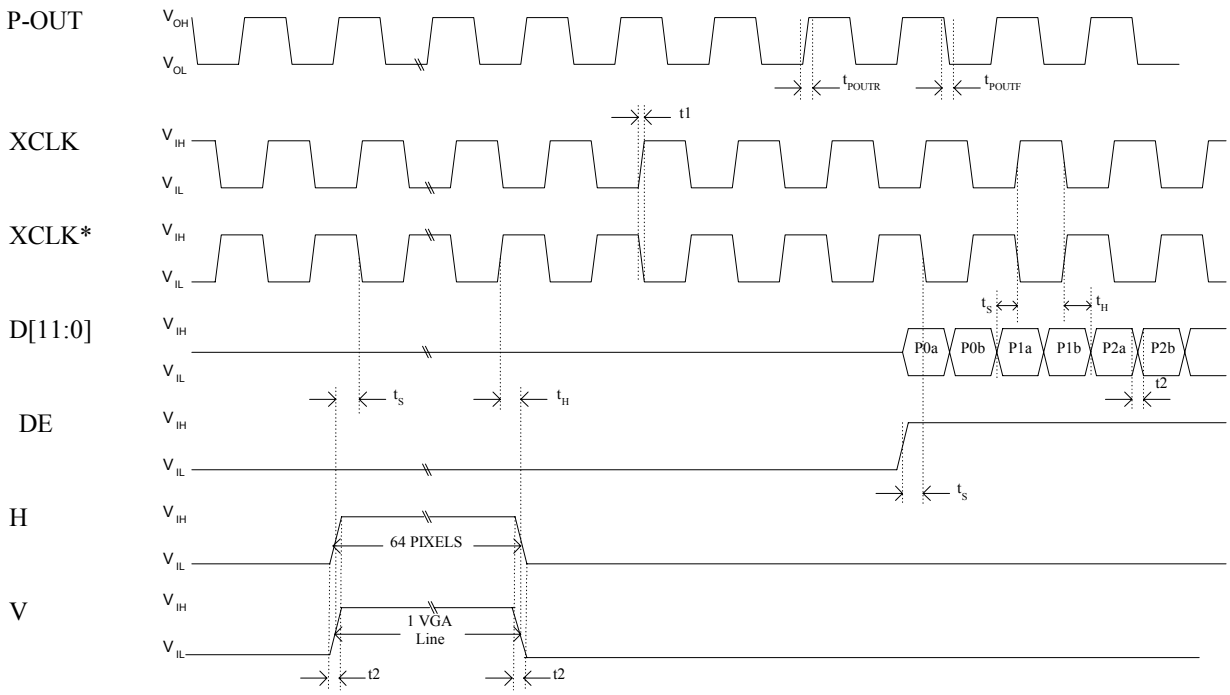

Figure 20: Timing for Clock - Master, Sync - Slave Mode

Table 32. Timing for Clock - Master, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Table 29**			
t_R	Pout Output Rise Time	see **Table 29**			
t_F	Pout Output Fall Time	see **Table 29**			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V & DE rise/fall time w/15pF load		1		ns

9. PACKAGE DIMENSIONS

64-pin LQFP

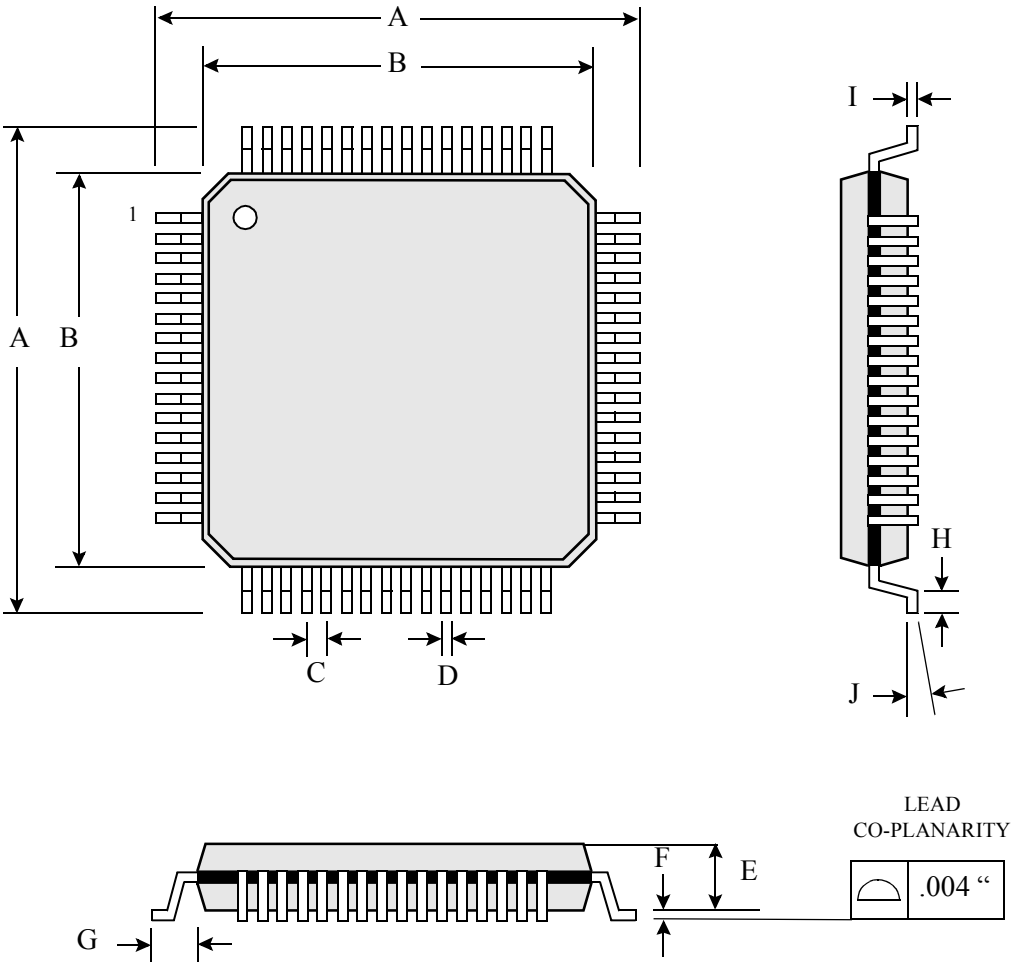

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	11.80		0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX	12.20	10.00		0.27	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

10. REVISION HISTORY

Rev. #	Date	Section	Description
1.0	11/01/01	All	First official release of CH7010A datasheet, rev. 1.0
3.0	09/06/02	All	CH7010A changed to CH7010B
		3.2	Pin description of table 1 updated.
			Table 28 added into datasheet.
		Register Map	Register map updated.
		All	Default bit values and public bits changed on various registers. 02h, 0Bh, 23h, 31h, 32h, 33h, 34h, 35h, 36h, 37h, 38h.
		7	Electrical Specifications changed: AC specifications added.
		8	Timing information tables updated.
	7/12/04	Section 5.4	Updated DVI hotplug description

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7010B-T	LQFP	64	3.3V
CH7010B-T-TR	LQFP in Tape & Reel	64	3.3V
CH7010B-TF	Lead free LQFP	64	3.3V
CH7010B-TF-TR	Lead free LQFP in Tape & Reel	64	3.3V

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