

DAVICOM Semiconductor, Inc.

DM5865

720H 4 channels NTSC/PAL Decoder

DATA SHEET

Preliminary
Version: DM5865-DS-P01
February 27, 2013

REVISION HISTORY:

Date	Revision	Description
2012/02/02	1.1	Initial release
2012/02/04	1.2	Application schematics modified

PRELIMINARY

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PRELIMINARY

Introduction

The DM5865 is a 4-channel video decoder which converts 4 channels of 6.5 MHz analog CVBS signals to 4 channels of digital 27 MHz CCIR656 signals. The DM5865 integrates two internal PLLs, and decodes 720H videos using the same (27MHz) external clock source. The DM5865 also features a patented fast switch function. With the fast switch function, the DM5865 can decode up to 8 analog CVBS with little frame rate loss.

The DM5865 also includes five audio ADCs and one audio DAC. Audio cascade up to 16 channels is also supported.

Features

Video Decoder

- Accepts NTSC (M), PAL (B, D, G, H, I, M, Nc)
- Hardware Fast Switch function
- Fast Switch also controllable by software or external pin
- Software channel ID in active region
- Four 10-bits video ADCs with built in 6.5 MHz analog low pass filter
- Automatic gain control for Luminance and Chrominance
- Programmable brightness, contrast, saturation, hue, and sharpness
- 5-H comb filter for YC separation
- Chrominance line filter for PAL phase error
- DLL for video synchronization, supports 27MHz crystal within +/-1000 ppm variance
- Advanced video synchronization for weak and noisy CVBS. Supports video signal transmitted by 500-meter long cable
- Up to 4 CCIR656 output interfaces which could be configured as 4 sets of CCIR656 (27MHz) or 2 sets of TDM2 (54MHz) or 2 set of TDM4 (108MHz)
- Support line lock camera

Audio Codecs

- Five audio ADCs and one audio DAC are integrated
- Master I2S/DSP playback, record and audio-mixing
- Supports extended I2S/DSP format transmitting up to 16 audio channels using one data pin
- Audio cascade up to 16 channels
- 16-bit or 8-bit 48/24/16/8 KHz PCM format

Miscellaneous

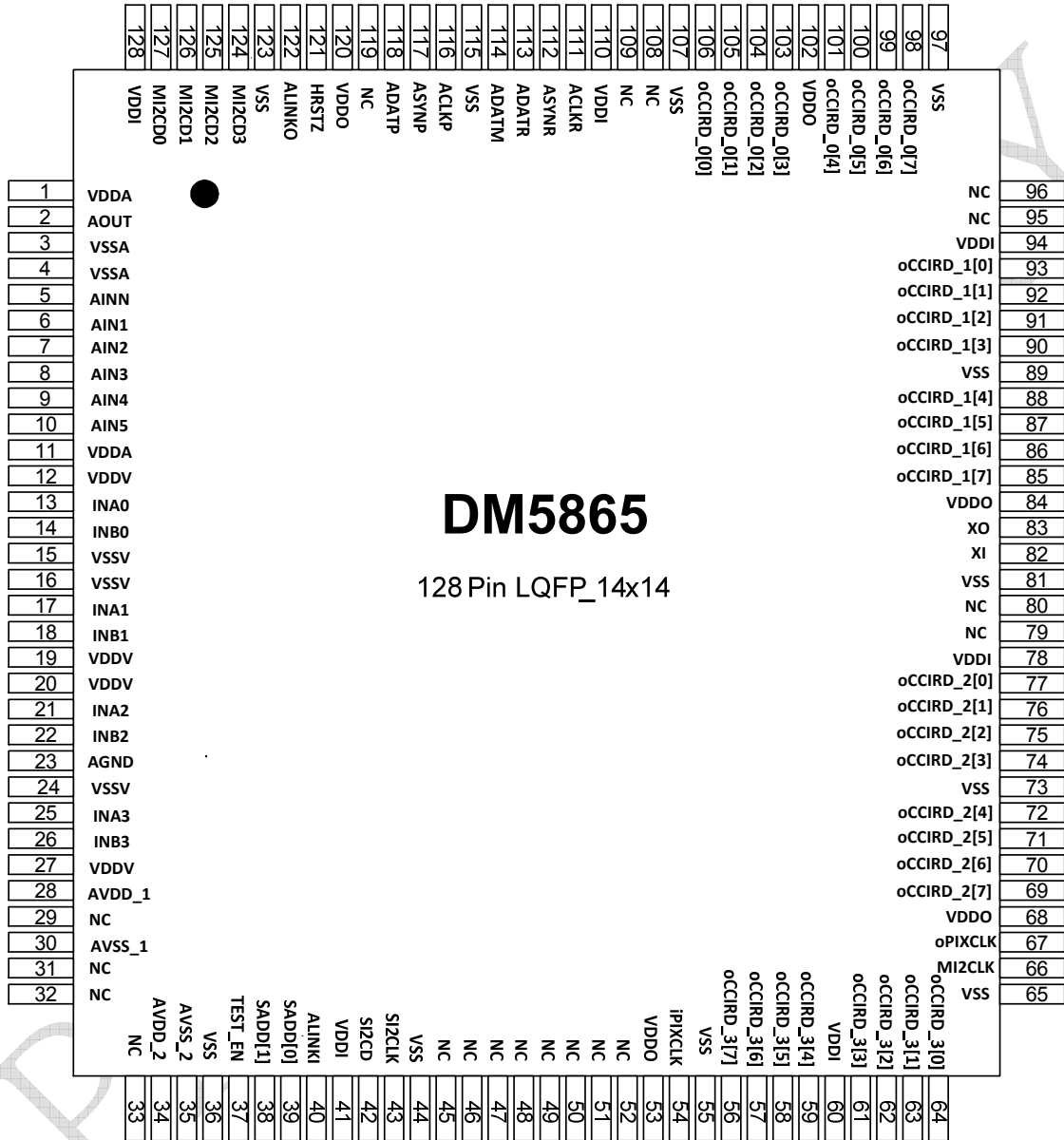
- Use a single external 27MHz crystal to support 720H video
- Two programmable PLLs integrated
- Slave I2C bus
- Ultra low power consumption. Under 500mW for normal operation. Under 50mW for suspend mode.
- 128-pin LQFP package (14mmx14mm)
- 1.8V core power, 3.3V analog power and 1.8V analog power

Applications

Suggested applications include

- DVR
- Car DVR
- Video capture card

Terminal Assignment



DM5865

128 Pin LQFP_14x14

Terminal Functions

Pin number	Pin Name	type	description
1	VDDA	P	1.8V Power for analog audio DAC
2	AOUT	A	Audio output
3	VSSA	G	Ground for analog audio DAC
4	VSSA	G	Ground for analog audio ADC
5	AINN	A	Audio input negative control
6	AIN1	A	Audio input of channel 0
7	AIN2	A	Audio input of channel 1
8	AIN3	A	Audio input of channel 2
9	AIN4	A	Audio input of channel 3
10	AIN5	A	Audio input of channel 4
11	VDDA	P	1.8V Power for analog audio ADC
12	VDDV	P	1.8V Power for video ADC
13	INA0	A	CVBS input A of channel 0 or S-VIDEO Y of channel 0
14	INB0	A	CVBS input B of channel 0 or S-VIDEO Y of channel 0
15	VSSV	G	Ground for video ADC
16	VSSV	G	Ground for video ADC
17	INA1	A	CVBS input A of channel 1 or S-VIDEO C of channel 0
18	INB1	A	CVBS input B of channel 1 or S-VIDEO C of channel 0
19	VDDV	P	1.8V Power for video ADC
20	VDDV	P	1.8V Power for video ADC
21	INA2	A	CVBS input A of channel 2 or S-VIDEO Y of channel 1
22	INB2	A	CVBS input B of channel 2 or S-VIDEO Y of channel 1
23	AGND	G	Analog ground (used as signal input reference, CH_AGND)
24	VSSV	G	Ground for video ADC
25	INA3	A	CVBS input A of channel 3 or S-VIDEO C of channel 1
26	INB3	A	CVBS input B of channel 3 or S-VIDEO C of channel 1
27	VDDV	P	1.8V Power for video ADC
28	AVDD_1	P	1.8V Power for analog clock PLL1
29	NC		
30	AVSS_1	G	Ground for analog clock PLL1

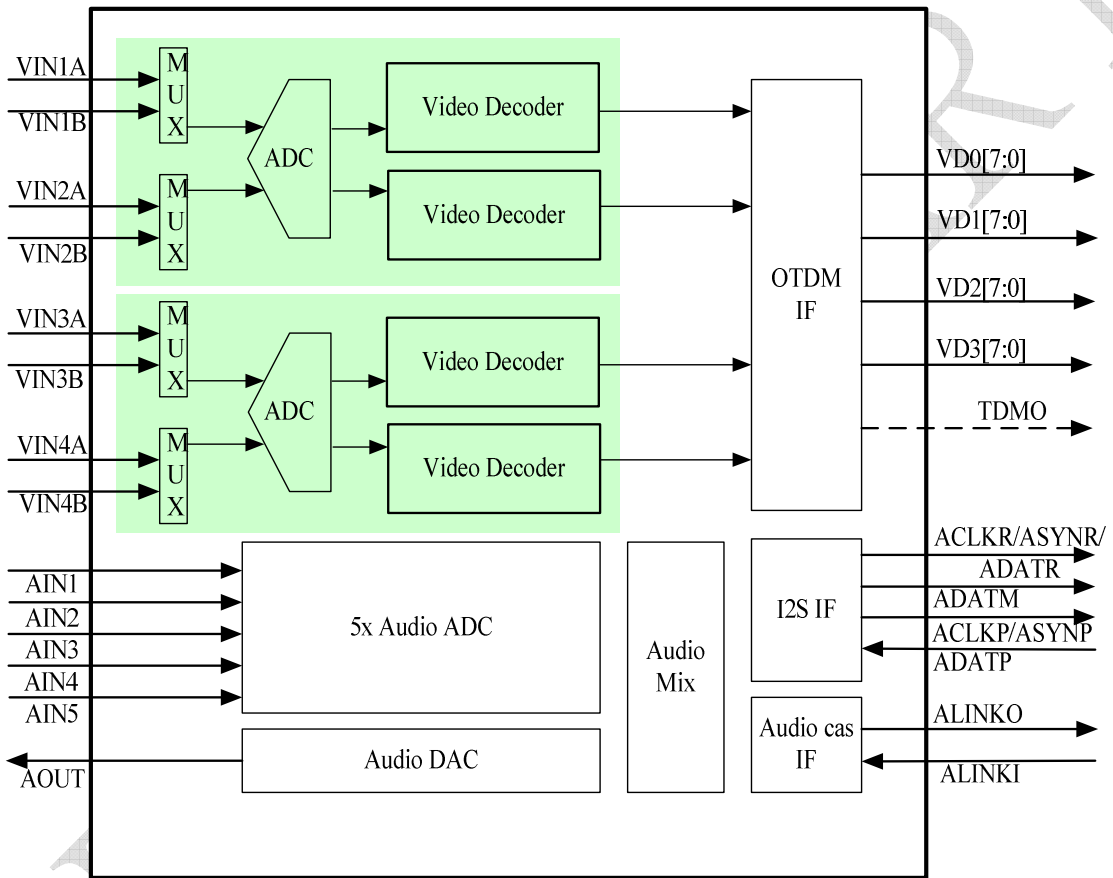
31	NC		
32	NC		
33	NC		
34	AVDD_2	P	1.8V Power for analog clock PLL2
35	AVSS_2	G	Ground for analog clock PLL2
36	VSS	G	Ground for internal logic and output driver
37	TEST_EN	I	Test enable, please connect it to ground
38	SADD[1]	I	I2C Device ID strapping
39	SADD[0]	I	I2C Device ID strapping
40	ALINKI	I	Audio Multi-chip serial input
41	VDDI	P	1.8V Power for internal logic.
42	SI2CD	IO	Slave I2C data (open drain)
43	SI2CLK	I	Slave I2C clock
44	VSS	G	Ground for internal logic and output driver.
45	NC		
46	NC		
47	NC		
48	NC		
49	NC		
50	NC		
51	NC		
52	NC		
53	VDDO	P	3.3V Power for output driver
54	NC		
55	VSS	G	Ground for internal logic and output driver
56	oCCIRD_3[7]	IO	Video data output of channel 3.
57	oCCIRD_3[6]	IO	Video data output of channel 3.
58	oCCIRD_3[5]	IO	Video data output of channel 3.
59	oCCIRD_3[4]	IO	Video data output of channel 3.
60	VDDI	P	1.8V Power for internal logic.
61	oCCIRD_3[3]	IO	Video data output of channel 3.
62	oCCIRD_3[2]	IO	Video data output of channel 3.
63	oCCIRD_3[1]	IO	Video data output of channel 3.
64	oCCIRD_3[0]	IO	Video data output of channel 3.
65	VSS	G	Ground for internal logic and output driver.
66	MI2CLK	IO	Master i2c clock (open drain)
67	oPIXCLK	O	CCIR656 27MHz, TDM 54/108 MHz
68	VDDO	P	3.3V Power for output driver.
69	oCCIRD_2[7]	IO	Video data output of channel 2.
70	oCCIRD_2[6]	IO	Video data output of channel 2.



71	oCCIRD_2[5]	IO	Video data output of channel 2.
72	oCCIRD_2[4]	IO	Video data output of channel 2.
73	VSS	G	Ground for internal logic and output driver.
74	oCCIRD_2[3]	IO	Video data output of channel 2.
75	oCCIRD_2[2]	IO	Video data output of channel 2.
76	oCCIRD_2[1]	IO	Video data output of channel 2.
77	oCCIRD_2[0]	IO	Video data output of channel 2.
78	VDDI	P	1.8V Power for internal logic.
79	NC		
80	NC		
81	VSS	G	Ground for internal logic and output driver.
82	XI	I	Crystal connection or Oscillator clock input.
83	XO	O	For crystal 27 MHz connection.
84	VDD0	P	3.3V Power for output driver.
85	oCCIRD_1[7]	IO	Video data output of channel 0, TDM54 output
86	oCCIRD_1[6]	IO	Video data output of channel 0, TDM54 output
87	oCCIRD_1[5]	IO	Video data output of channel 0, TDM54 output
88	oCCIRD_1[4]	IO	Video data output of channel 0, TDM54 output
89	VSS	G	Ground for internal logic and output driver.
90	oCCIRD_1[3]	IO	Video data output of channel 0, TDM54 output
91	oCCIRD_1[2]	IO	Video data output of channel 0, TDM54 output
92	oCCIRD_1[1]	IO	Video data output of channel 0, TDM54 output
93	oCCIRD_1[0]	IO	Video data output of channel 0, TDM54 output
94	VDDI	P	1.8V Power for internal logic.
95	NC		
96	NC		
97	VSS	G	Ground for internal logic and output driver.
98	oCCIRD_0[7]	O	Video data output of channel 0, TDM54 output or TDM108 output
99	oCCIRD_0[6]	O	Video data output of channel 0, TDM54 output or TDM108 output
100	oCCIRD_0[5]	O	Video data output of channel 0, TDM54 output or TDM108 output
101	oCCIRD_0[4]	O	Video data output of channel 0,

			TDM54 output or TDM108 output
102	VDDO	P	3.3V Power for output driver.
103	oCCIRD_0[3]	O	Video data output of channel 0, TDM54 output or TDM108 output
104	oCCIRD_0[2]	O	Video data output of channel 0, TDM54 output or TDM108 output
105	oCCIRD_0[1]	O	Video data output of channel 0, TDM54 output or TDM108 output
106	oCCIRD_0[0]	O	Video data output of channel 0, TDM54 output or TDM108 output
107	VSS	G	Ground for internal logic and output driver.
108	NC		
109	NC		
110	VDDI	P	1.8V Power for internal logic.
111	ACLKR	O	Audio serial clock output of record.
112	ASYNR	O	Audio serial sync output of record.
113	ADATR	O	Audio serial data output of record.
114	ADATM	O	Audio serial data output of mixing
115	VSS	G	Ground for internal logic and output driver.
116	ACLKP	O	Audio serial clock output of playback
117	ASYNP	O	Audio serial sync output of playback
118	ADATP	I	Audio serial data input of playback
119	NC		
120	VDDO	P	3.3V Power for output driver.
121	HRSTZ	I	System reset.
122	ALINKO	O	Audio Multi-chip serial output
123	VSS	G	Ground for internal logic and output driver.
124	MI2CD3	IO	Master I2C data3 (open drain)
125	MI2CD2	IO	Master I2C data2 (open drain)
126	MI2CD1	IO	Master I2C data1 (open drain)
127	MI2CD0	IO	Master I2C data0 (open drain)
128	VDDI	P	1.8V Power for internal logic.

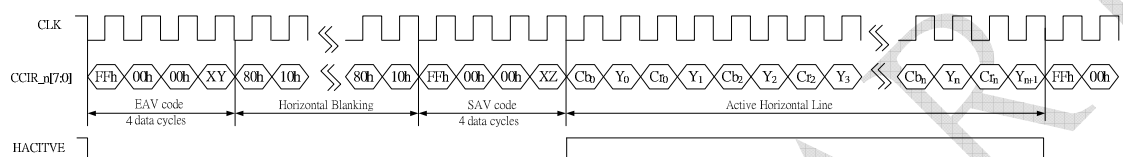
Block Diagram



Video Decoder

Video Interface

The DM5865 outputs 27MHz CCIR656 with 720x480/720x576 resolution. For these video outputs, SAV (Start of Active Video) and EAV (End of Active Video) are inserted to indicate active video interval. Each channel uses one output port to transmit video data, that is, luminance and chrominance data are transmitted through the same port. The output timing diagram is shown below.



The number of data cycles in active horizontal line will vary according to the output format. The active horizontal line contains 1440 cycles.

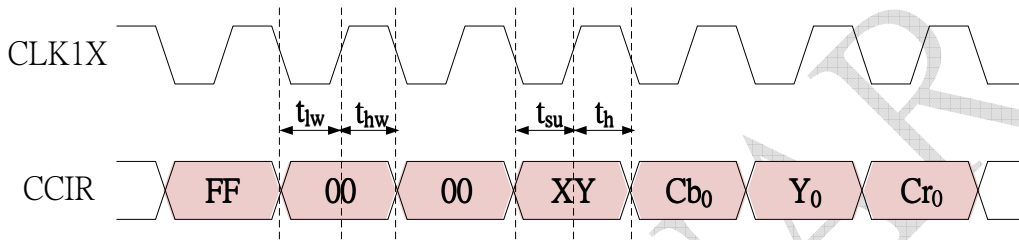
SAV and EAV indicate the active video interval. The values of the first three bytes in SAV and EAV are invariant preamble: 0xFF, 0x00, and 0x00. Different values are designated to the last byte according to different conditions: Field, V time, and H time. The MSB of this byte is always set to 1 and it's followed by three bits to represent the condition of F, V, and H respectively. The last four bits are used as protection bits. The detailed code sequences of SAV and EAV are illustrated in the following table.

Condition			FVH Value			SAV/EAV Code Sequence			
Field	V time	H time	F	V	H	Byte 0	Byte 1	Byte 2	Byte 3
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1

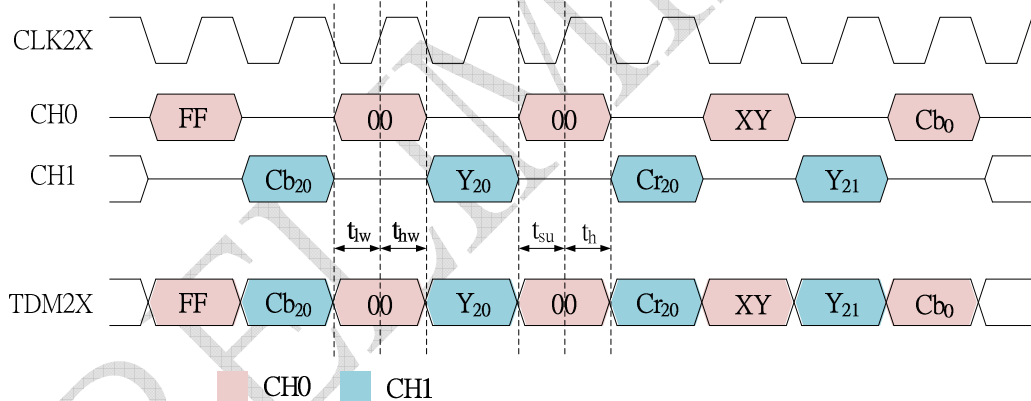
Multi-channel Time Division Multiplexing

The DM5865 supports 2/4-channel time division multiplexed output format. Thus two or four video channels can be transmitted through one output port. The clock rate should be two or four times of the original sampling rate according to the number of channels to be multiplexed.

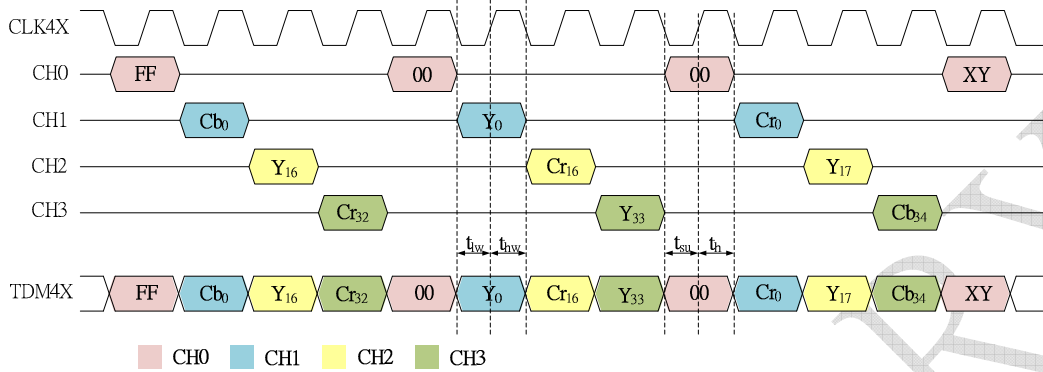
The basic case is the non-multiplexed output. The clock rate follows the original data rate (27 MHz). The timing diagram is illustrated below.



When two-channel multiplexing is selected, two times of the original clock rate is used (54 MHz). The timing diagram is illustrated below.



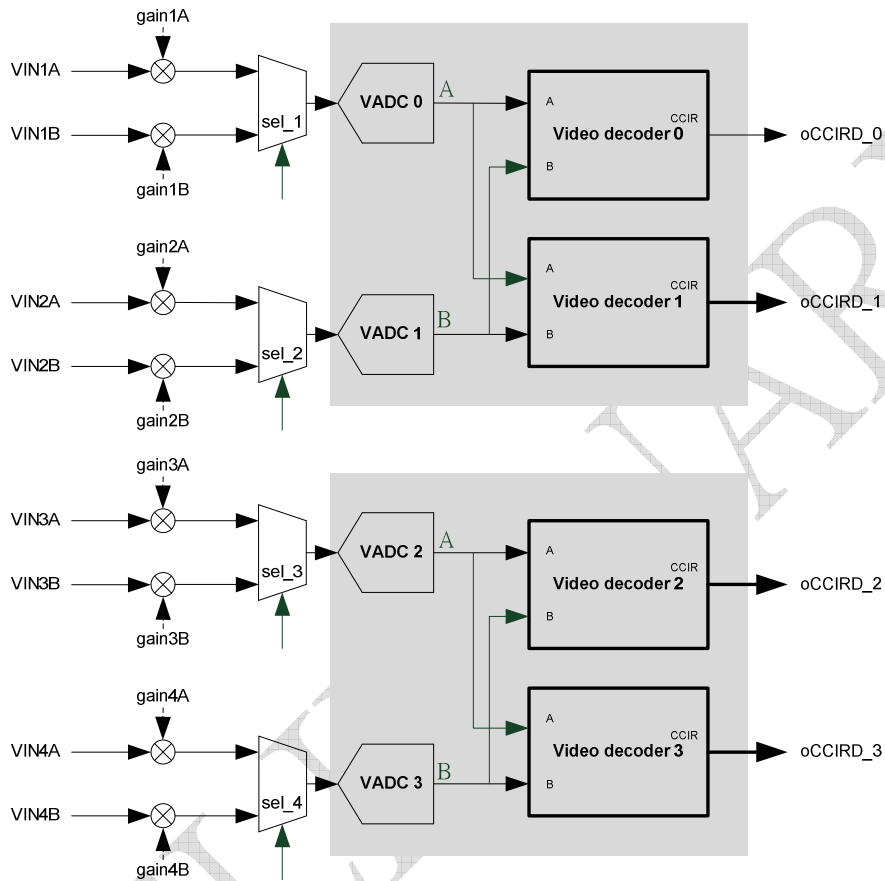
When four-channel multiplexing is selected, four times of the original clock rate is used (108 MHz). The timing diagram is illustrated below.



In the Multi-channel Time Division Multiplexing mode, channel IDs are used to indicate the corresponding channels. Channel IDs are defined as the last four bits in SAV/EAV code sequence (i.e. the originally-defined protection bits). The relationship between SAV/EAV code sequence and channel ID is illustrated in the following table.

Condition			FVH Value			EAV/SAV Code Sequence						
Field	V time	H time	F	V	H	Byte 0	Byte 1	Byte 2	Byte 3			
									Ch0	Ch1	Ch2	Ch3
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3

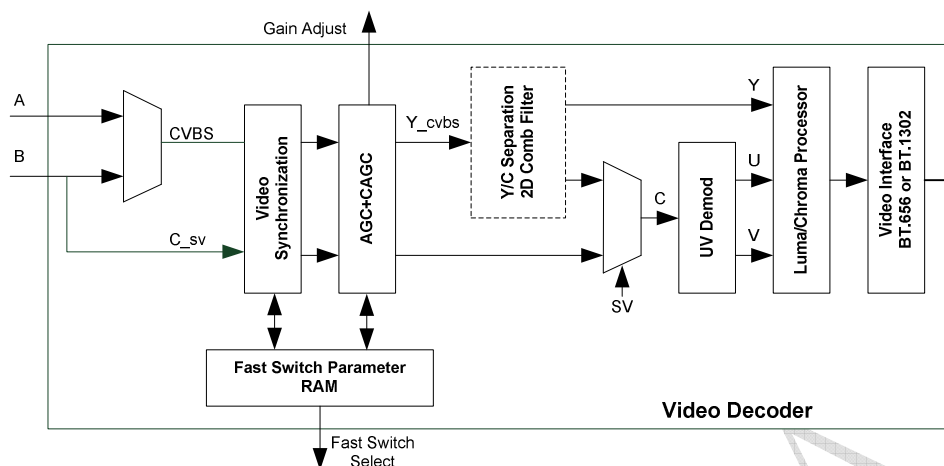
4-CH Video Decoder



The DM5865 contains four video decoders supporting up to 8 CVBS inputs.

Each CVBS has its own gain amplifier. For each pair of VINA and VINB, a 2-to-1 MUX selects one CVBS source and passes this source to one video analog-to-digital converter (VADC). The DM5865 has 4 VADCs and 4 video decoders (VD). The VADCs and VDs are organized as 2 banks as shown in the above figure. Each bank can be independently configured to operate at 27MHz.

Video Decoder Unit



The DM5865 video decoder contains a Video Synchronization block, an AGC block, an YC separation block, a UV Demodulation block, a Luma/Chroma Processor block and a BT 656 output block. A patented Fast Switch is also included.

In addition to CVBS, the DM5865 video decoder supports S-Video as well.

Video Synchronization

Video Synchronization performs video detection function. It automatically detects NTSC(M), NTSC(443), PAL(B,D,G,H,I), PAL(M), PAL(N), PAL(60). A smart video detection algorithm has been adopted. Therefore the DM5865 can perform fast and stable video synchronization even if the input signal is weak or the external crystal is with error as large as +/- 1000 ppm.

Automatic Gain Control

Automatic Gain Control (AGC) block performs both Luma AGC and Chroma AGC (CGAC). After video synchronization, Luma AGC adjusts input Luma level to the standard level (1Vpp). A further CAGC is performed after Luma AGC for signal with different Luma and Chroma attenuation.

Y/C Separation

Y/C Separation is for CVBS input only. After this block CVBS signal is separated into Luma and Chroma components. A 5-H 2D comb filter is adapted in the Y/C separation block.

UV demodulation

After Y/C separation, the UV demodulation block performs UV demodulation to the Chroma component. The phase and frequency of the UV demodulation is from a color burst subcarrier tracking block for both NTSC and PAL mode. A UV demodulation LPF is also adopted to filter out chroma noise.

Luma/Chroma Processor

This block contains a programmable Luma sharpness filter. Hue, Saturation, Brightness and Contrast adjustment are also supported. The adjusted video is then transformed from YUV to YCbCr domain for CCIR656 output interface.

Video Interface

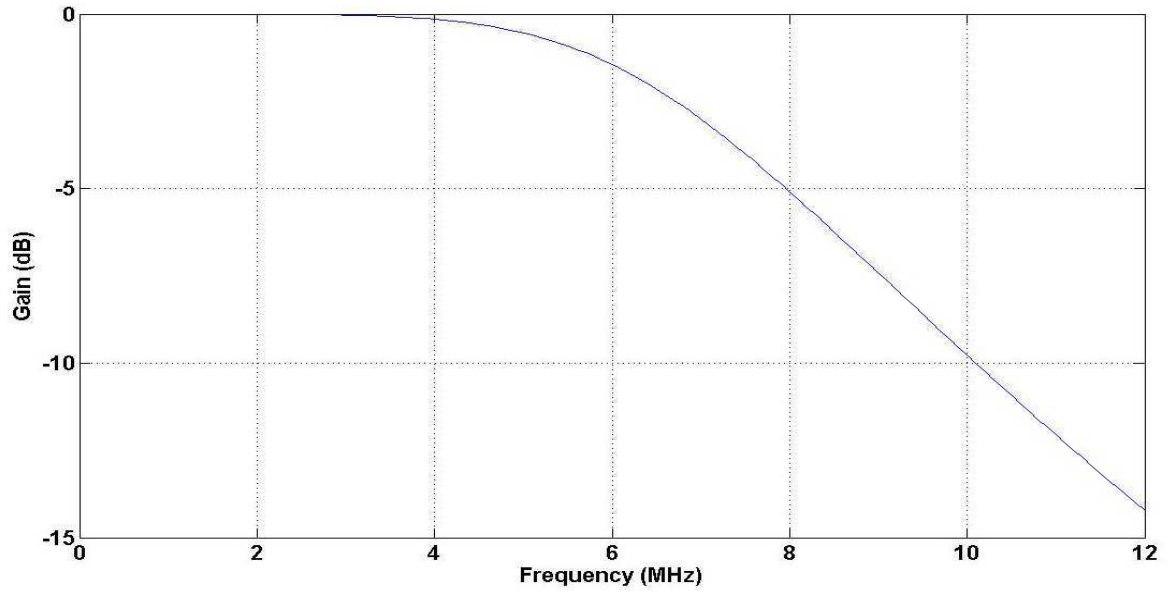
The DM5865 video decoder supports 27MHz BT.656 video output format. A horizontal cropping function also included in this block.

Fast Switch Parameter RAM

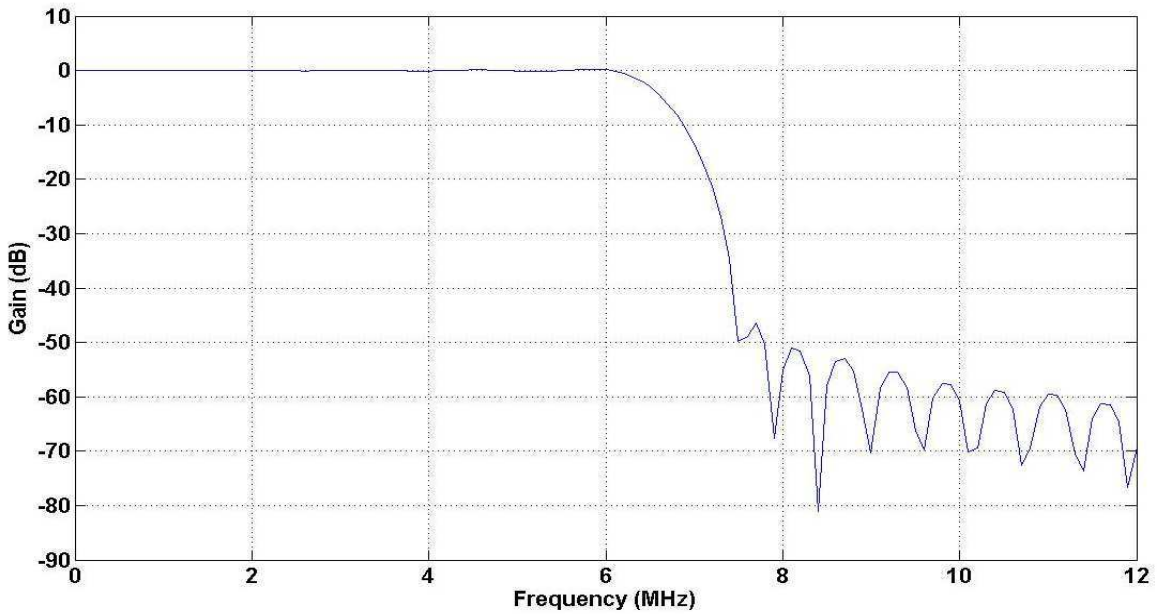
The DM5865 features a patented hardware video source fast switch function. The Fast Switch block has a table which stores video characteristic. Each time HW switches to a previously tracked video source it could complete video synchronization within several lines. With this feature, the DM5865 can decode up to 8 CVBS with little frame rate loss.

Filter response

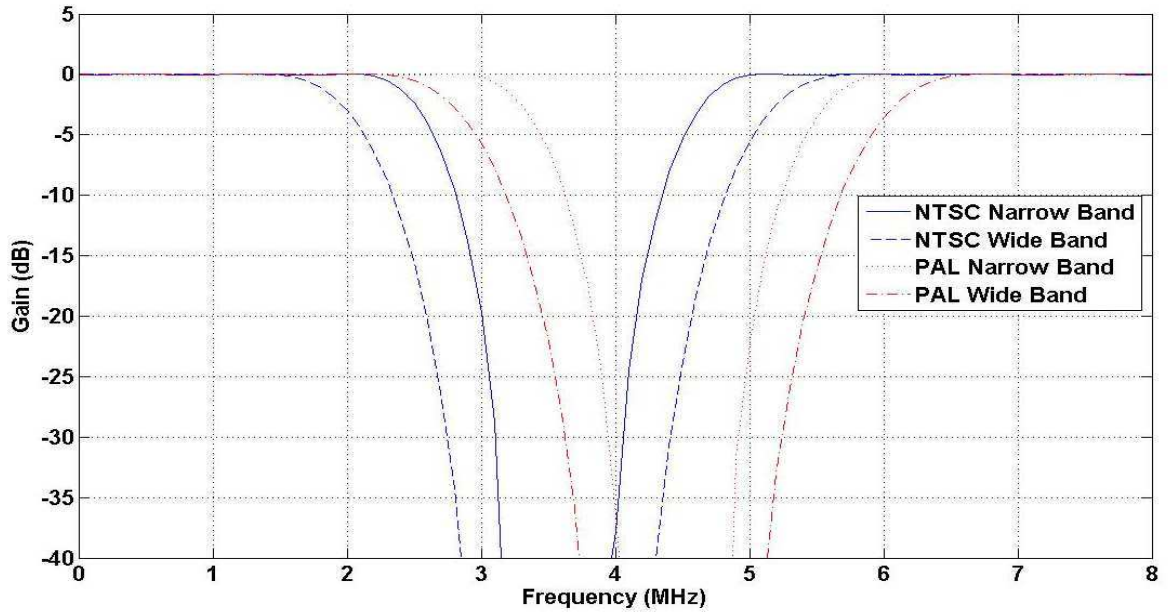
Anti-alias LPF



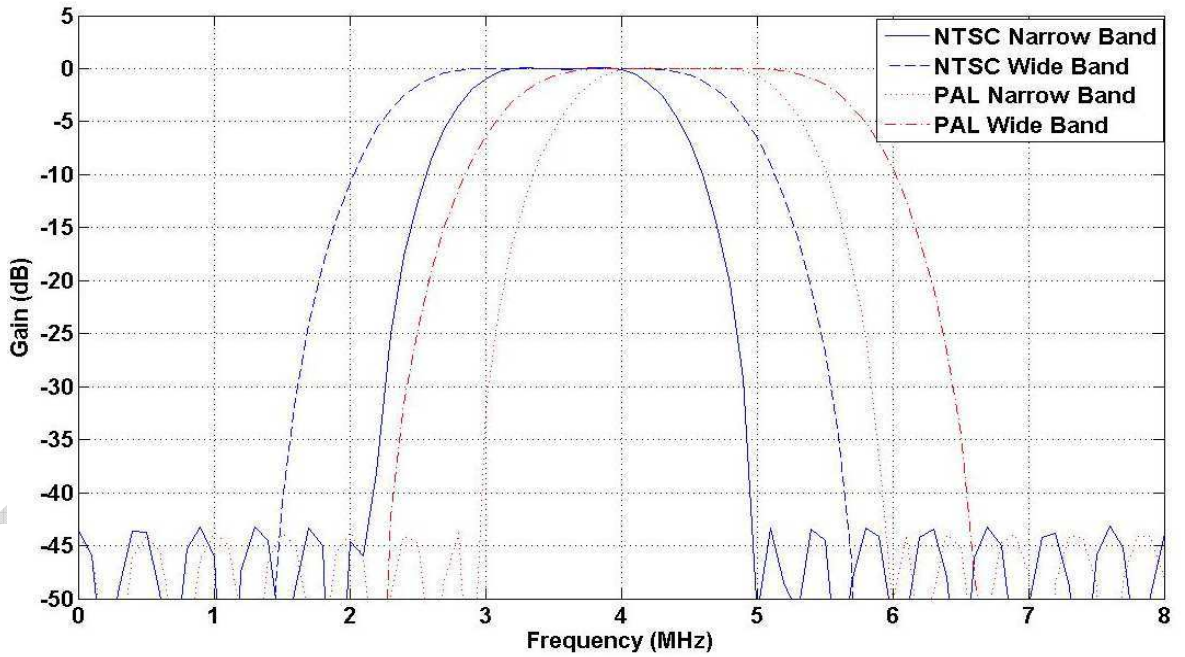
Decimation filter



Luma notch filter

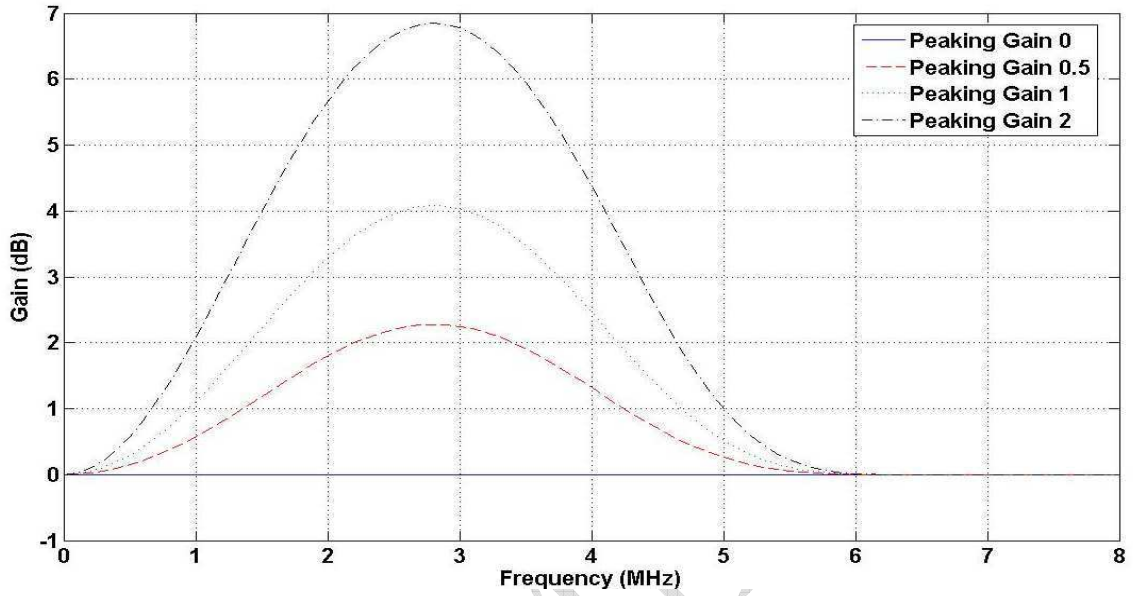


Chroma band pass filter

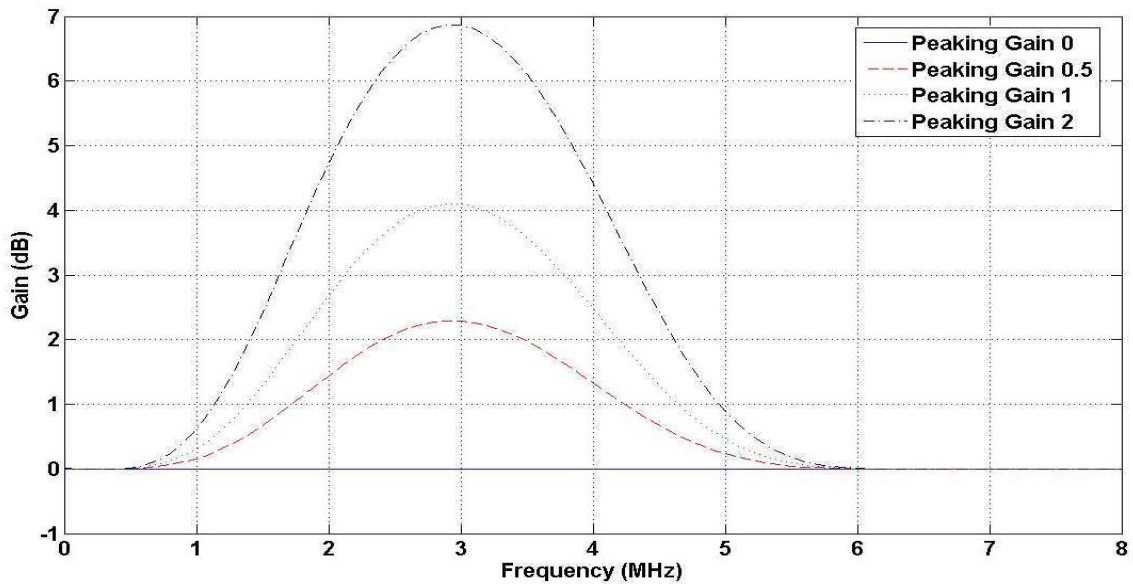


Y sharpness filter

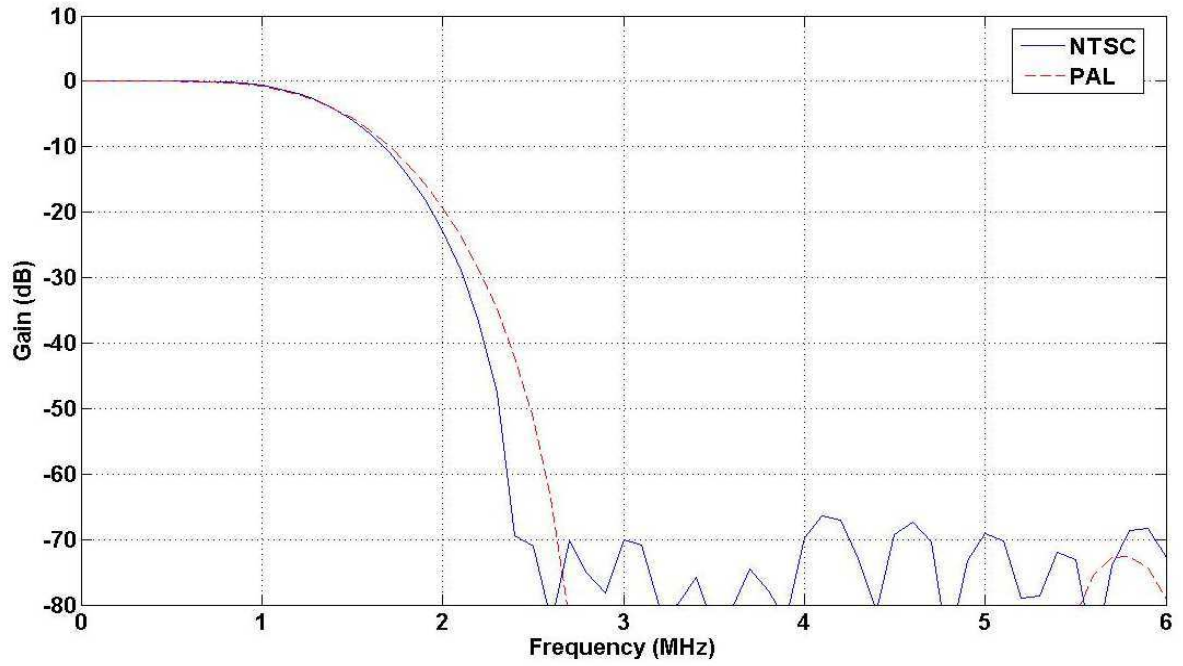
■ NTSC



■ PAL

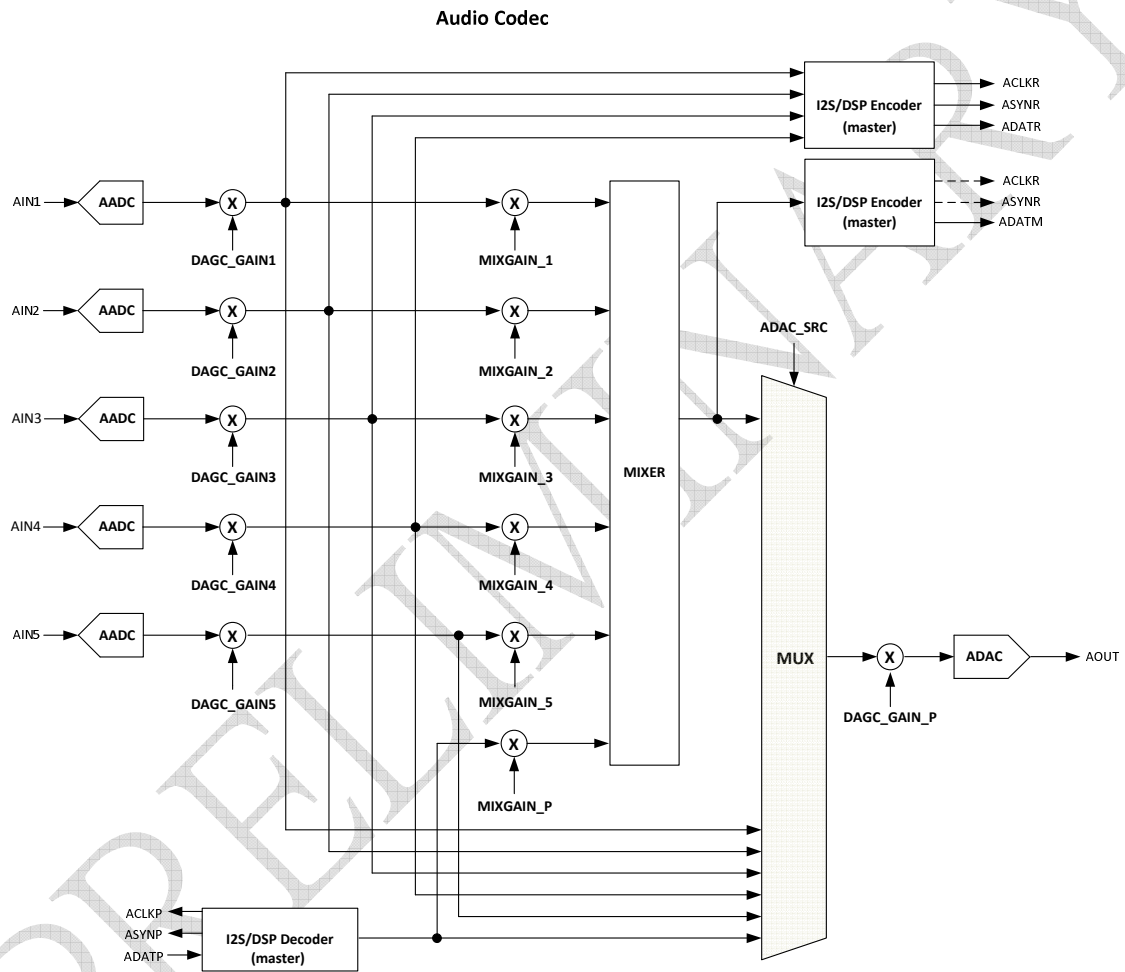


UV demodulation low pass filter



Audio CODEC

The audio codec in the DM5865 consists of five audio ADCs, one audio DAC, one audio mixer, one I2S/DSP decoder and two I2S/DSP encoders as shown below. The I2S/DSP decoder and encoders always operate in the master mode.



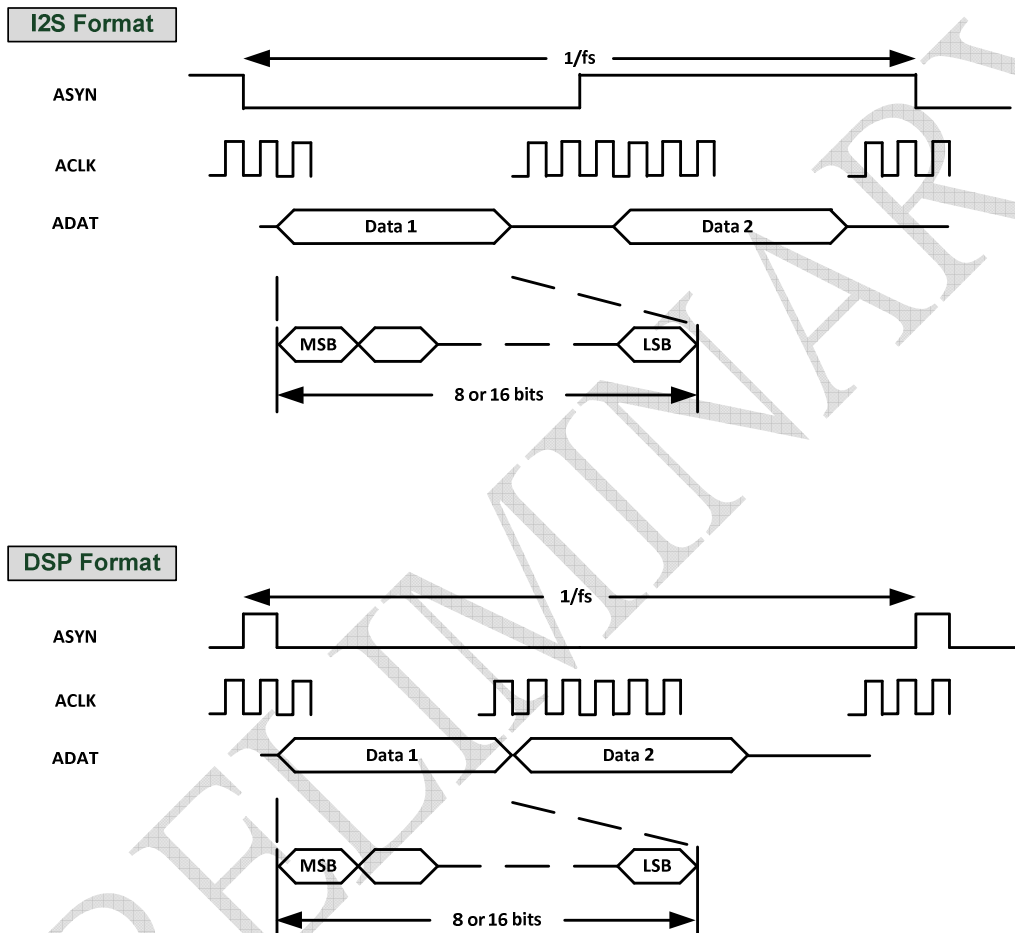
The I2S/DSP decoder is used for playback of digital input. It generates ACLKP and ASYNP signals and accepts serial data via ADATP from a slave device. The levels of the five analog audio inputs (AIN1 ~ AIN5) are programmable via the registers DAGC_GAIN1, DAGC_GAIN2, DAGC_GAIN3, DAGC_GAIN4 and DAGC_GAIN5. The six input audio sources can be mixed by the user-defined ratio specified by registers MIXGAIN_1, MIXGAIN_2, MIXGAIN_3, MIXGAIN_4, MIXGAIN_5, MIXGAIN_P. The mixed audio can be output through I2S/DSP encoder or DAC.

The codec provides three interfaces for audio output. The audio DAC can output analog audio for any one of the six input audio sources or the mixed audio. The analog output level is adjustable via register DAGC_GAIN_P. Two I2S/DSP encoders are present to output digital audio signal. The first one generates ACLKR, ASYNR and ADATR to output the 4 recorded audio inputs. The second encoder uses ADATM and shares the other two signals (ACLKR and ASYNR) to output the mixed audio.

The codec also supports audio cascade mode for multi-chip operation which will be described in a dedicated section.

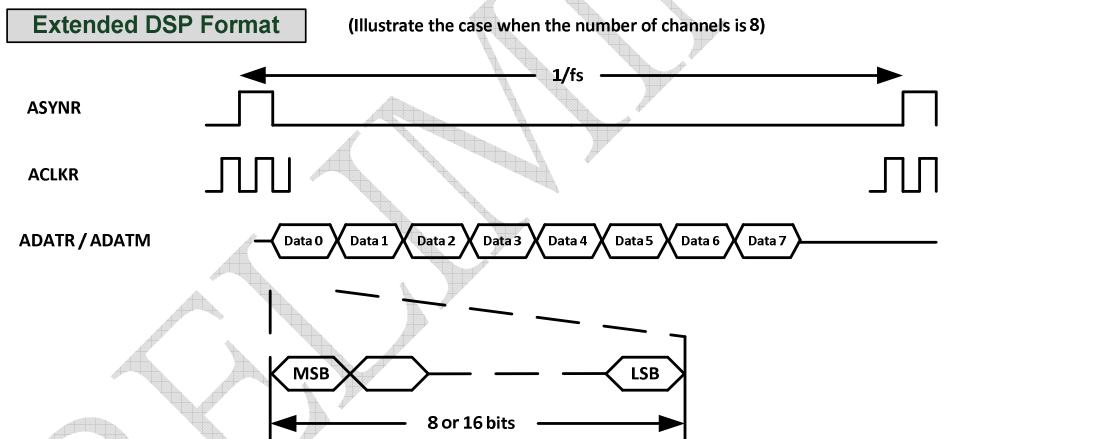
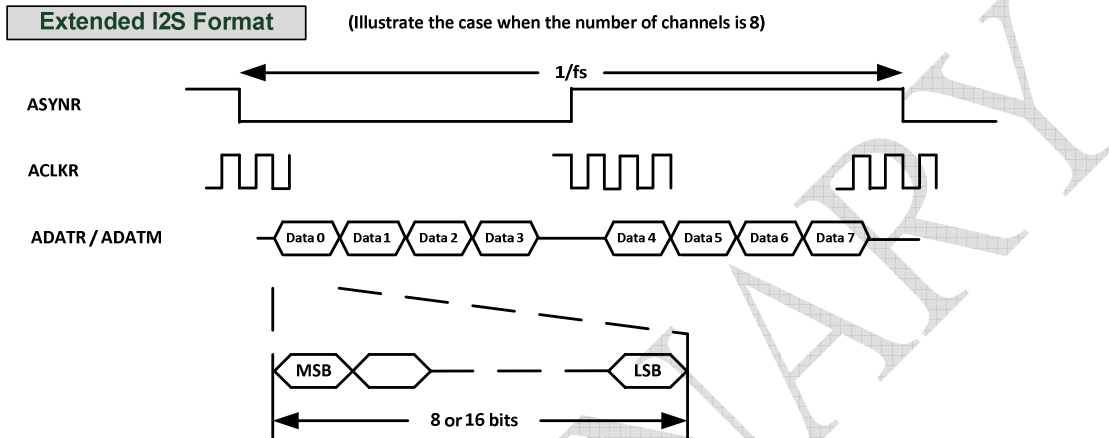
Digital Audio Format

The 3 digital audio interfaces (decoder for playback and encoder for record or mixing) follow the standard I2S or DSP protocol as shown below. Only master mode (codec being the master) is supported.



Extended Digital Audio Format

The digital audio encoders also support an extended I2S/DSP format to carry multiple audio channels through a single ADAT pin as shown below.



Cascade Mode for Multi-Chip Operation

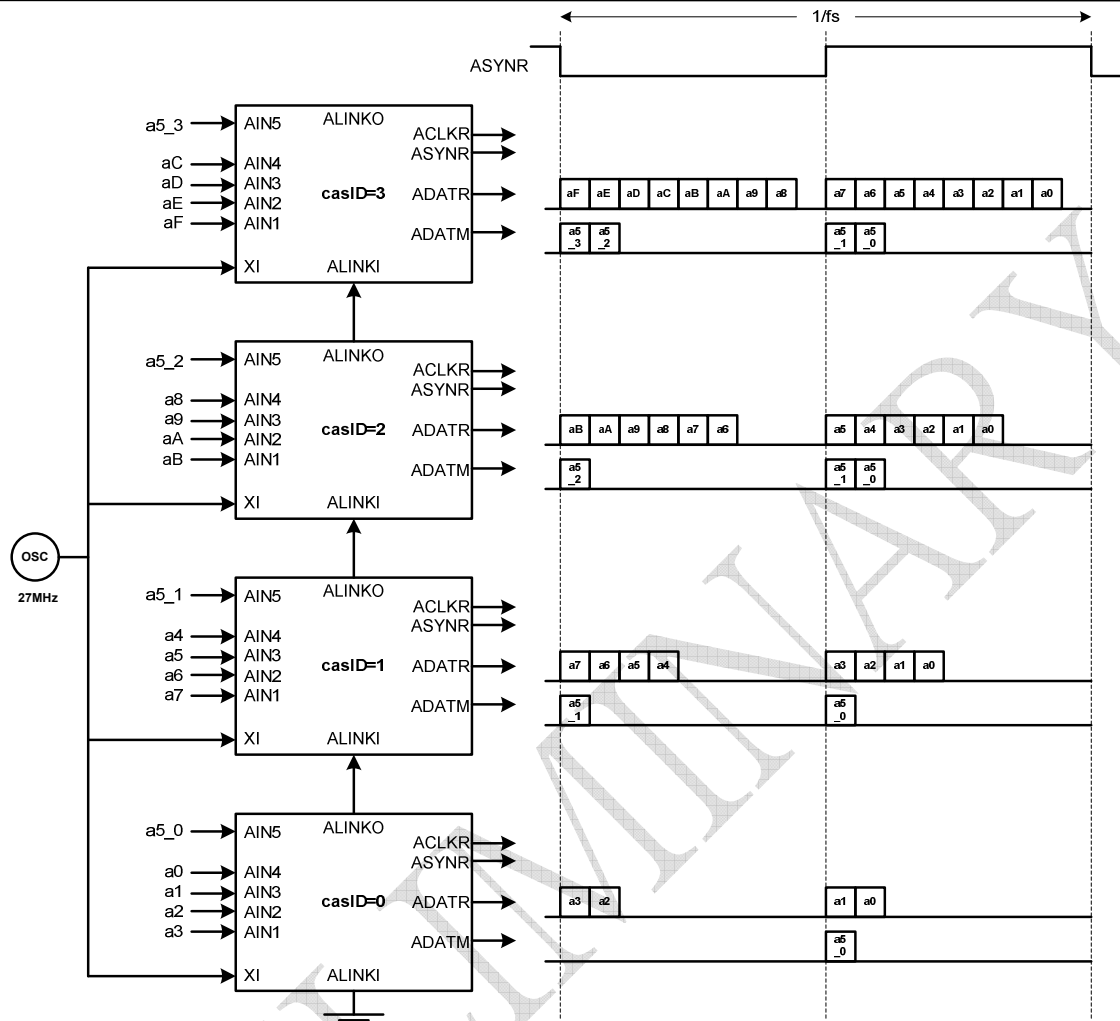
By using audio cascade mode, up to 16 analog audio sources can be cascaded and output through a single ACLKR/ASYNR/ADATR interface using the extended I2S/DSP format. Hence up to 4 chips can be cascaded in multi-chip application. A typical audio cascade system is shown below.

The table shown below summarizes the operation of audio cascade mode for various system configurations. Please note that 16-bit I2S/DSP data is not supported when using 16-channel cascade.

The analog audio input AIN5 can be optionally cascaded and output using the ADATM pin by setting the registers **MIXCASEN** and **ADATMOPT** as '1'.

	2-chip cascade (8 channels)		3-chip cascade (12 channels)		4-chip cascade (16 channels)	
	8-bit data	16-bit data	8-bit data	16-bit data	8-bit data	16-bit data
fs=48KHz	supported	supported	supported	supported	supported	prohibited
fs=24KHz	supported	supported	supported	supported	supported	prohibited
fs=16KHz	supported	supported	supported	supported	supported	prohibited
fs=8KHz	supported	supported	supported	supported	supported	prohibited

The Operation of Audio Cascade Mode for Various System Configurations



A Typical Audio Cascade System

<Note>

1. Here we use I2S mode as an example. The DSP mode works accordingly.
2. The waveform is a simplified version.
In real system the "ASYNR" signals in different cascade stages are not synchronous.

PLL

The DM5865 has two internal PLLs to generate the system and pixel clocks. A 27MHz is required for the PLLs.

The default PLL setting is shown in the following table.

	Crystal In clock (MHz)	PLL out (MHz)	Function
PLL1	27	144	System/pixel clock
PLL2	27	74.25	SMPTE 274M pixel clock

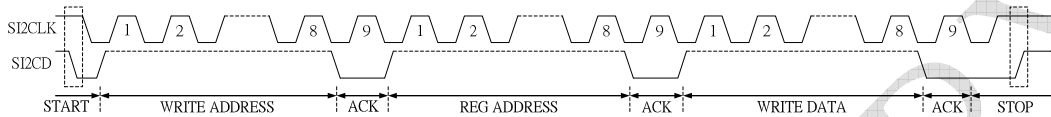
PLL default operated clock

The PLL parameters for various system configurations are shown in the following table.

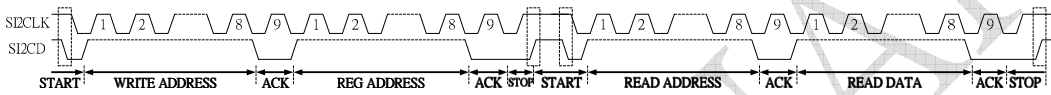
	Crystal(MHz)	PLL out(MHz)	M	N	OD
PLL1	27	144	64(62+2)	6(4+2)	1
	27	108	16(14+2)	2(0+2)	1
PLL2	27	144	64(62+2)	6(4+2)	1
	27	108	16(14+2)	2(0+2)	1
	27	74.25	22(20+2)	2(0+2)	2

Host Interface

In the DM5865, I²C is used for setting configuration and parameters, for example, brightness, contrast, saturation, hue, and sharpness control. The typical timing diagram of I²C write and read access is illustrated in the following figure.



Write operation of I²C bus



Read operation of I²C bus

Write/Read Address							
Slave Address						R/W	
1	1	0	0	0	SADD[1]	SADD[0]	0: Write; 1: Read

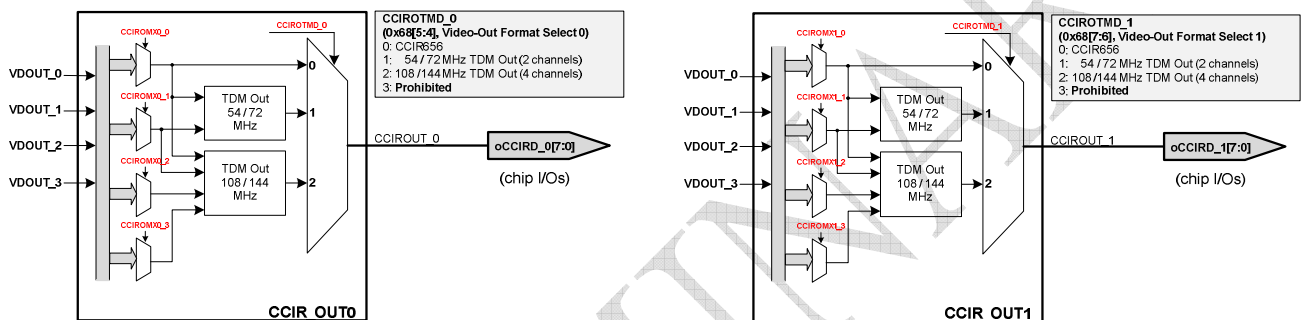
The external Pull-up/Pull-down resistors connected to the pins “DQ0” and “DQ1” indicate the device address SADD[1] and SADD[0]. When pull-up resistor is connected to DQ0 or DQ1, it indicates SADD[1] or SADD[0] with a high value. Otherwise when pull-down resistor is connected to DQ0 or DQ1, it indicates SADD[1] or SADD[0] with a low value.

	Write Address	Read Address
SADD[1:0]=2'h0	C0	C1
SADD[1:0]=2'h1	C2	C3
SADD[1:0]=2'h2	C4	C5
SADD[1:0]=2'h3	C6	C7

Chip-Level Output Unit

Three video output ports are available at chip level. The following figure depicts the data path of output ports.

The output ports are flexible in use. It can be programmed to output various output combinations. As shown in the figure, the register **CCIR0TM_X** is used to select up to 4 output videos from 6 possible sources. By programming register **CCIR0TM_X**, user can specify whether single channel (CCIR656/BT.1302), 2-channel TDM (@54 MHz), 4-channel TDM (@108 MHz).



CCIR0MX _{m,n} [2:0]	MUX Output
0	VDOUT_0
1	VDOUT_1
2	VDOUT_2
3	VDOUT_3

Video-Out Source Select (0x71 ~ 0x74, 0x9E ~ 0x9F)

<Note>

(1) VDOUT_0 ~ VDOUT_3 are from Video Decoder 0 ~ Video Decoder 3 respectively.

Data Path of Chip-Level Video Output Unit

Internal Control Registers

System Control

Address= 8'h64

System Control Page							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
				PAGE_3	PAGE_2	PAGE_1	PAGE_0

PAGE_0: VD space 0, to access VD_0 register please program this bit to 1.

PAGE_1: VD space 1, to access VD_1 register please program this bit to 1.

PAGE_2: VD space 2, to access VD_2 register please program this bit to 1.

PAGE_3: VD space 3, to access VD_3 register please program this bit to 1.

In case of register read, only one of the four bits can be set to 1.

Address= 8'h65

System Reset							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						RSTZ	TRSTZ

TRSTZ: When 1, reset whole chip except SW PLL, GPIO and Device ID setting. (WO)

RSTZ: When 1, reset all video decoders, TDM and audio interface. It also resets video decoder configurations.

Address= 8'h66

Global INT Mask							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDMAS K_3	VDMAS K_2	VDMAS K_1	VDMAS K_0

VDMASK_0: Enable INT from VD_0.

VDMASK_1: Enable INT from VD_1.

VDMASK_2: Enable INT from VD_2.

VDMASK_3: Enable INT from VD_3.

Address= 8'h67

Global INT Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDINT_3	VDINT_2	VDINT_1	VDINT_0

VDINT_0: VD_0 INT status. (RO)

VDINT_1: VD_1 INT status. (RO)

VDINT_2: VD_2 INT status. (RO)

VDINT_3: VD_3 INT status. (RO)

Address= 8'h68

CCIR656 IO Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		2'h0		0	0	0	0
CCIROTMD_1		CCIROTMD_0		CCIROE_3	CCIROE_2	CCIROE_1	CCIROE_0

CCIROE_0: Chip CCIR656_0 related 9 pins output enable.
When 1, output mode. When 0, input mode.

CCIROE_1: Chip CCIR656_1 related 9 pins output enable.
When 1, output mode. When 0, input mode.

CCIROE_2: Chip CCIR656_2 related 9 pins output enable.
When 1, output mode. When 0, input mode.

CCIROE_3: Chip CCIR656_3 related 9 pins output enable.
When 1, output mode. When 0, input mode.

CCIROTMD_0: Chip CCUROUT_0 output Mode type.

2'h0: CCIR656 output mode.

2'h1: 54Mhz TDM mode with D1 resolution for each channel.

2'h2: 108Mhz TDM mode with D1 resolution for each channel.

CCIROTMD_1: Chip CCUROUT_1 output Mode type.

2'h0: CCIR656 output mode.

2'h1: 54Mhz TDM mode with D1 resolution for each channel.

2'h2: 108Mhz TDM mode with D1 resolution for each channel.

Address= 8'h69

PIXCLK Polarity							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
OPIXCL K3_INV	OPIXCL K2_INV	OPIXCL K1_INV	OPIXCL K0_INV	OPIXCL K4_INV			

OPIXCLK4_INV: When 1, inverse output pixclk of CCIROUT_4.

OPIXCLK0_INV: When 1, inverse output pixclk of CCIROUT_0.

OPIXCLK1_INV: When 1, inverse output pixclk of CCIROUT_1.

OPIXCLK2_INV: When 1, inverse output pixclk of CCIROUT_2.

OPIXCLK3_INV: When 1, inverse output pixclk of CCIROUT_3.

Address= 8'h6A

IC Mode Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h0	
						CLKADCOPT	

CLKADCOPT: The VADC_1 input clock selection. (108MHz)

2'h0: The default value, sources from PLL1.

2'h1: Clock sources from PLL2.

2'h2: Clock source from chip pin NO.126.

Address= 8'h6B

Output Pixclk Delay Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
DLYMUX_PIXCLK1				DLYMUX_PIXCLK0			

DLYMUX_PIXCLK0: Programmable pixclk delay of CCIROUT_0.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

DLYMUX_PIXCLK1: Programmable pixclk delay of CCIROUT_1.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

Address= 8'h6C

VD Power Down							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDPWD N_3	VDPWD N_2	VDPWD N_1	VDPWD N_0

VDPWDN_0: When 1, VD 0 into power down mode.

VDPWDN_1: When 1, VD 1 into power down mode.

VDPWDN_2: When 1, VD 2 into power down mode.

VDPWDN_3: When 1, VD 3 into power down mode.

Address= 8'h6D

VD Power On Rstz							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDPRST 3	VDPRST 2	VDPRST 1	VDPRST 0

VDPRST0: Write 1, reset VD 0.

VDPRST1: Write 1, reset VD 1.

VDPRST2: Write 1, reset VD 2.

VDPRST3: Write 1, reset VD 3.

Address= 8'h6E

IP Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
VADCSEL			SW_VA DCBY PEN	SW_VA DCTST EN	SW_PLL BYPEN	SW_PLL TSTEN	SW_MBI SPATEN

SW_MBISTPATEN: When 1, drive MBIST detail signal to chip IO pins.

SW_PLLTSTEN: When 1, drive PLL out clocks to chip IO pins.

SW_PLLBYPEN: When 1, bypass internal pll out source.

SW_VADCTSTEN: When 1, drive VADCSEL indicated ADC outputs to chip IO pins.

SW_VADCBYPEN: When 1, bypass VADCBYPOPT indicated ADC with chip input ADC signals.

VADC_SEL: valid for SW_VADCTSTEN

3'h0: VADC_doutA=VADC_dout1, VADC_doutB=VADC_dout2

3'h1: VADC_doutA=VADC_dout3, VADC_doutB=VADC_dout4

3'h2: VADC_doutA= VADCMX0_0 =>[VADC_dout1/VADC_dout2] mux

VADC_doutA= VADCMX0_1 =>[VADC_dout3/VADC_dout4] mux

3'h3: will drive VADC_0 analog IP Do [15:1], selected signal to [VADC_doutA, VADC_doutB]

3'h4: will drive VADC_1 analog IP Do [15:1], selected signal to [VADC_doutA, VADC_doutB]

Address= 8'h6F

MBIST Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
BISTGO	MBDONE		MBERR_4	MBERR_3	MBERR_2	MBERR_1	MBERR_0

MBERR_0: When 1, memory of group 0 has error, Set by HW, write 1 to clear.

MBERR_1: When 1, memory of group 1 has error, Set by HW, write 1 to clear.

MBERR_2: When 1, memory of group 2 has error, Set by HW, write 1 to clear.

MBERR_3: When 1, memory of group 3 has error, Set by HW, write 1 to clear.

MBERR_4: When 1, memory of group 4 has error, Set by HW, write 1 to clear.

MBDONE: MBIST has finished self test, Set by HW, write 1 to clear.

BISTGO: Write 1 to start MBIST logic. HW auto clear this bit after MBIST done.

Address= 8'h71

CCIROUT_0 Otdm Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h1			0	3'h0		
	CCIROMX0_1				CCIROMX0_0		

CCIROMX0_0: The mux of CCIROUT_0's channel 0 at OTDM mode.

CCIROMX0_1: The mux of CCIROUT_0's channel 1 at OTDM mode.

Address= 8'h72

CCIROUT_0 Otdm Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h3			0	3'h2		
	CCIROMX0_3				CCIROMX0_2		

CCIROMX0_2: The mux of CCIROUT_0's channel 2 at OTDM mode.

CCIROMX0_3: The mux of CCIROUT_0's channel 3 at OTDM mode.

Address= 8'h73

CCIROUT_1 Otdm Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h1			0	3'h0		
	CCIROMX1_1				CCIROMX1_0		

CCIROMX1_0: The mux of CCIROUT_1's channel 0 at OTDM mode.

CCIROMX1_1: The mux of CCIROUT_1's channel 1 at OTDM mode.

Address= 8'h74

CCIROUT_1 Otdm Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h3			0	3'h2		
	CCIROMX1_3				CCIROMX1_2		

CCIROMX1_2: The mux of CCIROUT_1's channel 2 at OTDM mode.

CCIROMX1_3: The mux of CCIROUT_1's channel 3 at OTDM mode.

Address= 8'h75

IO/Clock Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
					ACLKPOE	ALINKOE	IRQOE

IRQOE: If using DQ14 as IRQ, set this bit as '1'

Otherwise, this bit is "don't care"

ALINKOE: If audio data is to be sent to next stage using audio cascade mode, set as '1'.

Otherwise, set as '0'

ACLKPOE: Set as '1' when I2S playback is to be enabled.

Address= 8'h77

CHIP Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
							PWRON

PWRON: Power On status. (RO)

Address= 8'h78

I2C Master Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hB8							
CH device address							

CH0~CH3: i2c slave device address. (R/W)

- DM5865 device address will be {4'hC,4'h0}
- I2CMaster_0: device address will be {4'hC,4'h2}
- I2CMaster_1: device address will be {4'hC,4'h4}
- I2CMaster_2: device address will be {4'hC,4'h6}
- I2CMaster_3: device address will be {4'hC,4'h8}
- For broadcast I2CMaster_CH0~I2CMaster_CH3, device address {4'HC,4'HE}

Address= 8'h79

I2CM status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	2'h0		0	0	0	0
	MI2CRD CMD	MI2CSEL		CHNAC K3	CHNAC K2	CHNAC K1	CHNAC K0

CHNACK0: CH0 I2C fail (RO, WC) .

CHNACK1: CH1 I2C fail (RO, WC) .

CHNACK2: CH2 I2C fail (RO, WC) .

CHNACK3: CH3 I2C fail (RO, WC) .

MI2CSEL: The device address is 0xCA and select which channel will be set.

-I2CMaster_CH0: device address will be {4'hC 4'ha} & {MI2CSEL=2'b00}.

-I2CMaster_CH1: device address will be {4'hC 4'ha} & {MI2CSEL=2'b01}.

-I2CMaster_CH2: device address will be {4'hC 4'ha} & {MI2CSEL=2'b10}.

-I2CMaster_CH3: device address will be {4'hC 4'ha} & {MI2CSEL=2'b11}.

MI2CRDCMD: When 1, the MI2C restart command enable.

Address= 8'h7F

SW FAST SWITCH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			OFASTS W_OPT	OFASTS W_SEL3	OFASTS W_SEL2	OFASTS W_SEL1	OFASTS W_SEL0

OFASTW_SEL0: valid when VD0 REG04[4]=1 and OFASTSW_OPT=1

set 0, select VIN1A as VD0 CVBS source

set 1, select VIN1B as VD0 CVBS source

OFASTW_SEL1: valid when VD1 REG04[4]=1 and OFASTSW_OPT=1

set 0, select VIN2A as VD1 CVBS source

set 1, select VIN2B as VD1 CVBS source

OFASTW_SEL2: valid when VD2 REG04[4]=1 and OFASTSW_OPT=1

set 0, select VIN3A as VD2 CVBS source

set 1, select VIN3B as VD2 CVBS source

OFASTW_SEL3: valid when VD3 REG04[4]=1 and OFASTSW_OPT=1

set 0, select VIN4A as VD3 CVBS source

set 1, select VIN4B as VD3 CVBS source

OFASTSW_OPT: valid when REG04[4]=1

Set 0, VD0-VD3 SW FASTSW control signal from OFASTSW_SEL0-
OFASTSW_SEL3

Set 1, VD0-VD3 SW FASTSW control signal from input pin
MPP0~MPP3

Video ADC

Address= 8'h80

Video ADC 0 Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	SW_sel_2		SW_sel_1		SWGAIN_0	pd_v2	pd_v1

pd_v1: Power down VIN1A & VIN1B, active high.

pd_v2: Power down VIN2A & VIN2B, active high.

SWGAIN_0: Software programs VADC 0's gain setting, active high. When low, the VADC 0' gain setting programmed by Hardware auto.

SW_sel_1: Software select active CVBS input. (0: VIN1A, 1: VIN1B)

SW_sel_2: Software select active CVBS input. (0: VIN2A, 1: VIN2B)

Address= 8'h81

Video ADC 0 Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hA				0	0	0	0
bias_vadc12				SvideoC_2B	SvideoC_2A	SvideoC_1B	SvideoC_1A

bias_vadc12: VADC 0's bias setting.

SvideoC_1A: Channel VIN1A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_1B: Channel VIN1B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_2A: Channel VIN2A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_2B: Channel VIN2B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

Address= 8'h82

Video ADC 0 Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SW_gain1B				SW_gain1A			

SW_gain1A: VIN1A's gain value, valid when REG80[2]=1.

SW_gain1B: VIN1B's gain value, valid when REG80[2]=1.

Minimum gain is set by 4'h0. Maximum gain is set by 4'hf.

The characteristic is the same as REG83

Address= 8'h83

Video ADC 0 Configuration 4							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SW_gain2B				SW_gain2A			

SW_gain2A: VIN2A's gain value, valid when REG80[2]=1.

SW_gain2B: VIN2B's gain value, valid when REG80[2]=1.

Address= 8'h84

Video ADC 0 Configuration 5							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
clmp1B				clmp1A			

Clmp1A: VIN1A's clamp value.

Clmp1B: VIN1B's clamp value.

The clamp can be used to adjust the sync tip value to the nominal value of 20.

Address= 8'h85

Video ADC 0 Configuration 6							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
Clmp2B				clmp2A			

Clmp2A: VIN2A's clamp value.

Clmp2B: VIN2B's clamp value.

Address= 8'h86

Video ADC 1 Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	SW_sel_4		SW_sel_3		SWGAIN_1	pd_v4	pd_v3

pd_v3: Power down VIN3A & VIN3B, active high.

pd_v4: Power down VIN3A & VIN3B, active high.

SWGAIN_1: Software programs VADC 1's gain setting, active high. When low, the VADC 1' gain setting programmed by Hardware auto.

SW_sel_3: Software select active CVBS input. (0: VIN3A, 1: VIN3B)

SW_sel_4: Software select active CVBS input. (0: VIN4A, 1: VIN4B)

Address= 8'h87

Video ADC 1 Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hA				0	0	0	0
bias_vadc34				SvideoC_4B	SvideoC_4A	SvideoC_3B	SvideoC_3A

bias_vadc34: VADC 1's bias setting.

SvideoC_3A: Channel VIN3A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_3B: Channel VIN3B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_4A: Channel VIN4A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

SvideoC_4B: Channel VIN4B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

Address= 8'h88

Video ADC 1 Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SW_gain3B				SW_gain3A			

SW_gain3A: VIN3A's gain value, valid when REG86[2]=1.

SW_gain3B: VIN3B's gain value, valid when REG86[2]=1.

Address= 8'h89

Video ADC 1 Configuration 4							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SW_gain4B				SW_gain4A			

SW_gain4A: VIN4A's gain value, valid when REG86[2]=1.

SW_gain4B: VIN4B's gain value, valid when REG86[2]=1.

Address= 8'h8A

Video ADC 1 Configuration 5							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
Clmp3B				Clmp3A			

Clmp3A: VIN3A's clamp value.

Clmp3B: VIN3B's clamp value.

Address= 8'h8B

Video ADC 1 Configuration 6							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
Clmp4B				Clmp4A			

Clmp4A: VIN4A's clamp value.

Clmp4B: VIN4B's clamp value.

Address= 8'h8C

Video ADC LPF Option							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h0		2'h0	
				lpf_34		lpf_12	

lpf_12: VADC 0 LPF selected.

lpf_34: VADC 1 LPF selected.

lpf_xx: 2'h0: 6MHz

2'h1: 9MHz

Others: bypass

Address= 8'h8D

VADC Clk Delay Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	DLYMUX_ANA34				DLYMUX_ANA12		

DLYMUX_ANA12: Programmable delay of digcore aclk_out0 from aclk_0.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

DLYMUX_ANA34: Programmable delay of digcore aclk_out1 from aclk_1.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

Address= 8'h8E

VADC Clk Delay Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
DLYMUX_ANA54				DLYMUX_ANA27			

DLYMUX_ANA27: Programmable delay of digcore aclk27_out from aclk27.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

DLYMUX_ANA54: Programmable delay of digcore aclk54_out from aclk54.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

Address= 8'h8F

VADC Digcore Config							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	3'h0		
					DLYMUX_VD		

DLYMUX_VD: Programmable delay of VD clk.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

PLL

Formula:

$$\text{CLK_OUT} = \text{XIN} * (\text{M}+2)/[(\text{N}+2)*\text{OD}*2]$$

Where CLK_OUT: PLL output frequency

XIN: PLL input frequency.

M: The numerator of PLL formula.

[N, OD]: The denominator of PLL formula.

Attention:

1. 100MHz <= CLK_OUT * OD <= 250MHz
2. 1MHz <= XIN/(N+2) <= 25MHz
3. OD >= 1

Truth Table:

PD	BP	OE	CLK_OUT
0	0	0	CLK_OUT
0	0	0	XIN
Don't Care	1	0	XIN
Don't Care	Don't Care	1	0
Other			Undefined

PD: Power down control; Active high.

BP: Bypass XIN to CLK_OUT; Active high.

OE: CLK_OUT enable pin, Active low.

Address= 8'h90

SW PLL Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SWPLL RST						SWPLL2	SWPLL1

SWPLL1: set PLL1 input configuration from SWPLL1_XX set, otherwise hard wired with chip default vale. (108MHz)

SWPLL2: set PLL2 input configuration from SWPLL2_XX set, otherwise hard wired with chip default vale. (74.25MHz)

SWPLL RST: set 1, chip will enter a reset mode waiting for PLL stable in 1ms. After that, SW needs to re-program all register setting except PLL configuration.

Address= 8'h91

SW PLL Config							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
		SWPLL2_OE	SWPLL1_OE	SWPLL2_PD	SWPLL2_BP	SWPLL1_PD	SWPLL1_BP

SWPLL1_BP: PLL1_BP SW program source.

SWPLL1_PD: PLL1_PD SW program source.

SWPLL2_BP: PLL2_BP SW program source.

SWPLL2_PD: PLL2_PD SW program source.

SWPLL1_OE: PLL1_OE SW program source.

SWPLL2_OE: PLL2_OE SW program source.

Address= 8'h92

SWPLL1_M							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
SWPLL1_M[7:0]							

SWPLL1_M: PLL1_M SW program source.

Address= 8'h93

SWPLL1_N							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	5'h0				
SWPLL1_M[8]			SWPLL1_N				

SWPLL1_N: PLL1_N SW program source

Address= 8'h94

SWPLL2_M							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
SWPLL2_M[7:0]							

SWPLL2_M: PLL2_M SW program source

Address= 8'h95

SWPLL2_N								
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit	
0	0	0	5'h0					
SWPLL2_M[8]			SWPLL2_N					

SWPLL2_N: PLL2_N SW program source

Address= 8'h96

SWPLL_OD							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
SWPLL2_OD				SWPLL1_OD			

SWPLL1_OD: PLL1_OD SW program source

SWPLL2_OD: PLL2_OD SW program source

DM5865 PLL SETTINGS Ref: 27MHz						
Ref: 27MHz	M	N	OD	PD	OE	BP
108 MHz	14	0	1	0	0	0
74.25 MHz	20	0	2	0	0	0

Audio ADC/DAC

Address= 8'hF0

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	ADAC_mute	ADAC_reset	ADAC_pd		AADC_test	AADC_reset	

AADC_reset: Audio ADC reset. (R/W: Active high)

AADC_test: Audio ADC test pin.

ADAC_pd: Audio DAC power down. (R/W: Active high)

ADAC_reset: Audio DAC reset. (R/W: Active high)

ADAC_mute: Audio DAC mute. (R/W: Active high)

Address= 8'hF1

Audio DAGC Config 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
AADC_DAGC_2				AADC_DAGC_1			

AADC_DAGC_1: Audio ADC 1 digital gain control.

AADC_DAGC_2: Audio ADC 2 digital gain control.

ADAC_DAGC_X[3:0], MIXGAIN_X[3:0]					
Set	Real Gain	dB	Set	Real Gain	dB
4'h0	0	-	4'h8	1.00	0
4'h1	0.125	-18.06	4'h9	1.25	1.94
4'h2	0.25	-12.04	4'hA	1.5	3.52
4'h3	0.375	-8.52	4'hB	1.75	4.86
4'h4	0.5	-6.02	4'hC	2.00	6.02
4'h5	0.625	-4.08	4'hD	2.25	7.04
4'h6	0.75	-2.50	4'hE	2.50	7.96
4'h7	0.875	-1.16	4'hF	2.75	8.79

Address= 8'hF2

Audio DAGC Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
AADC_DAGC_4				AADC_DAGC_3			

AADC_DAGC_3: Audio ADC 3 digital gain control.

AADC_DAGC_4: Audio ADC 4 digital gain control.

Address= 8'hF3

Audio DAGC Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
AADC_DAGC_P				AADC_DAGC_5			

AADC_DAGC_5: Audio ADC 5 digital gain control.

AADC_DAGC_P: Audio ADC digital gain control, source is selected from REGF8: ADAC_SRC .

Address= 8'hF4

Audio ADC Format							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h0		0	0
			AADC_MULCH	AADC_FSRATE		AADC_I2SMODE	

AADC_I2SMODE: (Digital I2S/DSP record interface): (master only)

1'b0: I2S mode

1'b1: DSP mode

AADC_FSRATE: (Digital I2S/DSP record interface)

2'b00: 48KHz

2'b01: 24KHz

2'b10: 16KHz

2'b11: 8KHz

AADC_MULCH: When 1, out 5 channels in record path.

When 0, out 2 channels in record path.

Address= 8'hF5

MIX Gain Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
MIXGAIN_2				MIXGAIN_1			

MIXOUT =

$$\begin{aligned} & \text{AIN1} * \text{ADC_DAGC_1} * \text{MIXGAIN_1} + \text{AIN2} * \text{ADC_DAGC_2} * \text{MIXGAIN_2} + \\ & \text{AIN3} * \text{ADC_DAGC_3} * \text{MIXGAIN_3} + \text{AIN4} * \text{ADC_DAGC_4} * \text{MIXGAIN_4} + \\ & \text{AIN5} * \text{ADC_DAGC_5} * \text{MIXGAIN_5} + \text{ADATP} * \text{MIXGAIN_P} \end{aligned}$$

Address= 8'hF6

MIX Gain Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
MIXGAIN_4				MIXGAIN_3			

Refer to REG F5

Address= 8'hF7

MIX Gain Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
MIXGAIN_P				MIXGAIN_5			

Refer to REG F5

Address= 8'hF8

Audio DAC Format							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	0	0	0
ADAC_T IME	ADAC_SRC			ADAC_FSRATE		ADAC_I 2SMOD E	ADAC_P RCH

ADAC_PRCH: When ADAC selecting the playback input source and PLAY_PRCH=0, ADAC chooses the playback left channel. Otherwise use playback right channel.

ADAC_I2SMODE: (Digital I2S/DSP playback interface): (mater only).

1'b0: I2S mode

1'b1: DSP mode.

ADAC_FSRATE: (Digital I2S/DSP playback interface):

2'b00: 48KHz

2'b01: 24KHz

2'b10: 16KHz

2'b11: 8KHz

DAC_SRC:

3'h0: ADATP (playback)

3'h1: MIXOUT

3'h2: AIN_1

3'h3: AIN_2

3'h4: AIN_3

3'h5: AIN_4

3'h6: AIN_5

ADAC_TIME:

When 1, use ADAC_FSRATE, ADAC mode to generate ACLKP/ASYNP.

Otherwise share the same timing signals with ACLKR/ASYNR.

Address= 8'hF9

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			AADC_p d5	AADC_p d4	AADC_p d3	AADC_p d2	AADC_p d1

AADC_pdX: Power down of Audio ADC X, active high.

Address= 8'hFA

Audio ADC/DAC Bias							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				4'h0			
ADAC_bias				AADC_bias			

ADAC_bias: Audio DAC's bias setting.

AADC_bias: Audio ADC's bias setting.

Address= 8'hFB

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
3'h0			0	0	0	2'h0	
AADCSEL			SW_AU DIOTST EN			VADCBYPOPT	

VADCBYPOPT: Video ADC bypass source option

2'b00: external A/B channel mode.

2'b01: external only A channel mode.

2'b10: external ADI mode.

SW_AUDIOTSTEN: When 1, chip enter to Audio Test mode, and drives Audio ADC/DAC test signal to I/O pins.

AADCSEL: Under Audio ADC test mode.

3'h0: AADC_1[15:0] selected to output pins.

3'h1: AADC_2[15:0] selected to output pins.

3'h2: AADC_3[15:0] selected to output pins.

3'h3: AADC_4[15:0] selected to output pins.

3'h4: AADC_5[15:0] selected to output pins.

Address= 8'hFC

Audio Cascade Mode Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		0	0	0	0	0	0
casID		SWCASLVLO	SWCASID	MIXCASEN	I2SRCASEN	ACASIE N	ACASOEN

casID and **SWCASLVLO** are effective only if (**SWCASID**=1). In this case SW should program these two registers to indicate the cascade ID of current stage. Please refer to the table below. If (**SWCASID**=0), these two registers are "don't care".

ID of Current Stage	SWCASLVLO	casID[1:0]
0	1'b1	2'b00
1	1'b0	2'b00
2	1'b0	2'b01
3	1'b0	2'b10

SWCASID: 0: The cascade ID is determined by HW logic.

1: The cascade ID is determined by SW through registers **casID** & **SWCASLVLO**.

MIXCASEN: When set as 1 the analog audio input AIN5 will be included in the cascade operation (using ADATM).

I2SRCASEN: 0: Audio cascade operation is disabled.

1: Audio cascade operation is enabled.

ACASIE N: 0: Cascade input pin (ALINKI) is disabled.

1: Cascade input pin (ALINKI) is enabled.

ACASOEN: Output enable control of cascade output pin (ALINKO). Active High.

Address= 8'hFD

Audio Cascade Mode Control and Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	2'h0	
FCLK_EN	I2SDATAWIDTH		ACASIDCHG	ACASACT	ACASIDVLD	ACASID	

FCLK_EN: Audio clock enable, active low.

I2SDATAWIDTH: 0: The I2S/DSP interface uses 16-bit data.

1: The I2S/DSP interface uses 8-bit data.

ACASIDCHG: (RO, Write One to Clear)

This flag is asserted when a change in **ACASID** is detected.

ACASACT: (RO)

This flag is asserted when audio cascade is in operation.

ACASIDVLD: (RO)

0: The value of the register **ACASID** is not valid.

1: The value of the register **ACASID** is valid.

ACASID: (RO) Indicate the cascade ID recognized by HW.

0: The ID of current stage is 1 or 0.

1: The ID of current stage is 2.

2: The ID of current stage is 3.

Address= 8'hFE

Mixed Audio Cascade & Audio Record 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
ADATM OPT						ADATR_2EN	

ADATMOPT: Set this bit the same value as **MIXCASEN**.

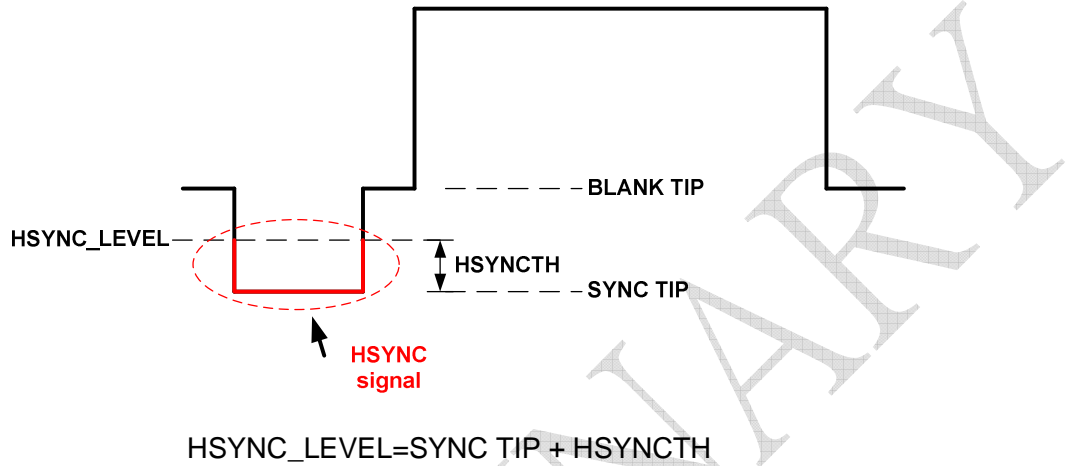
ADATR_2EN: Set as 1 to enable audio record channel 2 (using MI2CD1)

Address= 8'hFF

REVNUM							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h65							
REVNUM							

Video Decoder

HSYNC signal:



Address= 8'h00

VD Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	0	1	0
BBRSTZ	IFLDFASTSW	FASTSWEN	S_Video	ADC_A	ADI_ADC	EN	SRSTZ

SRSTZ: SW reset video decoder, WO

EN: Enable Video decoding function

S_Video: input signal is S-Video

FASTSWEN: Enable fast switch function

IFLDFASTSW: Set 1 : Fast switch boundary at every field end. Only Valid when REG04[3] : 1'b0.

Set 0: Fast switch boundary at frame end.

BBRSTZ: BB reset only, WO

Address= 8'h01

WATCHSEL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hf				0	0	2'b01	
AGC_LMT							

AGC_LMT: Analog AGC range

AGC

Address= 8'h02

AGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				1	0	1	1
AGC_gain					AGC_DT RACKE N	HWAGC EN	SYNCC AGCEN

SYNCCAGCEN: Set 1, enable CAGC gain update.

HWAGCEN: Hardware AGC enable

AGC_DTRACKEN: Dynamic sync tip tracking enable

AGC_gain: SW set AGC gain, RW

Address= 8'h03

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h63							
AGCDOWNTH[7:0]							

AGCDOWNTH: ADC couldn't larger than 867, if it is, will decrease the agc_gain.

Address= 8'h04

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	1	0	0	2'h3	
FASTSWOPT				OFASTSW		AGCDOWNTH[9:8]	

OFASTSW: Set 1: FASTSW control from input PIN(MPOUT).

Set 0: FASTSW source from internal logic related to FASTSWOPT, RW

FASTSWOPT: Set fast switch frame length ((FASTSWOPT+1)x8), RW

Video Detection Misc

Address= 8'h05

HSYNCTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
HSYNCTH							

HSYNCTH: Set horizontal sync threshold level

Address= 8'h06

Vdet_misc							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	0	1	1
MONOUT	MUKSEL			BLACKOUT	SETUP_7.5IRE	OCCIREN	ColorPOUT

ColorPOUT: Set 1, VD will drive Color panel when no video signal detected, otherwise drive black panel. Color panel setting see 0x2A[6:4]

OCCIREN: Set 1, VD will out CCIR656

SETUP_7.5IRE: Set 1, add 7.5 IRE to the BLANK_TIP

BLACKOUT: Set 1, VD will drive black panel or blue panel when no video signal detected.

MONOUT:force CCIR656 Cb=128, Cr=128

Color Killer

Address= 8'h08

ColorKill TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h20							
CBDIFFTH[7:0]							

CBDIFFTH: Set the color burst difference threshold

2D Comb Filter

Address= 8'h09

Com2D_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			FORCE_MONO		FORCE_VCOMB	NOTCH_FLTSEL	DIS_VC OMB

DIS_VCOMB: Set 1 to disable vertical comb filter

NOTCHFLTSEL: Set 0, use the wide band notchfilter

Set 1, use the narrow band notchfilter

FORCE_MONO: Set 1 to force the MONO signal mode.

Address= 8'h0C

PAL SW CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		0					0
Y_SHARP_GAIN							PALSW OPT

PALSWOPT: Set 1 to use standard pal switch define to demodulation.

For line lock camera, set this bit to 1.

Y_SHARP_GAIN:

2'h0 : no sharpness function

2'h1: sharpness gain 0.5

2'h2: sharpness gain 1

2'h3: sharpness gain 2

Address= 8'h10

VD Decoder status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
PAL_Nc	PAL- I,B,B1,G ,H,D/ PAL_N	PAL_M	PAL_60	NTSC- 443	NTSC- J/NTSC- M	COLOR KILL_52 5	COLOR KILL_62 5

The register show the video decoded status

RO. Set 1 to enable SW force mode.

Address= 8'h11

VD_STS							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
CLKLOCK_STST							DET_NONILT

DET_NONILT: RO. Detect the non-interlaced signal format.

CLKLOCK_STST: RO. Clock offset lock status

Address= 8'h12

DAGC_LMT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h3				4'hf			
CLKOFF_LOCK				DAGC_LMT			

DAGC_LMT: Digital AGC range

CLKOFF_LOCK: Clock offset locking function. 4'h0: always tracking

Others: clock offset lock within CLKOFF_LOCK * 8 ppm.

Address= 8'h13

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	1	1	0	1	0	0	1
SWFAR 54MD	HWFAR 54OPT	GAINLOCK_OPT	CLKOFFDIS	CBADJ	BLANK_SHIFTEN	ALINELOCK	CLKOFF_TRACKEN

CLKOFF_TRACKEN: CLKOFFSET tracking enable

ALINELOCK: active line lock option, fixed line start position.

BLANK_SHIFTEN: set 1, blank level will be modified according to color burst mean value per line.

CBADJ: Color burst adjust

CLKOFFDIS: Disable clock offset tracking function

GAINLOCK_OPT: Enable gain locking function after 16 frame decoded.

HWFAR54OPT: Set 1, FAR4FS will operate in 54Mhz when detecting 4.43 subcarrier

SWFAR54MD: Software force FAR4FS operate in 54Mhz.

Address= 8'h14

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	1	0	1
		LLCFASTMD			VDETOP T	LTRACK OPT	CLKLO CKOPT

CLKLOCKOPT: Set 0 : Always tracking clock offset when
 $\text{abs}(\text{clkoffset}) > \text{CLKOFF_LOCK} (\text{REG12}[7:4])$
 Set 1 : keep tracking until first time
 $\text{abs}(\text{clkoffset}) < \text{CLKOFF_LOCK}(\text{REG12}[7:4])$

LTRACKOPT: Set 1: Hardware continues active line (video) decoding when miss valid HSYNC signal until video loss.
 Set 0: Hardware performs active line (video) decoding until valid HSYNC signal detected.

VDETOPT: Set 1: using rising edge of HSYNC signal as line detection timing.
 Set0: using falling edge of HSYNC signal as line detection timing.
 For long cable application, set this bit to 1.

LLCFASTMD[1:0]:
 Line lock Auto Detection stable period. Valid when $\text{REG3B}[5]=1$.

Set 0: check line lock mode right after decode started

Set 1: check line lock mode after 8 frames decoded.

Set 2, 3: check line lock mode after 16 frames decoded.

Address= 8'h15

CLKOFF_CTL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	1	0	0
					CLKFRACEN	FIXHSYNC_MD L	SWFIXCLOCKOFF

SWFIXCLOCKOFF: Set 1, SW fixed clock offset. Force clock offset value=

{REG25[4:0],REG24[7:0],REG23[7:0]}.

FIXHSYNC_MD: Set 1, fixed the HSYNC_LEVEL to be REG05 HSYNCTH.

CLKFRACEN: Set 1, enable fraction clock offset tracking.

Address= 8'h17

CTI gain							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	6'd10					
HMIDTR ACK							

HMIDTRACK: Set 1: tracking BLANK TIP each line at Front Porch Blanking position (REG4B[7:0]).

Set 0: tracking BLANK TIP at CVBS serration period.

Address= 8'h18

LOWTRACK							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
FSHYBC OPT	DISCOL KILL		NONINT EN	CAGCO PT	TRHSYN COPT	LOWTR ACK	TRHSYN CTH

TRHSYNCTH: Set 1: enable HW auto update HSYNCTH during video detection.

Set 0: use fix HSYNCTH (REG05[7:0]) during video detection.

LOWTRACK: Set 1: tracking SYNC TIP per line(s) from LOWLEVEL TRACKER.

Set 0: tracking SYNC TIP at CVBS serration period.

TRHSYNCOPT: Set 1: use fix HSYNCTH (REG05) during video detection

Set 0: enable HW auto update HSYNCTH during video detection.

CAGCOPT: Set 1 to enable color AGC.

NONINTEN: Set 1 to enable auto detect non-interlaced singal.

DISCOLKILL: Set 1 to disable auto detect color kill mode

FSHYBCOPT: ONLY valid under FASTSWEN.

Set 1: Keep previous tracked HSYNCTH

Set 0: use REG05 as HSYNCTH

Address= 8'h20

AGC gain							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
DAGC Gain				AAGC Gain			

AAGC Gain: Analog AGC gain setting, RO

DAGC Gain: Digital AGC gain setting, RO

Address= 8'h21

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SYNC_TIP[7:0]							

SYNC_TIP: RO

Address= 8'h22

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
BLANK_TIP[7:0]							

BLANK_TIP: RO

Address= 8'h23

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
CLKOFF[7:0]							

CLKOFF: RO, internal 2's compliment clock offset tracking status. Unit (ppm)

Address= 8'h24

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
CLKOFF[15:8]							

CLKOFF: RO, internal 2's compliment clock offset tracking status. Unit (ppm)

Address= 8'h25

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			SYNC_TIP[20:16]				

SYNC_TIP: RO

Address= 8'h26

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				BLANK_TIP[9:8]		SYNC_TIP[9:8]	

BLANK_TIP: RO

SYNC_TIP: RO

Address= 8'h29

Blue Panel Select							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						PALBLP ANL	NTSCBL PANL

PALBLPANL: Valid when REG06[3]=1. When no signal, SW sets PAL blue panel out.

NTSCBLPANL: Valid when REG06[3]=1. When no signal, SW sets NTSC blue panel out.

When PALBPANL=0, NTSCBLPANL=0. HW takes PAL as default mode.

Address= 8'h2A

VD_MISC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h2	
ColorOut						MPP_OPT	

MPP_OPT: (Enable when GPOSEL (REG7A[7]) = 1'b1)

2'h0: drive field info to pin.

2'h1: drive Active info to pin.

2'h2: drive NOVID info to pin.

2'h3: drive FASTSW_SEL info to pin.

VD_MPP signal pin out:

(VD0,VD1,VD2,VD3)→(MI2CD0, MI2CD1, MI2CD2, MI2CD3)

ColorOut: valid when REG06[3]=1 and REG06[0]=1.

3'h0: blue panel

3'h1: red panel

3'h2: white panel

3'h3: green panel

3'h4: magenta panel

3'h7: color rotation mode, blue → red →

white → green → magenta → black → blue...

Color Process

Address= 8'h2B

COLOR_EXT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	2'h1		0	0	0	1
	CCIRBL ANKOP T					NTSC_C CIREXT	EXT_CO LOR

EXT_COLOR: Set 1, Y/Cb/Cr value from 8'h1~8'hfe

NTSC_CCIREXT: Set 1 in NTSC mode, CCIR656 output 487 active line.

CCIRBLANKOPT: Set 1: output blanking period close to standard CCIR656.

Set 0: with short V blank lines before active field start.

Address= 8'h2C

Hue							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
Hue[7:0]							

Hue: Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

Address= 8'h2D

Saturation							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h10							
Saturation							

Saturation: unsigned, Range : 0 ~ 15.9375

8'hff : maximum, about x16 color intensity.

8'h00: (no color)

Address= 8'h2E

Contrast							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h80							
Contrast							

Contrast: unsigned, Range : 0~255

255: maximum (x2) contrast

128: original signal (x1)

0: minimum contrast

Address= 8'h2F

Brightness							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h00							
Brightness							

Brightness: signed

127: brightest

0: darkest

Address= 8'h30

INT Mask							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1_MASK	VLOST_1_MASK	VDET_1_MASK		MDCHG_0_MASK	VLOST_0_MASK	VDET_0_MASK

VDET_0_MASK: Set 1, enable register 0x31 VDET_0 interrupt function, RW

VLOST_0_MASK: Set 1, enable register 0x31 VLOST_0 interrupt function, RW

MDCHG_0_MASK: Set 1 enable register 0x31 MDCHG_0 interrupt function, RW

VDET_1_MASK: Set 1 to enable register 0x31 VDET_1 interrupt function, RW

VLOST_1_MASK: Set 1 enable register 0x31 VLOST_1 interrupt function, RW

MDCHG_1_MASK: Set 1 enable register 0x31 MDCHG_1 interrupt function, RW

Address= 8'h31

INT status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1	VLOST_1	VDET_1		MDCHG_0	VLOST_0	VDET_0

VDET_0: when detect video signal, the interrupt set, set by HW, set 1 to clear

VLOST_0: when lose video signal, the interrupt set, set by HW, set 1 to clear

MDCHG_0: when detect video signal change, the interrupt set, set by HW, set 1 to clear

VDET_1: valid for fast switch mode channel B, when detect video signal, the interrupt set, set by HW, set 1 to clear

VLOST_1: valid for fast switch mode channel B, when lose video signal, the interrupt set, set by HW, set 1 to clear

MDCHG_1: valid for fast switch mode channel B, when detect video signal change format, the interrupt set, set by HW, set 1 to clear

Address= 8'h33

HUE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						Hue[9:8]	

Hue: Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

Address= 8'h34

FIELD OPTION							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
					FIELD_I NV	FIELD_ ONLY	

FIELD_ONLY: CCIR656 signal output field 0 only

FILED_INV: Inverse output CCIR656 signal field

Address= 8'h35

Chroma Average							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
						CAVNTS CMD	CAVPAL MD

CAVNTSCMD: Set 1, enable NTSC mode Cb/Cr line average.

Set 0, disable.

CAVPALMD: Set 1, enable PAL mode Cb/Cr line average.

Set 0, disable.

Address= 8'h36

MASK CCIR656 LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
						MASKALL	PAL_MSK3

PAL_MSK3: Set 1, it will mask field 0 and 1 last lines according to REG37

MASKALL: mask all active

Address= 8'h37

MASK LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h3			0	3'h3		
	MSK_LINE_F1				MSK_LINE_F0		

MSK_LINE_F0: When REG36[0] = 1, Mask Field 0 last number of active lines (0-7)

MSK_LINE_F1: When REG36[0] = 1, Mask Field 1 last number of active lines (0-7)

Address= 8'h38

MONO TH								
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit	
1	0	0	5'd31					
MONO_EN			MONO_TH					

MONO_TH: MONO mode AGC threshold. AGC max value 30. when set MONO_TH 31.

AGC will always less than MONO_TH.

MONO_EN: Set 0, when no valid color burst detected.

Output CCIR656 Y through Notch filter.

Set 1, when no valid color burst detected. Output CCIR656

Y through Notch filter if AGC_GAIN >= MONO_TH, otherwise output CCIR656 Y with ADC data.

When No valid color burst detected (color kill mode). Output

CCIR656 Cb/Cr with 128 (no color).

Address= 8'h39

COLOR BURST DETECT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h4			4'h5			
	COLBSTCYC			COLBSTHSEL			

COLBSTHSEL: Color Burst detection threshold.

4'h0: COLBSTH = 0.125*(BLANK TIP – SYNC TIP)

4'h1: COLBSTH = 0.25*(BLANK TIP – SYNC TIP)

4'h2:COLBSTH = 0.375*(BLANK TIP – SYNC TIP)

4'h3:COLBSTH = 0.5*(BLANK TIP – SYNC TIP)

4'h4:COLBSTH = 0.09375*(BLANK TIP – SYNC TIP)

4'h5:COLBSTH = 0.078125*(BLANK TIP – SYNC TIP)

4'h6:COLBSTH = 0.0625*(BLANK TIP – SYNC TIP)

4'h7:COLBSTH = 0.03125*(BLANK TIP – SYNC TIP)

4'h8:COLBSTH = 0

When color burst peak to peak value larger than COLBSTHSEL, it's been considered a good color burst signal cycle.

COLBSTCYC: When COLBSTCYC numbers of valid color burst cycle detected, VD will decode video with color and Color AGC will optionally started. Otherwise will enter color kill mode.

Address= 8'h3A

CAGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	0	0
CAGCE N	CAGCL OCKOP	cagc_gain					

cagc_gain: RO. Chroma gain value. [5:2] integer, [1:0] fractional.

(max 15.75, min 1)

CAGCLOCKOPT: Set 1, enable color AGC tracking until CAGC gain stable.

Set 0, color AGC tracking for first 15 video decoded frames.

CAGCEN : Set 1, enable color AGC.

Address= 8'h3B

Line Lock Camera								
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit	
0	0	0	0	0	0	0	0	
CAMLOCKOPT	LOCKCAM_DET	HLOCKDET1	ACTSHIFT					

ACTSHIFT: Active region shift, 2's complement (-16~15)

HLOCKDET1: Set 1, to enable auto-detect Line Lock camera.

LOCKCAM_DET: RO, Line lock camera detected. (RO)

CAMLOCKOPT: Set 1, when line lock camera used.

Address= 8'h3C

LLOCKTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'd20							
LLOCKTH							

LLOCKTH: Line Lock auto detection threshold, valid only when 0x3B[5]=1.

When REG13[1]=1, line boundary difference within a field larger than LLOCKTH, Line Lock Camera detected.

Note: when clock offset tracking unstable and REG13[1]=1, line boundary difference might be large within a field.

Address= 8'h3D

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	ORSTO PT	OBFOV F	OBFUD F	LLFAR4 FSOPT1			LLFAR4 FSOPT

LLFAR4FSOPT: Set 1, decode video chroma without clock offset compensation.

Set 0, decode video chroma after clock offset compensation.

Set this bit to one for Line Lock Camera.

LLFAR4FSOPT1: Set 1, Auto adjust the active region related to clock offset.

When force line lock mode, set this bit to 1;

OBFUDF: RO. CCIR output buffer under flow.

OBFOVF: RO. CCIR output buffer over flow.

ORSTOPT: Set 1, Reset CCIR output buffer when output buffer overflow or underflow.

Address= 8'h3D

OUT BUFFER							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h1a							
OBFTH							

OBFTH: CCIR656 output buffer ready threshold.

Once CCIR656 output buffer count is larger than

OBFTH, starts output CCIR656 active region.

PS. CCIR656 output buffer max length is 48, set OBFTH around middle level of buffer length.

Address= 8'h40

CCIROUT TYP EN							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
		H_SAV_ACT	CROPEN		FLDCHIDEN	EAVCHIDEN	SWCHIDEN

SWCHIDEN: Valid when REG00[5]=1(FASTSWEN). Add SW channel ID

in first 4 data of active line, valid at fast switch mode.(field/frame)

EAVCHIDEN: Valid when REG00[5]=1(FASTSWEN) Add channel ID in EAV[3:0] and SAV[3:0], valid at fast switch mode. (field/frame)

FLDCHIDEN: Valid when REG00[6:5]=2'h3 (**IFLDFASTSW**, FASTSWEN), output CVBS source A to field 0, output CVBS source B to field 1.

CROPEN: Video cropping function enable.

H_SAV_ACT: Set 1, HSYNC signal will include SAV data, otherwise HSYNC signal only at active region.

Address= 8'h41

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		2'h3		2'h0		2'h0	
H_STR[9:8]		H_ACT[9:8]		V_STR[9:8]		V_ACT[9:8]	

H_STR[9:8]: It defined the number of pixels start after SAV.

H_ACT[9:8]: It defined the number of active region.

V_STR[9:8]: It defined VSYNC start after active region line.

V_ACT[9:8]: It defined the number of VSYNC during active region.

$H_STR + H_ACT < \text{total number of pixels per line.}$

$V_STR + V_ACT < \text{total number of lines per field.}$

Address= 8'h42

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
H_STR[7:0]							

Address= 8'h43

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hC0							
H_ACT[7:0]							

Address= 8'h44

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
V_STR[7:0]							

Address= 8'h45

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'd240							
V_ACT[7:0]							

Address= 8'h46

Cb/Cr Slicer							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1					3'h2		
SLICER_EN					SLICER_RANGE		

SLICER_EN: CB/CR coring function enable.

SLICER_RANGE: Coring range (0 ~7). When $128 - \text{SLICER_RANGE} < (\text{CB/CR}) < 128 + \text{SLICER_RANGE}$, force the Chroma value to 128.

Address= 8'h4B

BLANK1TIP							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hdc							
BLANK1TIP							

BLANK1TIP: valid when REG17[7]. Line Blanking sample position.

Address= 8'h4C

HSYNLOWCYC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	7'd20						
HSYNLOWCYC							

HSYNLOWCYC: When low level (signal smaller than HSYNC LEVEL) signal exists over HSYNLOWCYC, it's considered as a HSYNC signal Candidate.

Address= 8'h4D

LMARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
LMARG27							

LMARG27: Sync signal detect margin after video detect.

Address= 8'h4E

MARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
MARG27							

MARG27: Sync signal detect margin before video detect.

Electrical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range

Supply voltage range: IOV _{DD} to DGND
.....
DV _{DD} to DGND
.....
PLL_AV _{DD} to PLL_AGND
..
CH1_AV _{DD} to CH1_AGND
...
Digital input voltage range, V _I to DGND
Input voltage range, XTAL1 to PLL_GND
Analog input voltage range A _I to CH1_AGND
Digital Output voltage range, V _O to DGND
Operating free-air temperature, TA

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
IODV _{DD}	Digital I/O supply voltage	2.97	3.3	3.63	V
DV _{DD}	Digital supply voltage	1.62	1.8	1.98	V
PLL_AV _{DD}	Analog PLL supply voltage	1.62	1.8	1.98	V
CH1_AV _{DD}	Analog core supply voltage	1.7	1.8	1.9	V
V _{I(P-P)}	Analog input voltage (ac-coupling necessary)	0.25		1.0	V
V _{IH}	Digital input voltage high	2		5	V
V _{IL}	Digital input voltage low	-0.3		0.8	V
V _{IH_XTAL}	XTAL input voltage high	0.7 PLL_AV _{DD}			V
V _{IL_XTAL}	XTAL input voltage low		0.3 PLL_AV _{DD}		V
I _{OH}	High-level output current			2	mA
I _{OL}	Low-level output current			-2	mA
I _{OH_SCLK}	SCLK high-level output current			4	mA
I _{OL_SCLK}	SCLK low-level output current			-4	mA
T _A	Operating free-air temperature	-40		125	°C

Crystal Specifications

CRYSTAL SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		27.0/36.0		MHz
Frequency tolerance		±100		ppm

Electrical Characteristics

$V_{DD} = 1.8\text{ V}$, $PLL_AV_{DD} = 1.8\text{ V}$, $CH1_AV_{DD} = 1.8\text{ V}$, $IOV_{DD} = 3.3\text{ V}$

For minimum/maximum values: $T_A = 0^\circ\text{C}$ to 70°C , and for typical values: $T_A = 25^\circ\text{C}$ unless otherwise noted

DC Electrical Characteristics

PARAMETER	TEST CONDITIONS (see NOTE 1)	MIN	TYP	MAX	UNIT
$I_{DD(I/O_D)}$ Digital I/O supply current	Color bar input		4.8		mA
$I_{DD(D)}$ Digital core supply current	Color bar input		50.7		mA
$I_{DD(PLL_A)}$ Analog PLL supply current	Color bar input		5.9		mA
$I_{DD(CH1_A)}$ Analog PLL supply current	Color bar input		26.1		mA
P_{TOT} Total power dissipation, normal mode	Color bar input		165	205	mW
P_{DOWN} Total power dissipation, power-down mode	Color bar input			5	mW
C_i Input capacitance	By design		8		pF

V_{OH}	Output voltage high	$I_{OH} = 2 \text{ mA}$	$0.8 IOV_{DD}$	V
V_{OL}	Output voltage low	$I_{OL} = -2 \text{ mA}$	0.2 2 IOV_{DD}	V
V_{OH_SCLK}	SCLK output voltage high	$I_{OH} = 4 \text{ mA}$	2 \cdot 3	V
V_{OL_SCLK}	SCLK output voltage low	$I_{OL} = -2 \text{ mA}$	0 \cdot 6	V
I_{IH}	High-level input current	$V_I = V_{IH}$	± 50	μA
I_{IL}	Low-level input current	$V_I = V_{IL}$	± 50	μA

NOTE 1: Measured with a load of 15 pf.

Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_i	Input impedance, analog video inputs	By design	500			$k\Omega$
C_i	Input capacitance, analog video inputs	By design		10		pF
$V_{i(pp)}$	Input voltage range *	$C_{coupling} = 0.1 \mu\text{F}$	0.25		1	V
ΔG	Gain control range			12		dB
DNL	DC differential non-linearity	A/D only		± 2		LSB
INL	DC integral non-linearity	A/D only		± 3		LSB
Fr	Frequency response	6 MHz		-0.9	-3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-		50		dB

		p		
NS	Noise spectrum	50% flat field	50	dB
DP	Differential phase		1.5	°
DG	Differential gain		0.5%	

* The 0.75-V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistors are 37.4 Ω.

Timing

Clocks, Video Data, Sync timing

Data Format : CCIR656 output					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PIXCLK High pulse duration	t_{hw}	18.5			ns
PIXCLK Low pulse duration	t_{lw}	18.5			ns
CCIR656 data out setup time	t_{su}	18.5			ns
CCIR656 data out hold time	t_h	18.5			ns

Output:CCIR656

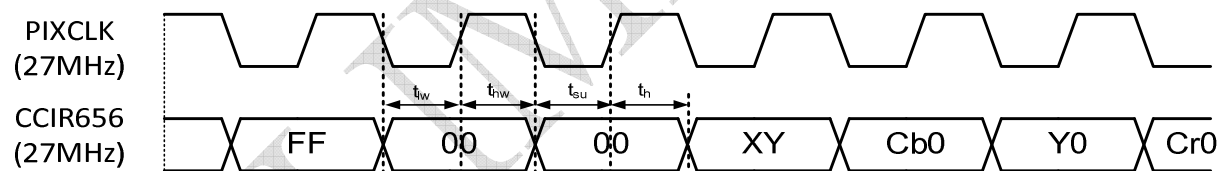
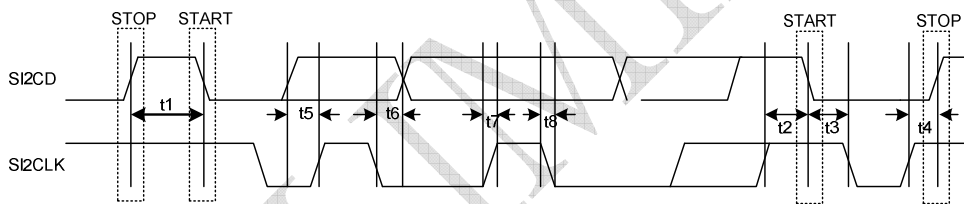


Figure 3-2 . Clocks, CCIR656 Output Data Timing

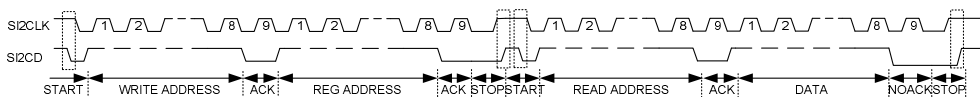
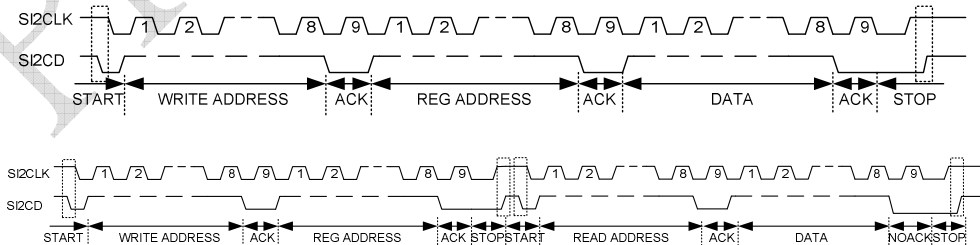
Data Format : CCIR656 input					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PIXCLK High pulse duration	t_{hw}	18.5			ns
PIXCLK Low pulse duration	t_{lw}	18.5			ns
CCIR656 data out setup time	t_{su}	18.5			ns
CCIR656 data out hold time	t_h	18.5			ns

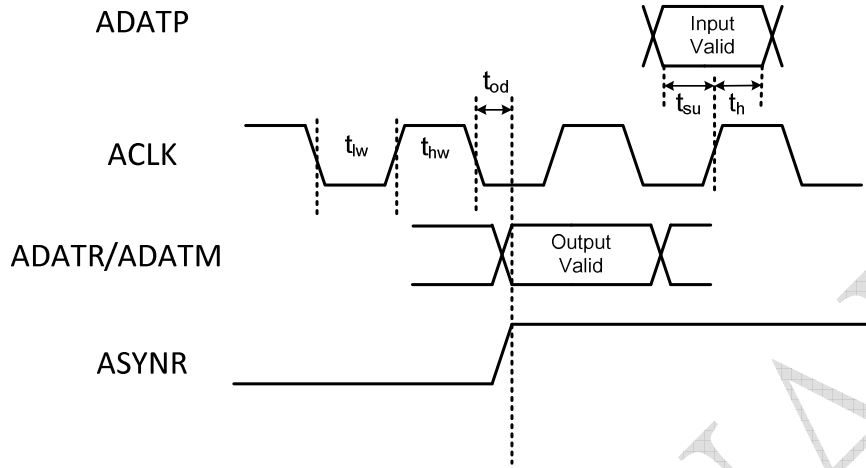
I²C Host Port Timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t₁ Bus free time between STOP and START		1.3			μs
t₂ Setup time for a (repeated) START condition		0.6			μs
t₃ Hold time (repeated) START condition		0.6			μs
t₄ Setup time for STOP condition		0.6			μs
t₅ Data setup time		200			ns
t₆ Data hold time		0		50	ns
t₇ Rise time I2CD and I2CLK signal		250			ns
t₈ Fall time I2CD and I2CLK signal			250		ns
C_b Capacitive load for each bus line				120	pF
f_{I2C} I ² C clock frequency				400	kHz



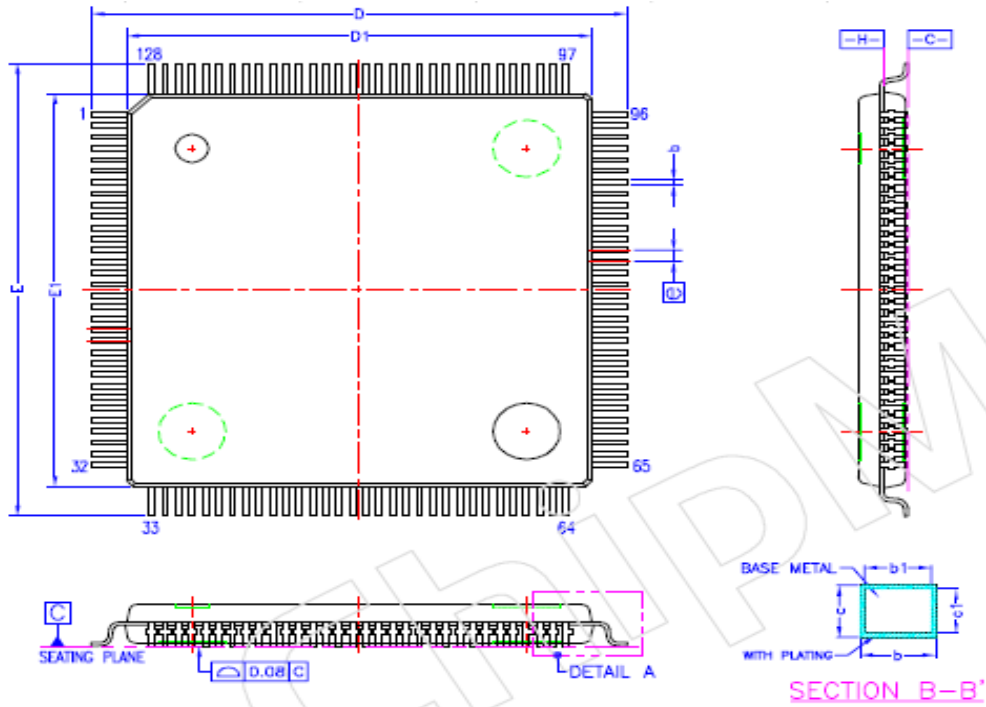
	Write Address	Read Address
SADD[0] Pull low SADD[1] Pull low	C0	C1
SADD[0] Pull high SADD[1] Pull low	C2	C3
SADD[0] Pull low SADD[1] Pull high	C4	C5
SADD[0] Pull high SADD[1] Pull high	C6	C7



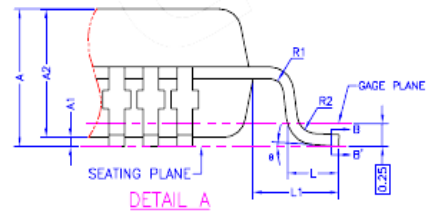
AC Characteristic of Digital Audio Interface


		Min	Typ	Max	Unit
t_{lw}	clock low time				ns
t_{hw}	clock high time				ns
t_{od}	output delay time				ns
t_{su}	input setup time				ns
t_h	input hold time				ns

Packaging



SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.008
D	15.90	16.00	16.10	0.626	0.630	0.634
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
[B]	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.040 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
ø	ø	3.5"	7"	ø	3.5"	7"



- REFER TO JEDEC STD. MS-026
- DIMENSION D AND E ARE DETERMINED AT SEATING PLANE [C].
- DIMENSION D1 AND E1 ARE DETERMINED AT DATUM [H].
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS WHICH INCLUDE MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm
- ALL DIMENSIONS ARE IN MILLIMETERS.



DM5865

720H 4 channels NTSC/PAL Decoder

Ordering Information

Part Number	Pin Count	Package
DM5865EP	128	LQFP (Pb-Free and Halogen-Free)

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.

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DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.