DAVICOM Semiconductor, Inc.

DM5900

720H 1 channel NTSC/PAL Decoder with fast switch function

DATA SHEET

Preliminary
Version: DM5900-DS-P01
February 27, 2013

REVISION HISTORY:

Date	Revision	Description
2012/03/19	1.1	Initial release

Table of Contents

Introduction

The DM5900 is a 1-channel video decoder designed for cameras with 720H CCD sensor. The DM5900 converts 6.5 MHz analog CVBS signals to digital 27 MHz CCIR656 signals. The DM5900 integrates an internal PLL. The DM5900 also features a patented fast switch function. With the fast switch function, the DM5900 can decode up to 2 analog CVBS with little frame rate loss.

Features

Video Decoder

- Accepts NTSC (M), PAL (B, D, G, H, I, M, Nc).
- Video decoder could be programmed to operate at 27MHz.
- Hardware Fast Switch function
- Fast Switch also controllable by software or external pin
- Software channel ID in active region
- 10-bits video ADCs with built in 6.5 MHz analog low pass filter
- Automatic gain control for Luminance and Chrominance
- Programmable brightness, contrast, saturation, hue, and sharpness
- 5-H comb filter for YC separation
- Support video interface YCbCr 4:2:2, 4:1:1, 4:2:0 format
- Support mirror function
- Chrominance line filter for PAL phase error
- DLL for video synchronization, supports 27MHz crystal within +/-1000 ppm variance
- Advanced video synchronization for weak and noisy CVBS. Supports video signal transmitted by 500-meter long cable
- Support line lock camera

Miscellaneous

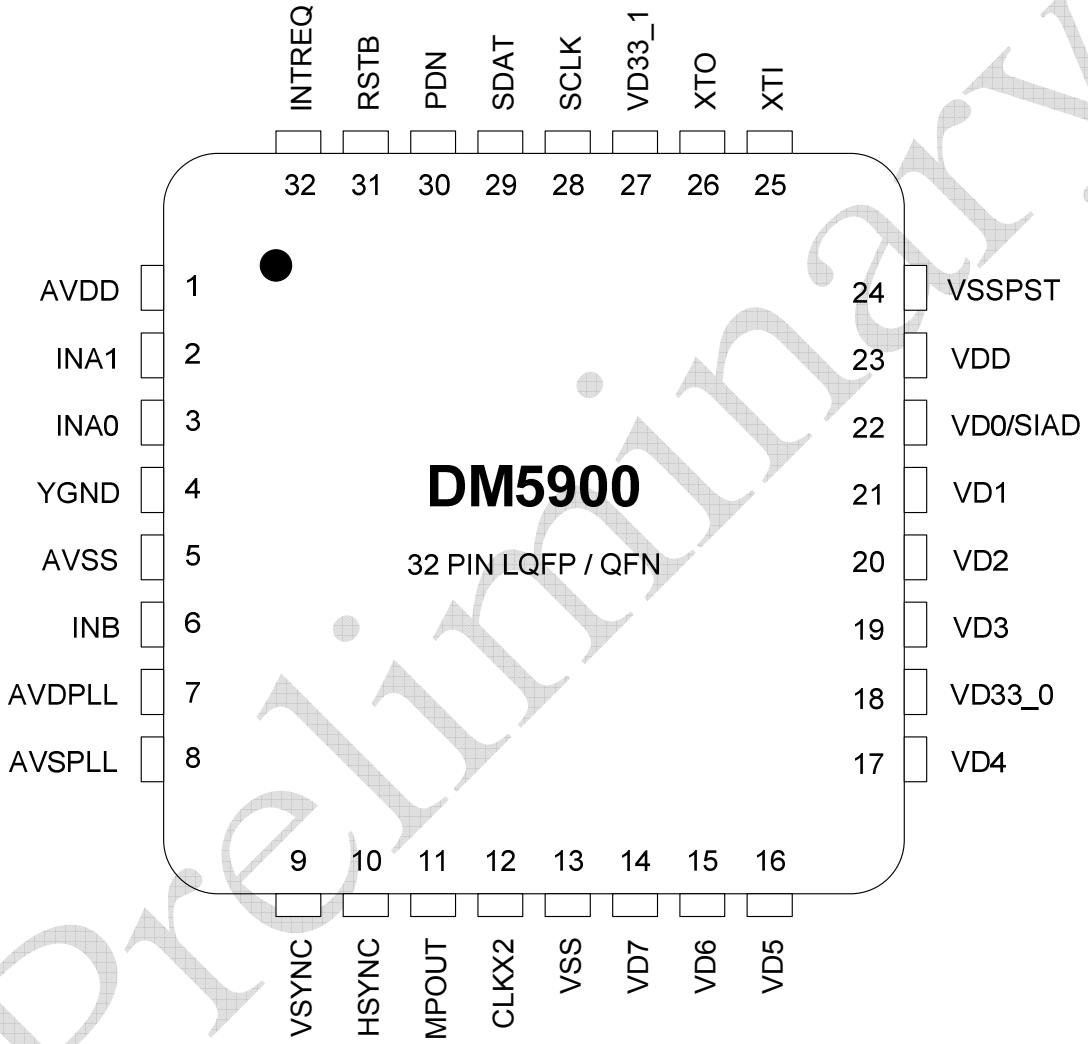
- Use a single external 27MHz crystal to support 720H video
- One programmable PLL integrated
- Slave I2C bus
- Ultra low power consumption. Under 150mW for normal operation. Under 50mW for suspend mode.
- 32-pin LQFP (5mmx5mm) or 32-pin QFN (4mmx4mm) package
- 1.8V core power, 3.3V analog power and 1.8V analog power

Applications

Suggested applications include

- DVR
- Car DVR
- Video capture card

Terminal Assignment



Terminal Functions

Pin Name	Pin number	Type	Description
Analog Video Signals			
INA0	3	A	Analog input A0.
INA1	2	A	Analog input A1.
YGND	4	G	Analog ground. (used as signal input reference)
INB	6	A	Analog input B. (analog chroma input)

Pin Name	Pin number	Type	Description
Video Output Signals			
HSYNC	10	O	Horizontal Sync and multi-purpose output. See register for control information.
VSYNC	9	O	Vertical Sync and multi-purpose output. See register for control information.
CLKX2	12	O	Data output clk.
MPOUT	11	O	Multi-purpose output pin. See register for control information.
VD7,VD6,VD5, VD4,VD3,VD2, VD1	14,15,16,17, 19,20,21	I/O	Digital Video data output of 4:2:2 YCbCr[7:1]. VD[7] is the MSB
VD0/SIAD	22	I/O	Digital Video data output of 4:2:2 YCbCr. SIAD: The i2c interface address select pin 0. Default pull-down device ID: 8'hB8 otherwise device ID is 8'hBA

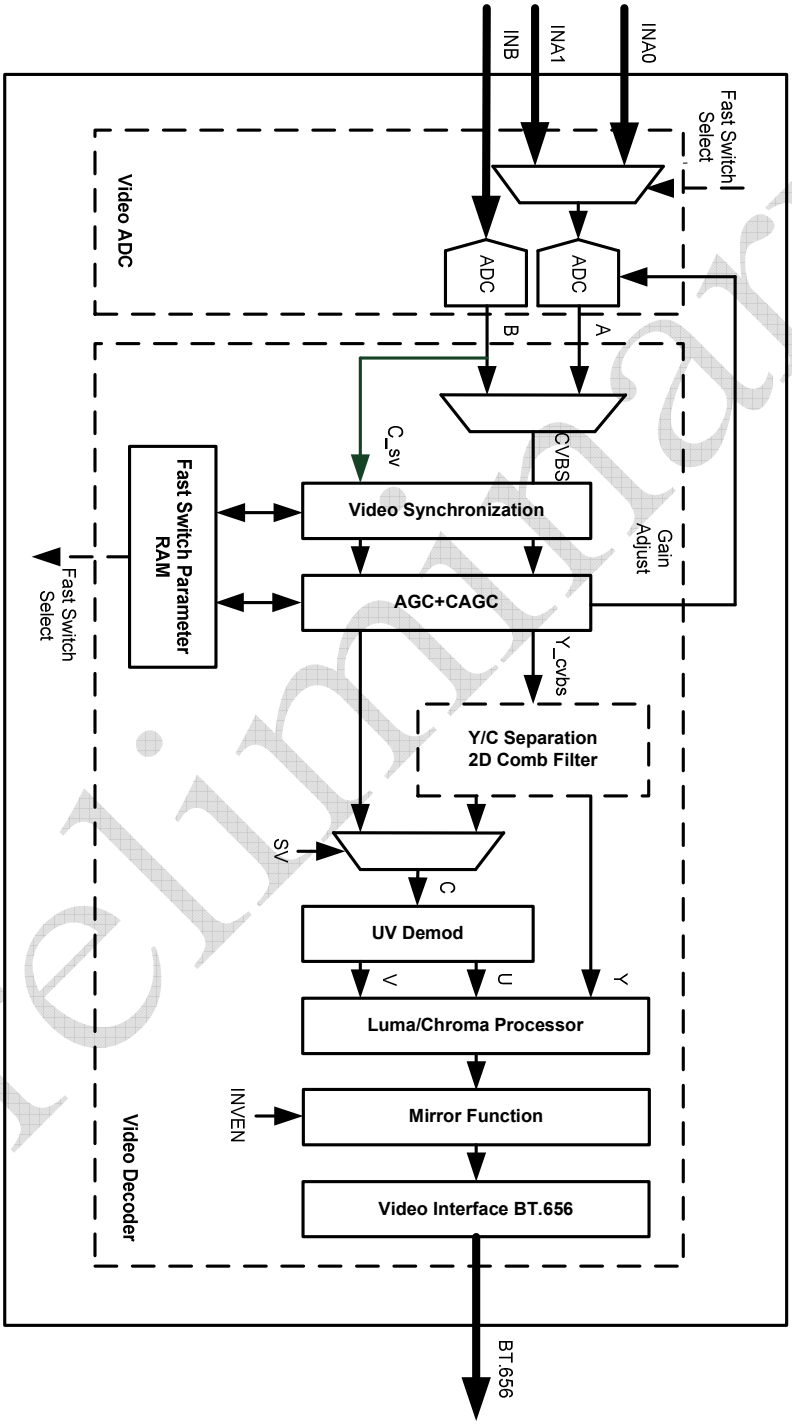
Pin Name	Pin number	Type	Description
Clock signals			
XTI	25	I	Clock input. A 27 MHz fundamental crystal or a single-ended oscillator can be connected
XTO	26	O	Clock output. For connecting a crystal

Pin Name	Pin number	Type	Description
General Signals			
RSTB	31	I	Reset input. Low active
PDN	30	I	Power down control pin. # is high active
INTREQ	32	O	Interrupt output signal

Pin Name	Pin number	Type	Description
Host Interface			
SCLK	28	I	The I2C serial interface Clock line.
SDAT	29	I/O	The I2C serial interface Data line.

Pin Name	Pin number	Type	Description
Power and Ground Pins			
VDD	23	P	1.8V digital core power
VSS	13	G	1.8V digital ground
VD33_0	18	P	3.3V digital I/O power
VD33_1	27	P	3.3V digital I/O power
VSSPST	24	G	3.3V digital I/O ground
AVDD	1	P	1.8V analog supply ADC.
AVSS	5	G	Analog ground.
AVDPLL	7	P	1.8V analog supply PLL
AVSPLL	8	G	Analog ground PLL

Block Diagram



Introduction

The DM5900 video decoder contains a Video Synchronization block, an AGC block, an YC separation block, a UV Demodulation block, a Luma/Chroma Processor block, a Mirror Function block and a BT 656 output block. A patented Fast Switch is also included.

In addition to CVBS, the DM5900 video decoder supports S-Video as well.

Video Synchronization

Video Synchronization performs video detection function. It automatically detects NTSC(M), NTSC(443), PAL(B,D,G,H,I), PAL(M), PAL(N), PAL(60). A smart video detection algorithm has been adopted. Therefore the DM5900 can perform fast and stable video synchronization even if the input signal is weak or the external crystal is with error as large as +/- 1000 ppm.

Automatic Gain Control

Automatic Gain Control (AGC) block performs both Luma AGC and Chroma AGC (CGAC). After video synchronization, Luma AGC adjusts input Luma level to the standard level (1Vpp). A further CAGC is performed after Luma AGC for signal with different Luma and Chroma attenuation.

Y/C Separation

Y/C Separation is for CVBS input only. After this block CVBS signal is separated into Luma and Chroma components. A 5-H 2D comb filter is adapted in the Y/C separation block.

UV demodulation

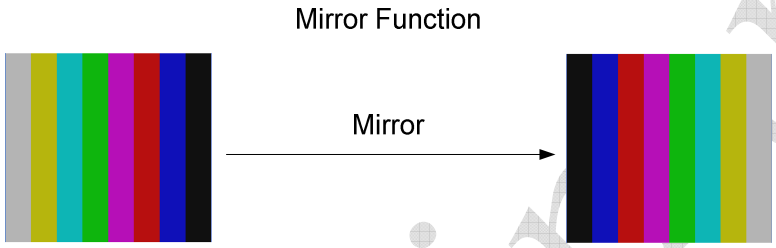
After Y/C separation, the UV demodulation block performs UV demodulation to the Chroma component. The phase and frequency of the UV demodulation is from a color burst subcarrier tracking block for both NTSC and PAL mode. A UV demodulation LPF is also adopted to filter out chroma noise.

Luma/Chroma Processor

This block contains a programmable Luma sharpness filter. Hue, Saturation, Brightness and Contrast adjustment are also supported. The adjusted video is then transformed from YUV to YCbCr domain for CCIR656 output interface.

Mirror Function

The DM5900 also supports mirroring function. When mirroring function is performed, the samples at each line are horizontally left-right flipped. The following figure illustrates the result of horizontal mirroring.



Video Interface

The DM5900 video decoder supports 27MHz BT.656 video output format with BT.601 synchronization signals. It also supports YCbCr 4:1:1 and 4:2:0 formats. A horizontal cropping function also included in this block.

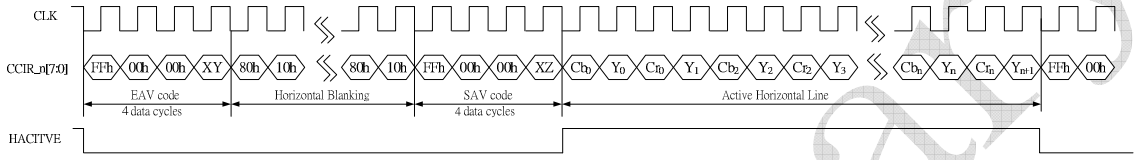
Fast Switch Parameter RAM

The DM5900 features a patented hardware video source fast switch function. The Fast Switch block has a table which stores video characteristic. Each time HW switches to a previously tracked video source it could complete video synchronization within several lines. With this feature, the DM5900 can decode up to 2 CVBS with little frame rate loss.

Video Interface

The DM5160 outputs 27MHz CCIR656 with 720x480/720x576 resolution (conventional 720H). For these video outputs, SAV (Start of Active Video) and EAV (End of Active Video) are inserted to indicate active video interval. Each channel uses one output port to transmit video data, that is, luminance and chrominance data are transmitted through the same port. The output timing diagram is shown below.

YCbCr 4:2:2

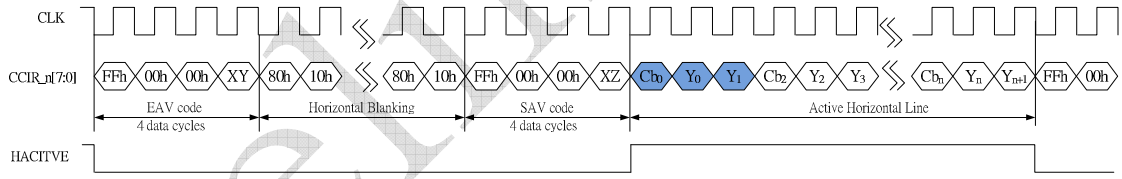


The number of data cycles in active horizontal line will vary according to the output YCbCr 4:2:2 format. For video outputs, the active horizontal line contains 1440 cycles.

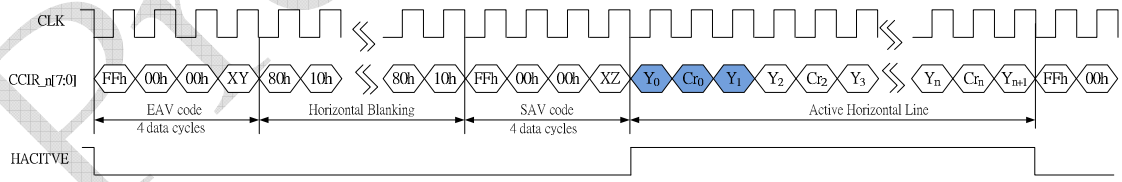
The DM5900 also supports the 4:2:0 and 4:1:1 format. The output timing diagram is shown below.

YCbCr 4:2:0

Odd Line:

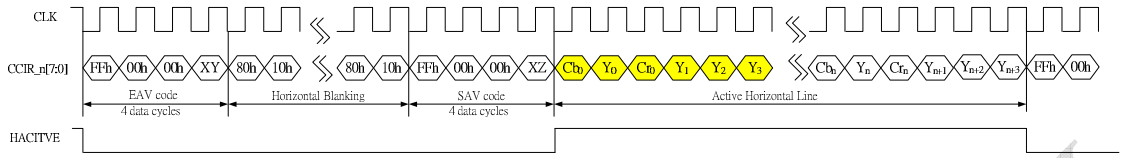


Even Line:



The number of data cycles in active horizontal line will vary according to the output YCbCr 4:2:0 format. For video outputs, the active horizontal line contains 1080 cycles.

YCbCr 4:1:1



The number of data cycles in active horizontal line will vary according to the output YCbCr 4:1:1 format. For video outputs, the active horizontal line contains 1080 cycles.

SAV and EAV indicate the active video interval. The values of the first three bytes in SAV and EAV are invariant preamble: 0xFF, 0x00, and 0x00. Different values are designated to the last byte according to different conditions: Field, V time, and H time. The MSB of this byte is always set to 1 and it's followed by three bits to represent the condition of F, V, and H respectively. The last four bits are used as protection bits. The detailed code sequences of SAV and EAV are illustrated in the following table.

Condition			FVH Value			SAV/EAV Code Sequence			
Field	V time	H time	F	V	H	Byte 0	Byte 1	Byte 2	Byte 3
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1

BT601 Synchronization Signals

External syncs are provided via the following signals

- VSYNC (vertical sync signal)
- HSYNC (horizontal sync signal)
- FID (field indicator)

VSYNC, HSYNC and FID are programmed to be the external syncs for BT.601. The default setting for a 525/625 line video output are given as an example below.

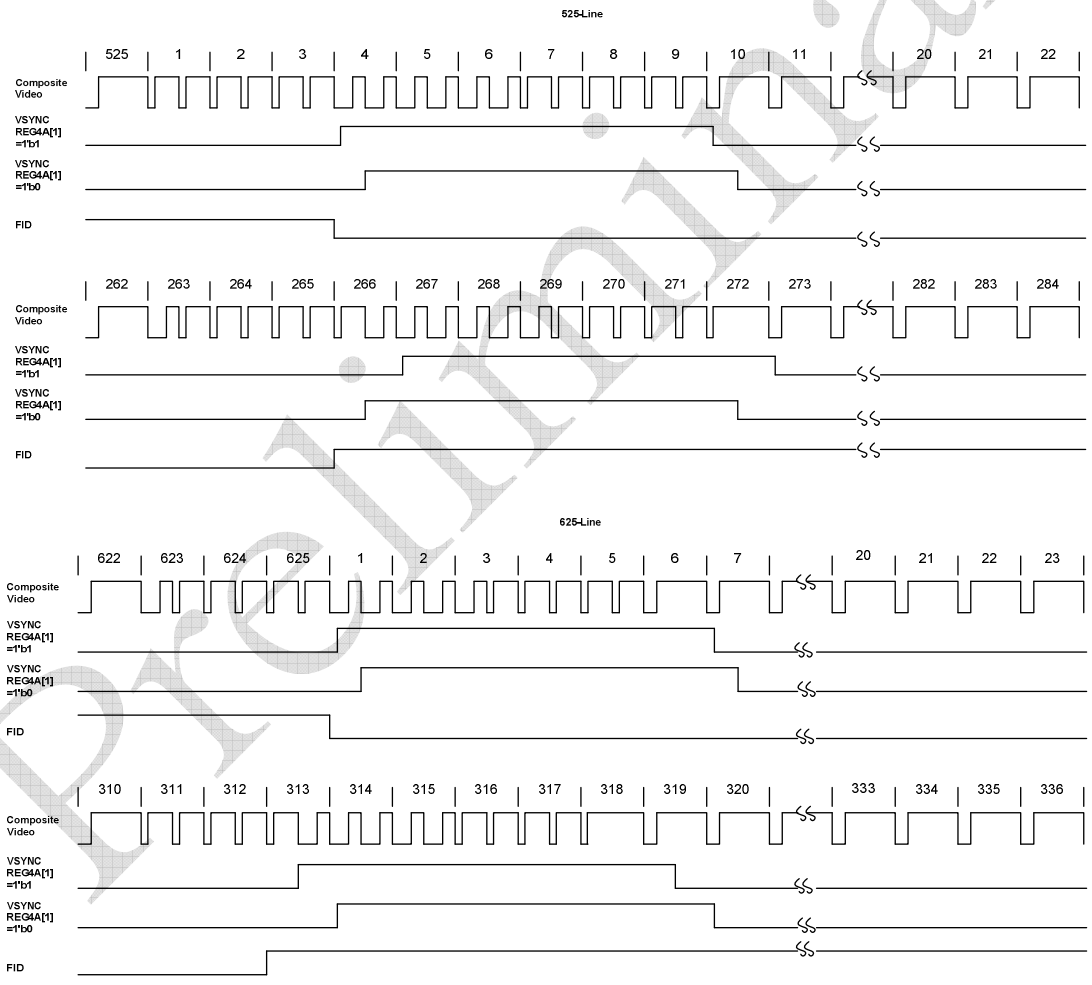
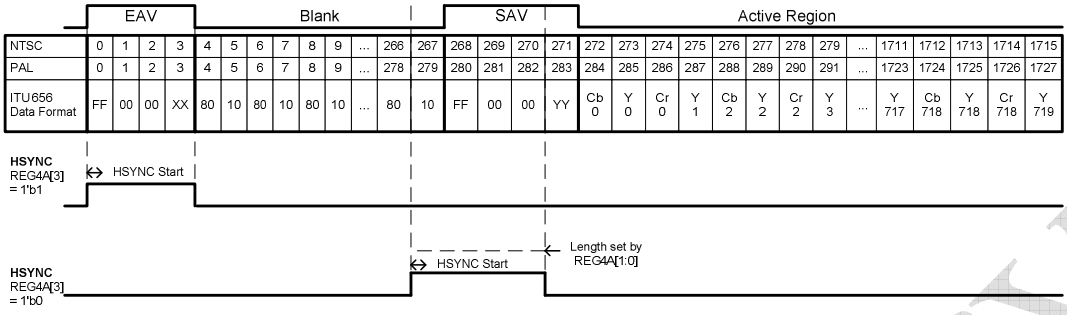


Fig: BT 601 Timing diagram

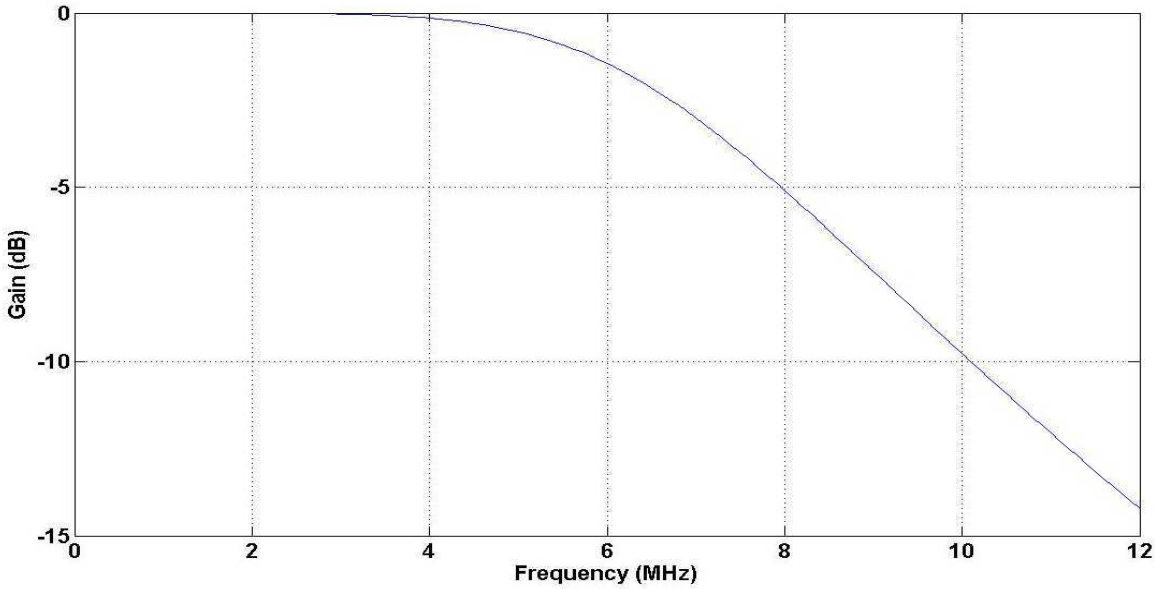


	EAV				Blank									SAV				Active Region													
NTSC	0	1	2	3	4	5	6	7	8	9	...	266	267	268	269	270	271	272	273	274	275	276	277	278	279	...	1711	1712	1713	1714	1715
PAL	0	1	2	3	4	5	6	7	8	9	...	278	279	280	281	282	283	284	285	286	287	288	289	290	291	...	1723	1724	1725	1726	1727
ITU656 Data Format	FF	00	00	XX	80	10	80	10	80	10	...	80	10	FF	00	00	YY	Cb 0	Y 0	Cr 0	Y 1	Cb 2	Y 2	Cr 2	Y 3	...	Y 717	Cb 718	Y 718	Cr 718	Y 719

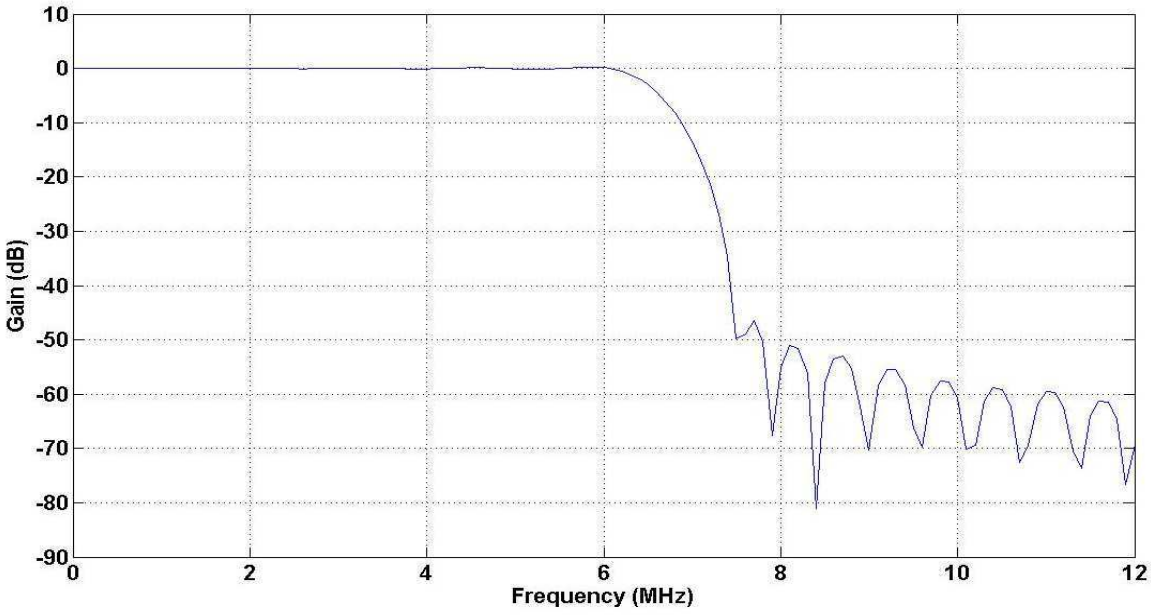
Fig: Horizontal Synchronization Signals

Filter response

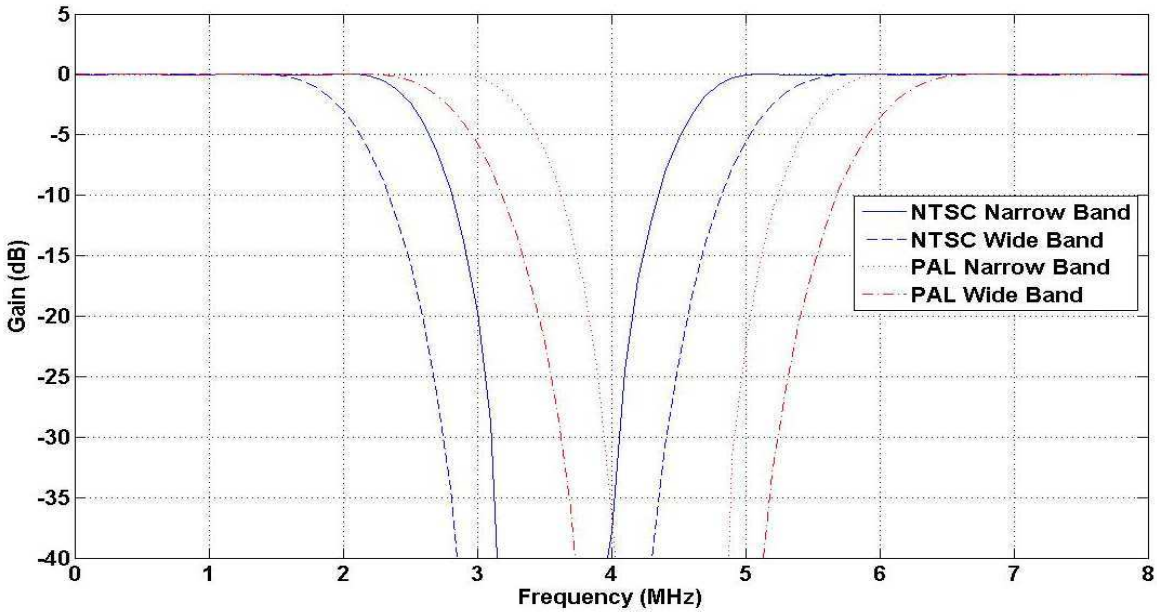
Anti-alias LPF



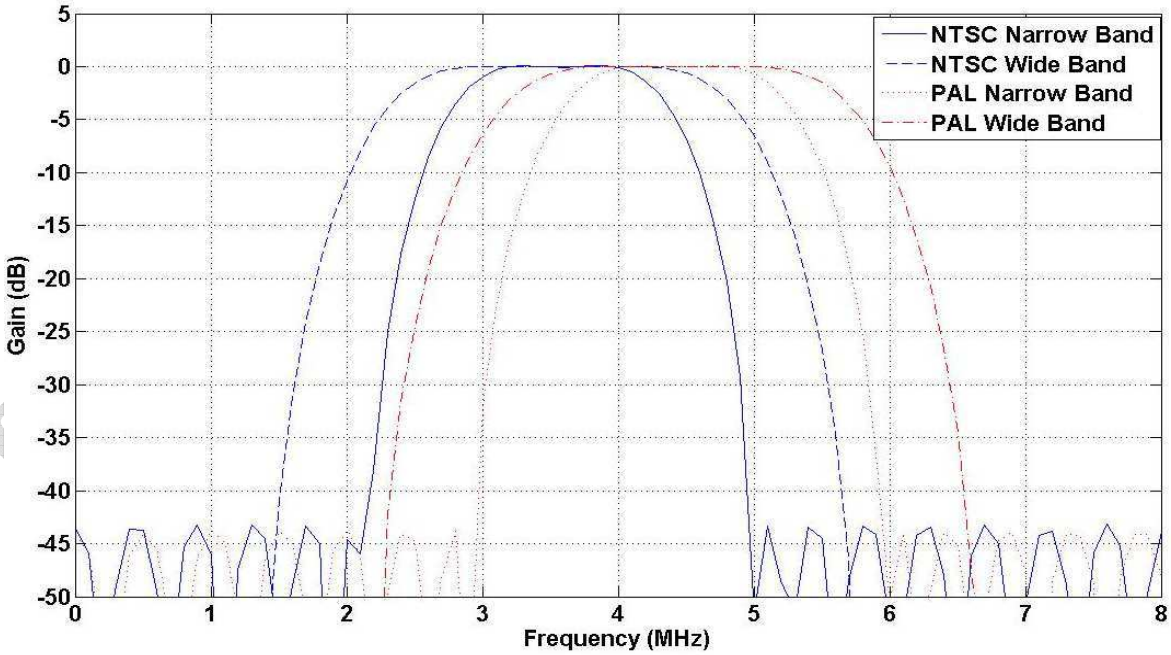
Decimation filter



Luma notch filter

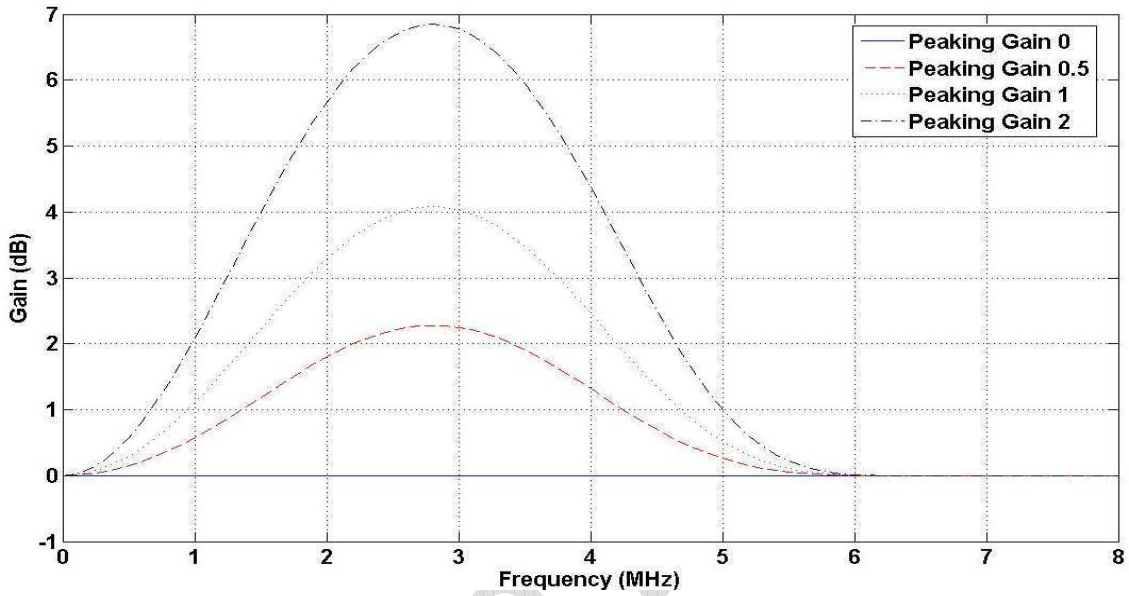


Chroma band pass filter

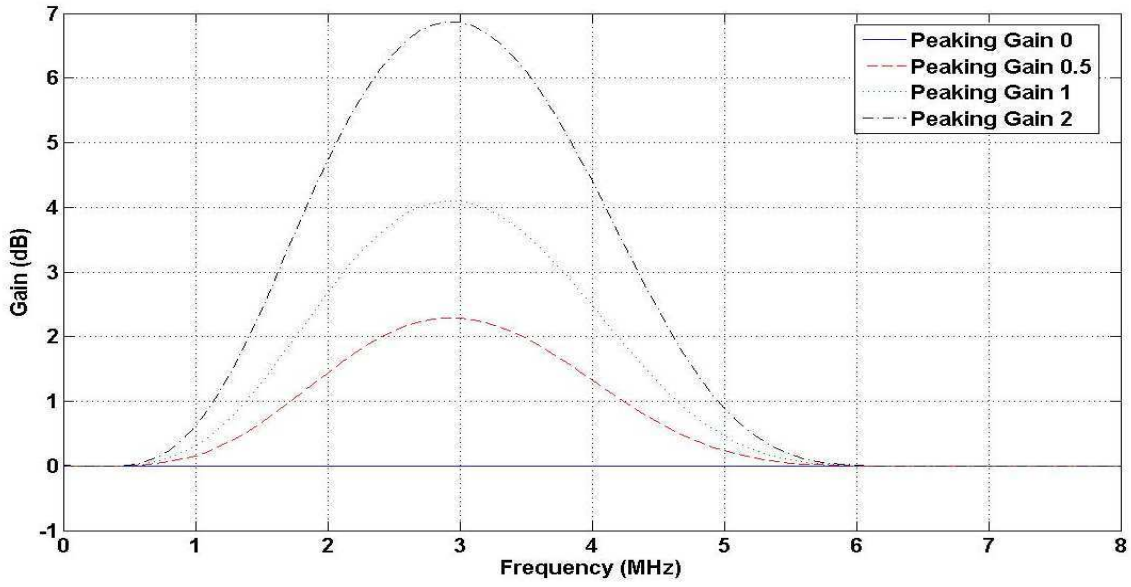


Y sharpness filter

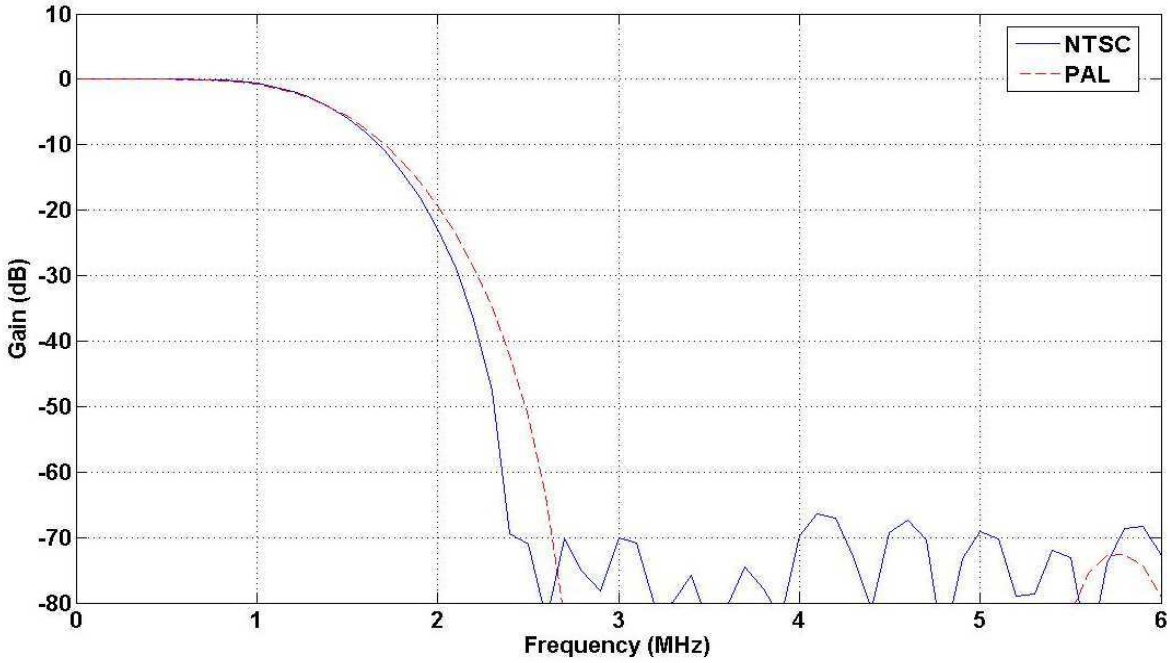
- NTSC



- PAL



UV demodulation low pass filter



PLL

The DM5900 has an internal PLL to generate the system and pixel clocks. A 27MHz is required for the PLL.

The default PLL setting is shown in the following table.

	Crystal In clock (MHz)	PLL out (MHz)	Function
PLL1	27	54	System/pixel clock

PLL default operated clock

The PLL parameters for various system configurations are shown in the following table.

	Crystal(MHz)	PLL out(MHz)	M	N	OD
PLL1	27	54	14	0	2

Formula:

CLK_OUT = XIN * (M+2)/[(N+2)*OD*2]

Where CLK_OUT: PLL output frequency

XIN: PLL input frequency.

M: The numerator of PLL formula.

[N, OD]: The denominator of PLL formula.

Attention:

1. 100MHz <= CLK_OUT * OD <= 250MHz
2. 1MHz <= XIN/(N+2)<=25MHz
3. OD >=1

Truth Table:

PD	BP	OE	CLK_OUT
0	0	0	CLK_OUT
0	0	0	XIN
Don't Care	1	0	XIN
Don't Care	Don't Care	1	0
Other			Undefined

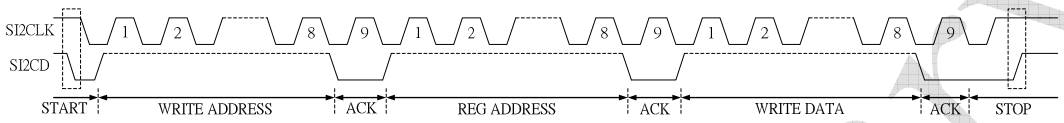
PD: Power down control; Active high.

BP: Bypass XIN to CLK_OUT; Active high.

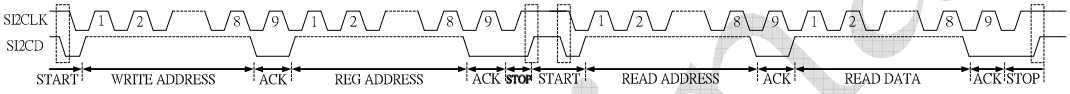
OE: CLK_OUT enable pin, Active low.

Host Interface

In the DM5900, I^2C is used for setting configuration and parameters, for example, brightness, contrast, saturation, hue, and sharpness control. The typical timing diagram of I^2C write and read access is illustrated in the following figure.



Write operation of I^2C bus



Read operation of I^2C bus

Write/Read Address							
Slave Address							R/W
1	0	1	1	1	0	SIAD	0: Write; 1: Read

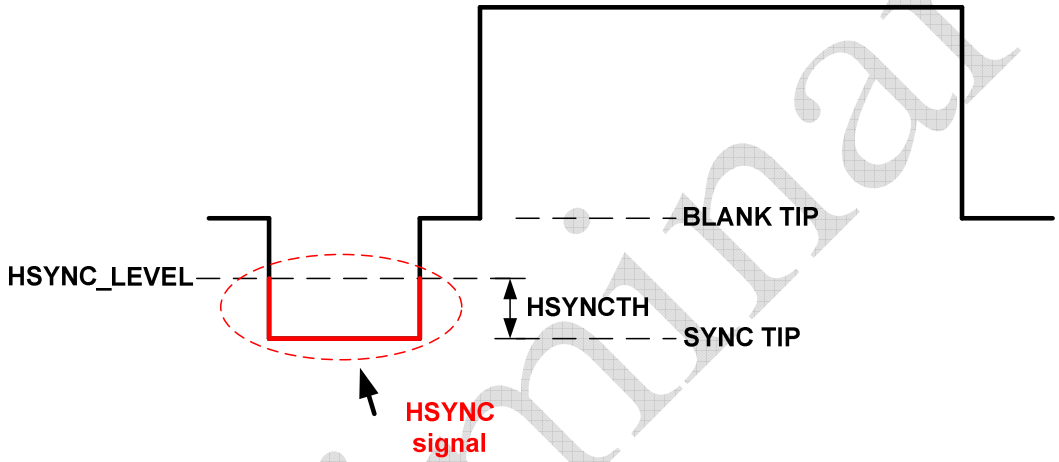
The external Pull-up/Pull-down resister connected to the pin “VD0/SIAD” indicates the device address SIAD. When pull-up resistor is connected to the pin, it indicates SIAD with a high value. Otherwise when pull-down resistor is connected to the pin, it indicates SIAD with a low value.

	Write Address	Read Address
SIAD = 0	B8	B9
SIAD = 1	BA	BB

Internal Control Registers

Video Decoder

HSYNC signal:



HSYNC_LEVEL=SYNC TIP + HSYNCTH

Address= 8'h00

VD Control							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**1**	**0**	**1**	**0**
BBRSTZ	**IFLDFASTSW**	**FASTSWEN**	**S_Video**	**ADC_A**	**ADI_ADC**	**EN**	**SRSTZ**

SRSTZ: SW reset video decoder, WO

EN: Enable Video decoding function

S_Video: When input signal is S-Video, set this bit to be 1

FASTSWEN: Enable fast switch function

IFLDFASTSW: Set 1: Fast switch boundary at every field end. Only Valid when REG04[3] : 1'b0.

Set 0: Fast switch boundary at frame end.

BBRSTZ: Base Band reset only, WO

Address= 8'h01

WATCHSEL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hf				0	0	2'b01	
AGC_LMT							

AGC_LMT: Analog AGC range

AGC

Address= 8'h02

AGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				1	0	1	1
AGC_gain					AGC_DTRACKEN	HWAGCEN	SYNCCAGCEN

SYNCCAGCEN: Set 1, enable CAGC gain update.

HWAGCEN: Hardware AGC enable

AGC_DTRACKEN: Dynamic sync tip tracking enable

AGC_gain: SW set AGC gain, RW

Address= 8'h03

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h63							
AGCDOWNTH[7:0]							

AGCDOWNTH: ADC couldn't larger than 867, if it is, will decrease the agc_gain.

Address= 8'h04

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h3	
FASTSWOPT				OFASTSW		AGCDOWNTH[9:8]	

OFASTSW: Set 1: FASTSW control from input PIN (MPOUT).

Set 0: FASTSW source from internal logic related to FASTSWOPT, RW

FASTSWOPT: Set fast switch frame length ((FASTSWOPT+1)x8), RW

Video Detection Misc

Address= 8'h05

HSYNCTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
HSYNCTH							

HSYNCTH: Set horizontal sync threshold level

Address= 8'h06

Vdet_misc							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	0	1	1
MONOUT	MUKSEL			BLACKOUT	SETUP_7.5IRE	OCCIREN	ColorPOUT

ColorPOUT: Set 1, VD will drive Color panel when no video signal detected, otherwise drive black panel. Color panel setting see 0x**2A**[6:4]

OCCIREN: Set 1, VD will out CCIR656

SETUP_7.5IRE: Set 1, add 7.5 IRE to the BLANK_TIP

BLACKOUT: Set 1, VD will drive black panel or blue panel when no video signal detected.

MONOUT: Force CCIR656 Cb=128, Cr=128

Color Killer

Address= 8'h08

ColorKill TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
CBDIFFTH[7:0]							

CBDIFFTH: Set the color burst difference threshold

2D Comb Filter

Address= 8'h09

Com2D_CFG							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
			FORCE_MONO			**NOTCHFLTSEL**	**DIS_VCOMB**

DIS_VCOMB: Set 1 to disable vertical comb filter

NOTCHFLTSEL: Set 0, use the wide band notchfilter

Set 1, use the narrow band notchfilter

FORCE_MONO: Set 1 to force the MONO signal mode.

Address= 8'h0C

PAL SW CFG							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
2'h0			**0**				**0**
Y_SHARP_GAIN			**PALSWINV**				**PALSWOPT**

PALSWOPT: Set 1 to use standard pal switch define to demodulation.

For line lock camera, set this bit to 1.

PALSWINV: Only valid when PALSWOPT=1. Set 1, PAL switch will be inversed.

Y_SHARP_GAIN: 2'h0: no sharpness function

2'h1: sharpness gain 0.5

2'h2: sharpness gain 1

2'h3: sharpness gain 2

Address= 8'h10

VD Decoder status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
PAL_Nc	PAL-I,B,B1,G,H,D/PAL_N	PAL_M	PAL_60	NTSC-443	NTSC-J/NTSC-M	COLOR KILL_525	COLOR KILL_625

The register show the video decoded status

RO. Set 1 to enable SW force mode.

Address= 8'h11

VD_STS							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
CLKLOCK_STST							DET_NONILT

DET_NONILT: RO. Detect the non-interlaced signal format.

CLKLOCK_STST: RO. Clock offset lock status

Address= 8'h12

DAGC_LMT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h3				4'hf			
CLKOFF_LOCK				DAGC_LMT			

DAGC_LMT: Digital AGC range

CLKOFF_LOCK: Clock offset locking function. 4'h0: always tracking

Others: clock offset lock within CLKOFF_LOCK * 8 ppm.

Address= 8'h13

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	1	1	0	1	0	1	1
SWFAR54MD	HWFAR54OPT	GAINLOCK_OPT	CLKOFFDIS	CBADJ	BLANK_SHIFTEN	ALINELOCK	CLKOFF_TRACKEN

CLKOFF_TRACKEN: CLKOFFSET tracking enable

ALINELOCK: Active line lock option, fixed line start position.

BLANK_SHIFTEN: Set 1, blank level will be modified according to color burst mean value per line.

CBADJ: Color burst adjust

CLKOFFDIS: Disable clock offset tracking function

GAINLOCK_OPT: Enable gain locking function after 16 frame decoded.

HWFAR54OPT: Set 1, FAR4FS will operate in 54Mhz when detecting 4.43 subcarrier

SWFAR54MD: Software force FAR4FS operate in 54MHz.

Address= 8'h14

VD_CFG							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**1**	**0**	**1**	**1**	**1**
		LLCFASTMD			**VDETOPT**	**LTRACKOPT**	**CLKLOCKOPT**

CLKLOCKOPT: Set 0 : Always tracking clock offset when

abs(clkoffset)> CLKOFF_LOCK (REG12[7:4])

Set 1 : keep tracking until first time

abs(clkoffset)< CLKOFF_LOCK(REG12[7:4])

LTRACKOPT: Set 1: Hardware continues active line (video) decoding when miss valid HSYNC signal until video loss.

Set 0: Hardware performs active line (video) decoding until valid HSYNC signal detected.

VDETOPT: Set 1: using rising edge of HSYNC signal as line detection timing.

Set0: using falling edge of HSYNC signal as line detection timing.

For long cable application, set this bit to 1.

LLCFASTMD[1:0]:

Line lock Auto Detection stable period. Valid when REG3B[5]=1.

Set 0: check line lock mode right after decode started

Set 1: check line lock mode after 8 frames decoded.

Set 2, 3: check line lock mode after 16 frames decoded.

Address= 8'h15

CLKOFF_CTL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	1	0	0
					CLKFRACEN	FIXHSYNC_MDL	SWFIXCLOCKOFF

SWFIXCLOCKOFF: Set 1, SW fixed clock offset. Force clock offset value= {REG25[4:0],REG24[7:0],REG23[7:0]}.

FIXHSYNC_MDL: Set 1, fixed the HSYNC_LEVEL to be REG05 HSYNCTH.

CLKFRACEN: Set 1, enable fraction clock offset tracking.

Address= 8'h17

HSYNC TRACK							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	6'd10					
HMIDTRACK	SWBLANKTIP						

HMIDTRACK: Set 1: tracking BLANK TIP each line at Front Porch Blanking position (REG4B[7:0]).

Set 0: tracking BLANK TIP at CVBS serration period.

SWBLANK1TIP: Only valid when REG17[8] = 1. Set 1: the estimation position of blanking level is REG4B[7:0].

Address= 8'h18

LOWTRACK							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	1	0	0	0	1	0
FSHYBCOPT	DISCOLKILL		NONINTEN	CAGCOPT	TRHSYNCOPT	LOWTRACK	TRHSYNCTH

TRHSYNCTH: Set 1: enable HW auto update HSYNCTH during video detection.

Set 0: use fix HSYNCTH (REG05[7:0]) during video detection.

LOWTRACK: Set 1: tracking SYNC TIP per line(s) from LOWLEVEL TRACKER.

Set 0: tracking SYNC TIP at CVBS serration period.

TRHSYNCOPT: Set 1: use fix HSYNCTH (REG05) during video detection

Set 0: enable HW auto update HSYNCTH during video detection.

CAGCOPT: Set 1 to enable color AGC.

NONINTEN: Set 1 to enable auto detect non-interlaced singal.

DISCOLKILL: Set 1 to disable auto detect color kill mode

FSHYBCOPT: ONLY valid under FASTSWEN.

Set 1: Keep previous tracked HSYNCTH

Set 0: use REG05 as HSYNCTH

Address= 8'h1A

BURST DETECT OPTION							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
FCOLRDETEN			COLR2CYC		BRST_DLY		

BRST_DLY: The number of color burst cycle delay.

COLR2CYC: Set 1, using two color burst cycle average to demodulation.

Set 0, using four color burst cycle average to demodulation.

FCOLRDETEN:

Set 1, fixed the color burst detect position.

Set 0, using auto detect color burst.

Address= 8'h1B

Reserved							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
				Reserved			

Reserved: RO.

Address= 8'h20

AGC gain							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
DAGC Gain				**AAGC Gain**			

AAGC Gain: Analog AGC gain setting, RO

DAGC Gain: Digital AGC gain setting, RO

Address= 8'h21

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SYNC_TIP[7:0]							

SYNC_TIP: RO

Address= 8'h22

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
BLANK_TIP[7:0]							

BLANK_TIP: RO

Address= 8'h23

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
CLKOFF[7:0]							

CLKOFF: RO, internal 2's compliment clock offset tracking status. Unit (ppm)

Address= 8'h24

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
CLKOFF[15:8]							

CLKOFF: RO, internal 2's compliment clock offset tracking status. Unit (ppm)

Address= 8'h25

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
			SYNC_TIP[20:16]				

SYNC_TIP: RO

Address= 8'h26

7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
				BLANK_TIP[9:8]		**SYNC_TIP[9:8]**	

BLANK_TIP: RO

SYNC_TIP: RO

Address= 8'h29

Blue Panel Select							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						PALBLPANL	NTSCBLPANL

PALBLPANL: Valid when REG06[3]=1. When no signal is presented, SW sets PAL blue panel out.

NTSCBLPANL: Valid when REG06[3]=1. When no signal is presented, SW sets NTSC blue panel out.

When PALBPANL=0, NTSCBLPANL=0. HW takes PAL as default mode.

Address= 8'h2A

VD_MISC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h0		2'h2	
	ColorOut			MPOUTMD		MPP_OPT	

MPP_OPT: 2'h0: drive field info to pin.

2'h1: drive Active info to pin.

2'h2: drive NOVID info to pin.

2'h3: drive FASTSW_SEL info to pin.

MPOUTMD: 2'h0: drive the XTI clock to MPOUT pin.

2'h1: drive the MPP to MPOUT pin.

2'h2 or 2'h3: drive FID_601 to MPOUT pin.

ColorOut: valid when REG06[3]=1 and REG06[0]=1.

3'h0: blue panel

3'h1: red panel

3'h2: white panel

3'h3: green panel

3'h4: magenta panel

3'h7: color rotation mode, blue → red →

white → green → magenta → black → blue…

Color Process

Address= 8'h2B

COLOR_EXT							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**1**	**2'h0**		**0**	**0**	**0**	**1**
	CCIRBLANKOPT					**NTSC_CCIREXT**	**EXT_COLOR**

EXT_COLOR: Set 1, Y/Cb/Cr value from 8'h1~8'hfe

NTSC_CCIREXT: Set 1 in NTSC mode, CCIR656 output 487 active line.

CCIRBLANKOPT: Set 1: output blanking period close to standard CCIR656.

Set 0: with short V blank lines before active field start.

Address= 8'h2C

Hue							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
Hue[7:0]							

Hue: Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

Address= 8'h2D

Saturation							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h10							
Saturation							

Saturation: unsigned, Range: 0 ~ 15.9375

8'hff: maximum, about x16 color intensity.

8'h00: (no color)

Address= 8'h2E

Contrast							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
8'h80							
Contrast							

Contrast: unsigned, Range : 0~2

8'hff: maximum (x2) contrast

8'h80: original signal (x1)

8'h00: minimum contrast

Address= 8'h2F

Brightness							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
8'h00							
Brightness							

Brightness: singed

8'h7f: brightest

8'h80: darkest

Address= 8'h30

INT Mask							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1_MASK	VLOST_1_MASK	VDET_1_MASK		MDCHG_0_MASK	VLOST_0_MASK	VDET_0_MASK

VDET_0_MASK: Set 1, enable register 0x31 VDET_0 interrupt function, RW

VLOST_0_MASK: Set 1, enable register 0x31 VLOST_0 interrupt function, RW

MDCHG_0_MASK: Set 1 enable register 0x31 MDCHG_0 interrupt function, RW

VDET_1_MASK: Set 1 to enable register 0x31 VDET_1 interrupt function, RW

VLOST_1_MASK: Set 1 enable register 0x31 VLOST_1 interrupt function, RW

MDCHG_1_MASK:Set 1 enable register 0x31 MDCHG_1 interrupt function, RW

Address= 8'h31

INT status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1	VLOST_1	VDET_1		MDCHG_0	VLOST_0	VDET_0

VDET_0: when detect video signal, the interrupt set, set by HW, set 1 to clear

VLOST_0: when lose video signal, the interrupt set, set by HW, set 1 to clear

MDCHG_0: when detect video signal change, the interrupt set, set by HW, set 1 to clear

VDET_1: valid for fast switch mode channel B, when detect video signal, the interrupt set, set by HW, set 1 to clear

VLOST_1: valid for fast switch mode channel B, when lose video signal, the interrupt set, set by HW, set 1 to clear

MDCHG_1: valid for fast switch mode channel B, when detect video signal change format, the interrupt set, set by HW, set 1 to clear

Address= 8'h33

HUE							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
						Hue[9:8]	

Hue: Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

Address= 8'h34

FIELD OPTION							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
					FIELD_INV	**FIELD_ONLY**	

FIELD_ONLY:CCIR656 signal output field 0 only

FILED_INV: Inverse output CCIR656 signal field

Address= 8'h35

Chroma Average							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
INVEN						CAVNTSCMD	CAVPALMD

INVEN: Mirror function enable. Set 1, enable mirror function.

See Pag.12

CAVNTSCMD: Set 1, enable NTSC mode Cb/Cr line average.

Set 0, disable.

CAVPALMD: Set 1, enable PAL mode Cb/Cr line average.

Set 0, disable.

Address= 8'h36

MASK CCIR656 LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
						MASKALL	PAL_MSK3

PAL_MSK3: Set 1, it will mask field 0 and 1 last lines according to REG37

MASKALL: mask all active

Address= 8'h37

MASK LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	MSK_LINE_F1				MSK_LINE_F0		

MSK_LINE_F0: When REG36[0] = 1, Mask Field 0 last number of active lines (0-7)

MSK_LINE_F1: When REG36[0] = 1, Mask Field 1 last number of active lines (0-7)

Address= 8'h38

MONO TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	5'h1f				
MONO_EN			MONO_TH				

MONO_TH: MONO mode AGC threshold. AGC max value 30. when set MONO_TH 31. AGC will always less than MONO_TH.

MONO_EN: Set 0, when no valid color burst detected.

Output CCIR656 Y through Notch filter.

Set 1, when no valid color burst detected. Output CCIR656 Y through Notch filer if AGC_GAIN>=MONO_TH, otherwise output CCIR656 Y with ADC data.

When No valid color burst detected (color kill mode). Output CCIR656 Cb/Cr with 128 (no color).

Address= 8'h39

COLOR BURST DETECT							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
1	**3'h4**			**4'h5**			
CAGCTRACKEN	**COLBSTCYC**			**COLBSTHSEL**			

COLBSTHSEL: Color Burst detection threshold.

4'h0 :COLBSTH = 0.125*(BLANK TIP – SYNC TIP)

4'h1 :COLBSTH = 0.25*(BLANK TIP – SYNC TIP)

4'h2 :COLBSTH = 0.375*(BLANK TIP – SYNC TIP)

4'h3 :COLBSTH = 0.5*(BLANK TIP – SYNC TIP)

4'h4:COLBSTH = 0.09375*(BLANK TIP – SYNC TIP)

4'h5 :COLBSTH = 0.078125*(BLANK TIP – SYNC TIP)

4'h6 :COLBSTH = 0.0625*(BLANK TIP – SYNC TIP)

4'h7 :COLBSTH = 0.03125*(BLANK TIP – SYNC TIP)

4'h8 :COLBSTH = 0

When color burst peak to peak value larger than

COLBSTHSEL, it's been considered a good color burst signal cycle

COLBSTCYC: When COLBSTCYC numbers of valid color bust cycle detected, VD will decode video with color and Color AGC will optionally started. Otherwise will enter color kill mode

CAGCTRACKEN: CAGC Track enable. Set 0 to disable CAGC track

Address= 8'h3A

CAGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	0	0
CAGCEN	CAGCLOCKOP	cagc_gain					

cagc_gain: RO. Chroma gain value. [5:2] integer, [1:0] fractional. (max 15.75, min 1)

CAGCLOCKOPT: Set 1, enable color AGC tracking until CAGC gain stable.

Set 0, color AGC tracking for first 15 video decoded frames.

CAGCEN : Set 1, enable color AGC.

Address= 8'h3B

Line Lock Camera							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	0	0
CAMLOCKOPT	LOCKCAM_DET	HLOCKDET1	ACTSHIFT				

ACTSHIFT: Active region shift, 2's compliment (-16~15)

HLOCKDET1: Set 1, to enable auto-detect Line Lock camera.

LOCKCAM_DET: RO, Line lock camera detected. (RO)

CAMLOCKOPT: Set 1, when line lock camera used.

Address= 8'h3C

LLOCKTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h20							
LLOCKTH							

LLOCKTH: Line Lock auto detection threshold, valid only when 0x3B[5]=1.

When REG13[1]=1, line boundary difference within a field larger than LLOCKTH, Line Lock Camera detected.

Note: when clock offset tracking unstable and REG13[1]=1, line boundary difference might be large within a field.

Address= 8'h3D

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	1	0	0	0	0	0	0
	ORSTOPT	OBFOVF	OBFUDF	LLFAR4FSOPT1			LLFAR4FSOPT

LLFAR4FSOPT: Set 1, decode video chroma without clock offset compensation.

Set 0, decode video choma after clock offset compensation.

Set this bit to one for Line Lock Camera.

LLFAR4FSOPT1: Set 1, Auto adjust the active region related to clock offset.

When force line lock mode, set this bit to 1;

OBFUDF: RO. CCIR output buffer under flow.

OBFOVF: RO. CCIR output buffer over flow.

ORSTOPT: Set 1, Reset CCIR output buffer when output buffer overflow or underflow.

Address= 8'h3D

DROP FRAME							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
FRDROP							FRDROPEN

FRDROPEN: Frame drop enable. Set 1 to enable drop frame function.

FRDROP: Drop frame number:

Output Frame Rate = (1-1/FRDROP)*Frame_Rate when FRDROP>0.

NTSC mode Frame_Rate = 30 frame/sec

PAL mode Frame_Rate = 25 frame/sec

Ex. FREROPEN=1, FRDROP=2, NTSC mode;

Output Frame Rate = (1-1/2)*30 frame/sec = 15 frame/sec

Address= 8'h3F

OUT BUFFER							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h1a							
OBFTH							

OBFTH: CCIR656 output buffer ready threshold.

Once CCIR656 output buffer count is larger than

OBFTH, starts output CCIR656 active region.

PS. CCIR656 output buffer max length is 48, set OBFTH around middle level of buffer length.

Address= 8'h40

CCIROUT TYP EN							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
PIX420EN	**PIX411EN**		**CROPEN**		**FLDCHIDEN**	**EAVCHIDEN**	**SWCHIDEN**

SWCHIDEN: Valid when REG00[5]=1(FASTSWEN). Add SW channel ID in first 4 data of active line, valid at fast switch mode. (field/frame)

EAVCHIDEN: Valid when REG00[5]=1(FASTSWEN) Add channel ID in EAV[3:0] and SAV[3:0], valid at fasts witch mode. (field/frame)

FLDCHIDEN: Valid when REG00[6:5]=2'h3 (**IFLDFASTSW**, FASTSWEN), output CVBS source A to field 0, output CVBS source B to field 1.

CROPEN: Video cropping function enable.

PIX411EN: PIXOUT 411 mode enable. Set 1, the PIXOUT set to be YCbCr 4:1:1

The output format as below:

CbYCrYYYCbYCrYYY…

PIX420EN: PIXOUT 420 mode enable. Set 1, the PIXOUT set to be YCbCr 4:2:0

The output format as below:

Odd line: CbYYCbYY…

Even line: YCrYYCrY…

Address= 8'h41

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		2'h3		2'h0		2'h0	
H_STR[9:8]		H_ACT[9:8]					

H_STR[9:8]: It defined the number of pixels start after SAV.

H_ACT[9:8]: It defined the number of active region.

H_STR + H_ACT < total number of pixels per line.

Address= 8'h42

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
H_STR[7:0]							

Address= 8'h43

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hC0							
H_ACT[7:0]							

Address= 8'h46

Cb/Cr Slicer							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
1					**3'h2**		
SLICER_EN					**SLICER_RANGE**		

SLICER_EN: CB/CR coring function enable.

SLICER_RANGE: Coring range (0 ~7). When 128 – **SLICER_RANGE** < (CB/CR) < 128+**SLICER_RANGE**, force the Chroma value to 128.

Address= 8'h4A

BT.601 Configuration							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
HSYNC_INV	**VSYNC_INV**	**FID_INV**		**HSYNC_EAV_STR**	**VSYNC_ODD_STR**	**HSYNCWIDTH**	

HSYNC_INV: Inverses output of BT.601 HSYNC signal.

VSYNC_INV: Inverses output of BT.601 VSYNC signal.

FID_INV: Inverses output of FID signal. (output pin is MPOUT, see REG2A[3:2])

HSYNC_EAV_STR:

BT. 601 HSYNC option, please refer capture of *Synchronization Signals*.

VSYNC_ODD_STR:

BT. 601 VSYCN option, please refer capture of *Synchronization Signals*.

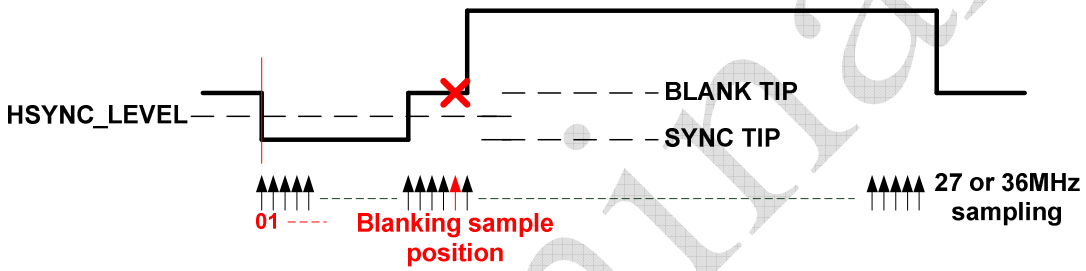
HSYNCWIDTH:

Software programmed the value of HSYNC valid length, this register only works when HSYNC_EAV_STR set 0.

Address= 8'h4B

BLANK1TIP							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h93							
BLANK1TIP							

BLANK1TIP: valid when REG17[7]. Line Blanking sample position.



Address= 8'h4C

HSYNCLOWCYC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	7'd20						
	HSYNCLOWCYC						

HSYNCLOWCYC: When low level (signal smaller than HSYNC LEVEL) signal exists over HSYNCLOWCYC, it's considered as a HSYNC signal Candidate.

Address= 8'h4D

LMARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h50							
LMARG27							

LMARG27: Sync signal detect margin after video detect.

Address= 8'h4E

MARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h50							
MARG27							

MARG27: Sync signal detect margin before video detect.

Address= 8'h50

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
HSYNC_INV	VSYNC_INV	INTREQ_INV	MPOUT_INV	HSYNC_CSR_OE	VSYNC_CSR_OE	INTREQ_CSR_OE	MPOUT_CSR_OE

MPOUT_CSR_OE: MPOUT output enable.

INTREQ_CSR_OE: INTREQ output enable

VSYNC_CSR_OE: VSYNC output enable

HSYNC_CSR_OE: HSYNC output enable

MPOUT_INV: MPOUT output inverse

INTREQ_INV: INTREQ output inverse

VSYNC_INV: VSYNC output inverse

HSYNC_INV: HSYNC output inverse

Address= 8'h51

RSTZ							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SHRSTZ							**TRSTZ**

TRSTZ: system reset

SHRSTZ: SW hardware reset

Address= 8'h52

VD POWER DOWN							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
IODIS		**HWPDNPOR**	**HWPDEN**			**PLLPWRDNOPT**	**SW_VDPWRDN**

SW_VDPWRDN: SW Power down video decoder. (When 1, power down)

PLLPWRDNOPT: PLL Power down option.

HWPDEN: HW Power down video decoder.

HWPDNPOR: Only valid when HWPDEN=1. When 1, PIN PDN=1 is power down. When 0, PIN PDN=0 is power down

IODIS: when 1 in normal function, all pin set to be input pin

Address= 8'h54

VADC CONFIG							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
4'ha				**0**	**0**	**1**	**0**
Bias				**B_SvideoC**	**SWGAIN_EN**	**pd_B**	**pd_A**

pd_A: power down VADC channel A

pd_B: power down VADC channel B

B_SvideoC: when channel B input signal is S-video C, B_SvideoC set 1

SWGAIN_EN: software gain enable.

Bias: video ADC bias config

Address= 8'h55

VADC CONFIG							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SW_GAINA1				**SW_GAINA0**			

SW_GAINA0: Set SWGAIN_EN=1, software set VADC channel A0 gain.

SW_GAINA1: Set SWGAIN_EN=1, software set VADC channel A1 gain.

Address= 8'h56

VADC CONFIG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				SW_GAINB			

SW_GAINB: Set SWGAIN_EN=1, software set VADC channel B gain.

Address= 8'h57

VADC CONFIG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
ClmpA1				ClmpA0			

ClmpA0: VADC A0 channel clamp.

ClmpA1: VADC A1 channel clamp.

Address= 8'h58

VADC CONFIG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				ClmpB			

ClmpB: VADC B channel clamp.

Address= 8'h59

VADC CONFIG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			sel_A			LPF_BYP	lpf_sel

sel_A: select CHA0 or CHA1 (Default A0)

LPF_BYP: Bypass Video ADC LPF when 1.

lpf_sel: The bandwidth of the low pass filter is 10MHz when 1, 6.5MHz when 0

Address= 8'h5A

TEST MODE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h0	
		SW_PLLBYPASSEN	SW_VADCBYPASSEN	SW_PLL_MBISTTST	SW_VADCTST	VADCTST_SEL	

SW_PLL_MBISTTST: Set 1, drive PLL&MBIST detail signal to chip IO pins.

SW_PLLBAPSSEN: Set 1, bypass internal pll out source.

VADCTST_SEL: valid for VADCTSTEN and VADCBYPEN.

in VADCTSTEN case:
2'b0: Dout = DoutA,
2'b1: Dout = DoutB
2'b2: Dout = when clk27 high DoutA, clk27 low DoutB

SW_VADCTST: Set 1, drive VADCSEL indicated ADC outputs to chip IO pins.

SW_VADCBYPASSEN: Set 1, bypass ADC data in from I/O pins.

Address= 8'h5B

MBIST CONTROL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
BISTGO					MBDONE	MBERR_1	MBERR_0

BISTGO: Set 1 to start MBIST logic. HW auto clear this bit after MBIST done.

MBDONE: Set by HW, set 1 to clear.

MBEER_0: when read back 1, sram broken, Set by HW, set 1 to clear.

MBEER_1: when read back 1, sram broken, Set by HW, set 1 to clear.

Address= 8'h5D

CONFIG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	DYMUX_VCLK			OPCLK_INV	DLYMUX_PCLK		

DLYMUX_PCLK: Selected PCLK delay time. (3'h0 is smallest, 3'h7 is longest)

OPCLK_INV: Set 1 to inverse PCLK output.

DLYMUX_VCLK: Selected pll_54 delay time to vadc.

(3'h0 is smallest, 3'h7 is longest)

Address= 8'h5F

REVISION_ID							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
8'h3B							
REVISION_ID							

REVISION_ID: RO, The DM5900 CHIP version ID.

PLL

Formula:

CLK_OUT = XIN * (M+2)/[(N+2)*OD*2]

Where CLK_OUT: PLL output frequency

XIN: PLL input frequency.

M: The numerator of PLL formula.

[N, OD]: The denominator of PLL formula.

Attention:

1. 100MHz <= CLK_OUT * OD <= 250MHz
2. 1MHz <= XIN/(N+2)<=25MHz
3. OD >=1

Truth Table:

PD	BP	OE	CLK_OUT
0	0	0	CLK_OUT
0	0	0	XIN
Don't Care	1	0	XIN
Don't Care	Don't Care	1	0
Other			Undefined

PD: Power down control; Active high.

BP: Bypass XIN to CLK_OUT; Active high.

OE: CLK_OUT enable pin, Active low.

Address= 8'h60

SW PLL Control							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SWPLL RST							**SWPLL1**

SWPLL1: set PLL1 input configuration from SWPLL1_XX set, otherwise hard wired with chip default vale.

SWPLLRST: set 1, chip will enter a reset mode waiting for PLL stable in 1ms. After that, SW needs to re-program all register setting except PLL configuration.

Address= 8'h61

SW PLL Config							
7-bit	**6-bit**	**5-bit**	**4-bit**	**3-bit**	**2-bit**	**1-bit**	**0-bit**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SWPLL1_OD					**SWPLL1 _OE**	**SWPLL1 _PD**	**SWPLL1 _BP**

SWPLL1_BP: PLL1_BP SW program source.

SWPLL1_PD: PLL1_PD SW program source.

SWPLL1_OE: PLL1_OE SW program source.

SWPLL1_OD: PLL1_OD SW program source

Address= 8'h62

SWPLL1 M							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
SWPLL1_M[7:0]							

SWPLL1_M: PLL1_M SW program source.

Address= 8'h63

SWPLL1_N							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	5'h0				
SWPLL1_M[8]			SWPLL1_N				

SWPLL1_N: PLL1_N SW program source

Address= 8'h6F

Fast Switch Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						OFSWOPT	OFSWSEL

OFSWOPT: When 1 and REG04[3]=1, Fast switch select signal is OFSWSEL (REG6F[0]). Otherwise, the fast switch select signal is PIN MPOUT(FID).

OFSWSEL: Fast switch selet signal. Only valid when OFSWOPT = 1.

Electrical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range

Supply voltage range: IOV_{DD} to DGND . . . . . .

DV_{DD} to DGND . . . . . .

PLL_AV_{DD} to PLL_AGND . . . . . .

$CH1\_AV_{DD}$ to CH1_AGND . . . . . .

Digital input voltage range, V_I to DGND . . . . . .

Input voltage range, XTAL1 to PLL_GND . . . . . .

Analog input voltage range A_I to CH1_AGND . . . . . .

Digital Output voltage range, V_O to DGND . . . . . .

Operating free-air temperature, TA . . . . . .

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
$IODV_{DD}$	Digital I/O supply voltage	2.97	3.3	3.63	V
DV_{DD}	Digital supply voltage	1.62	1.8	1.98	V
PLL_AV_{DD}	Analog PLL supply voltage	1.62	1.8	1.98	V
$CH1\_AV_{DD}$	Analog core supply voltage	1.7	1.8	1.9	V
$V_{I(P-P)}$	Analog input voltage (ac-coupling necessary)	0.25		1.0	V
V_{IH}	Digital input voltage high	2		5	V
V_{IL}	Digital input voltage low	-0.3		0.8	V
V_{IH_XTAL}	XTAL input voltage high	0.7 PLL_AV_{DD}			V
V_{IL_XTAL}	XTAL input voltage low			0.3 PLL_AV_{DD}	V
I_{OH}	High-level output current			2	mA
I_{OL}	Low-level output current			-2	mA
I_{OH_SCLK}	SCLK high-level output current			4	mA
I_{OL_SCLK}	SCLK low-level output current			-4	mA
T_A	Operating free-air temperature	-40		125	^oC

Crystal Specifications

CRYSTAL SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		27.0		MHz
Frequency tolerance		±100		ppm

Electrical Characteristics

DV_{DD} = 1.8 V, PLL_AV_{DD} = 1.8 V, $CH1\_AV_{DD}$ = 1.8 V, IOV_{DD} = 3.3 V

For minimum/maximum values: T_A = 0°C to 70°C, and for typical values: T_A = 25°C unless otherwise noted

DC Electrical Characteristics

PARAMETER	TEST CONDITIONS (see NOTE 1)	MIN	TYP	MAX	UNIT
$I_{DD(IO\_D)}$ Digital I/O supply current	Color bar input		4.8		mA
$I_{DD(D)}$ Digital core supply current	Color bar input		50.7		mA
$I_{DD(PLL\_A)}$ Analog PLL supply current	Color bar input		5.9		mA
$I_{DD(CH1-A)}$ Analog PLL supply current	Color bar input		26.1		mA
P_{TOT} Total power dissipation, normal mode	Color bar input		165	205	mW
P_{DOWN} Total power dissipation, power-down mode	Color bar input			5	mW

C_i	Input capacitance	By design	8	pF
V_{OH}	Output voltage high	I_{OH} = 2 mA	0.8 IOV_{DD}	V
V_{OL}	Output voltage low	I_{OL} = -2 mA	0.22 IOV_{DD}	V
V_{OH_SCLK}	SCLK output voltage high	I_{OH} = 4 mA	2.3	V
V_{OL_SCLK}	SCLK output voltage low	I_{OL} = -2 mA	0.6	V
I_{IH}	High-level input current	$V_I = V_{IH}$	±50	µA
I_{IL}	Low-level input current	$V_I = V_{IL}$	±50	µA

NOTE 1: Measured with a load of 15 pf.

Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_i	Input impedance, analog video inputs	By design	500			kΩ
C_i	Input capacitance, analog video inputs	By design		10		pF
$Vi_{(pp)}$	Input voltage range *	$C_{coupling}$ = 0.1 µF	0.25		1	V
ΔG	Gain control range			12		dB
DNL	DC differential non-linearity	A/D only		±2		LSB

INL	DC integral non-linearity	A/D only	±3	LSB
Fr	Frequency response	6 MHz	-0.9 -3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-p	50	dB
NS	Noise spectrum	50% flat field	50	dB
DP	Differential phase		1.5	°
DG	Differential gain		0.5%	

* The 0.75-V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistors are 37.4 Ω.

Timing

Clocks, Video Data, Sync timing

Data Format : CCIR656 output					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
PIXCLK High pulse duration	t_{hw}	18.5			ns
PIXCLK Low pulse duration	t_{lw}	18.5			ns
CCIR656 data out setup time	t_{su}	18.5			ns
CCIR656 data out hold time	t_h	18.5			ns

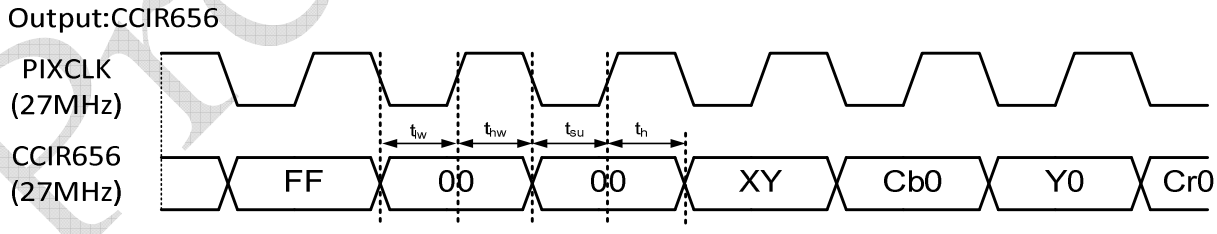
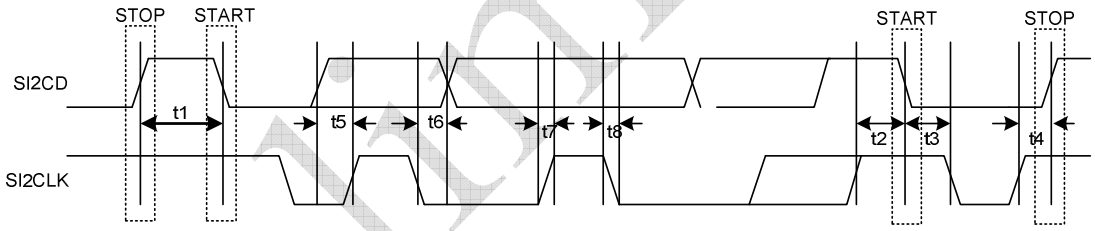


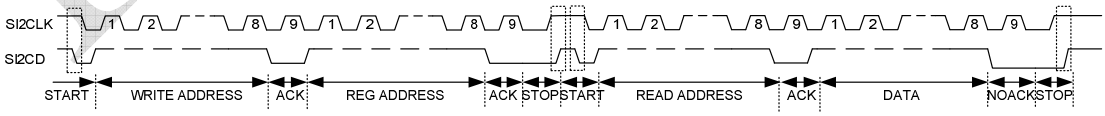
Figure 3-2 . Clocks, CCIR656 Output Data Timing

I²C Host Port Timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1 Bus free time between STOP and START		1.3			µs
t_2 Setup time for a (repeated) START condition		0.6			µs
t_3 Hold time (repeated) START condition		0.6			µs
t_4 Setup time for STOP condition		0.6			µs
t_5 Data setup time		200			ns
t_6 Data hold time		0		50	ns
t_7 Rise time I2CD and I2CLK signal		250			ns
t_8 Fall time I2CD and I2CLK signal			250		ns
C_b Capacitive load for each bus line				120	pF
f_{I2C} I^2C clock frequency				400	kHz

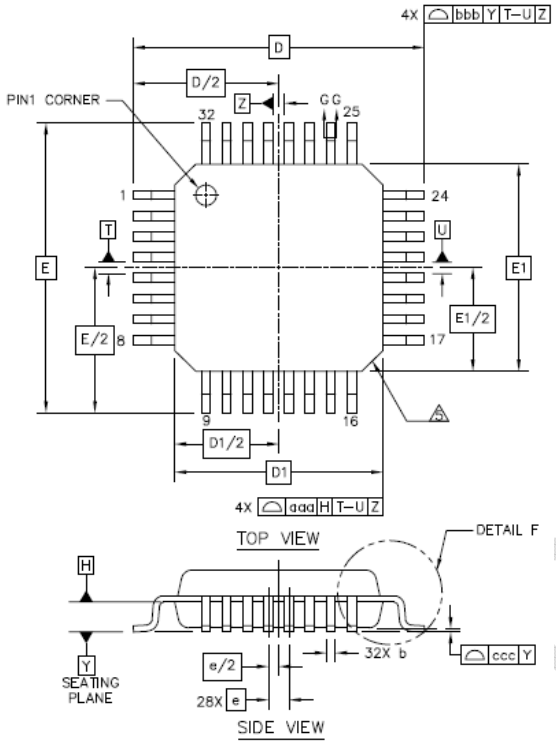


	Write Address	Read Address
SIAD = 0	B8	B9
SIAD = 1	BA	BB



Packaging

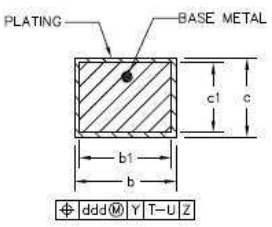
(1) 32 PIN LQFP



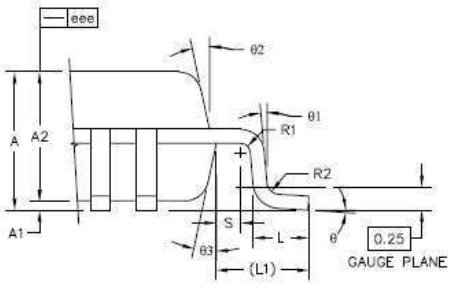
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	---	1.45
LEAD WIDTH(PLATING)		b	0.18	---	0.27
LEAD WIDTH		b1	0.17	---	0.23
L/F THICKNESS(PLATING)		c	0.1	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	7 BSC		
	Y	E	7 BSC		
	X	D1	5 BSC		
	Y	E1	5 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	---	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	---	7°
		θ1	0°	---	---
		θ2	11°	---	13°
		θ3	11°	---	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

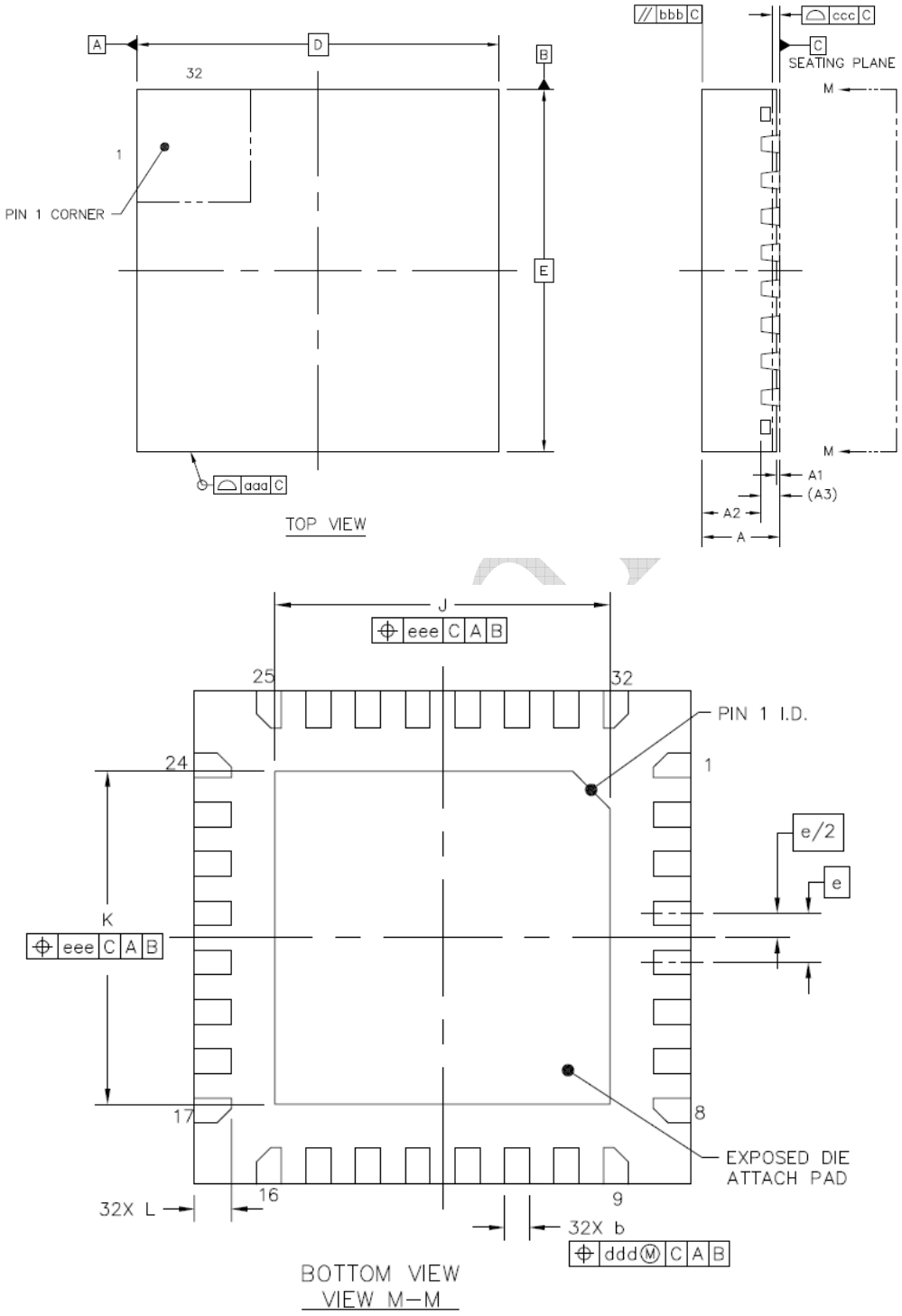


SECTION G–G
SCALE: 100/1



DETAIL F
SCALE: 20/1

(2) 32 PIN QFN


A
D
B
32
1
PIN 1 CORNER
E
aaa C
TOP VIEW
bbb C
ccc C
C
SEATING PLANE
M
M
A1
(A3)
A2
A
J
eee C A B
25
32
PIN 1 I.D.
24
1
e/2
e
K
eee C A B
17
8
EXPOSED DIE
ATTACH PAD
32X L
16
9
32X b
ddd M C A B
BOTTOM VIEW
VIEW M–M

32 PIN QFN

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.3	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Ordering Information

Part Number	Pin Count	Package
DM5900EP	32	LQFP (Pb-Free and Halogen-Free)

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.