

1. General Description

The DM9102D is a fully integrated and cost effective single chip Fast Ethernet NIC controller. It is designed with low power and high performance process. It is a 2.5/3.3V device with 5V tolerance.

The DM9102D provides direct interface to the PCI bus and supports bus master mode to achieve the high performance of the PCI bus. It fully complies with PCI 2.2. In the media side, the DM9102D interfaces to the UTP3, 4, 5 in 10Base-T and the UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. The auto-negotiation and

HP Auto-MDIX function can automatically configure the DM9102D to take the maximum advantage of its abilities. The DM9102D also supports IEEE 802.3x's full-duplex flow control to prevent the receive overflow of link partner. The IPv4 IP/TCP/UDP checksum generation and checking can reduce the system CPU utilization.

The DM9102D supports two types of power management mechanisms. The main mechanism is based on the OnNow architecture, which is required for PC99. The alternative mechanism is based upon the remote Wake-On-LAN mechanism.

2. Block Diagram

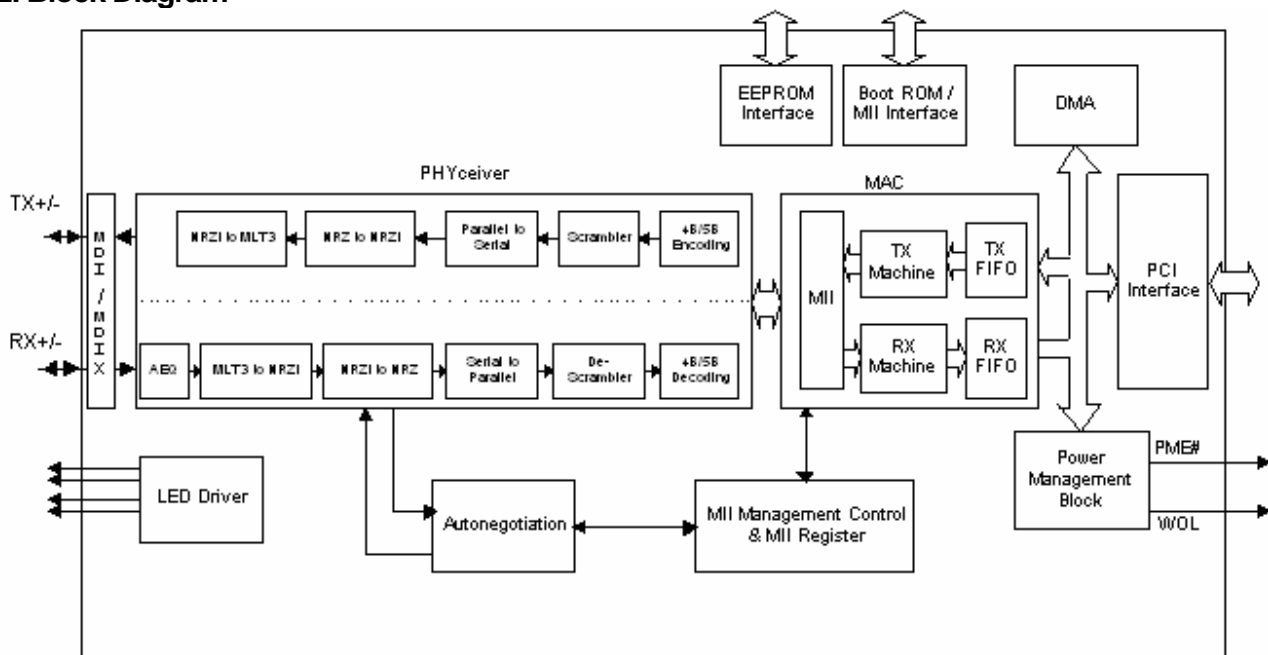




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