INNOVATIVE SEMICONDUCTORS, INC.

PRODUCT BRIEF

ISI-500

Inverse Discrete Cosine Transform (IDCT) Synthesizable IP

Overview

Chip manufacturers that are developing decoders for MPEG-2, MPEG-1, JPEG, H261, H263 and H264 video standards need three main building blocks: a variable length decoder, an IDCT and a frame reconstruction block. The ISI-500 is a high performance IDCT synthesizable block that meets the video standards requirements using commercially available process technology.

Architecture

• The ISI-500 architecture achieves high performance, flexibility and low gate count. The architecture implements a two dimensional IDCT.

• A pipeline executes the instructions in an overlapped manner. Three phases are used: Instruction Decode/Operand Fetch, Instruction Execute and Write Back.

• An innovative memory design is used to store intermediate results.

• The design uses one multiplier and several adders to achieve performance close to the theoretical maximum.

• Delays due to data dependencies are minimized reducing the number of pipeline stall cycles to a minimum.

• The configuration parameters for the block are data path width, four or eight adders and custom or register implementation of the two memory banks.

Interface

The SL500a interfaces with the inverse Quantization block on one side and the frame reconstruction block on the other side. Two banks of memories are used to pipeline the VLD, IDCT and FR stages. The interface is simple and similar to a memory read/write

Functional Blocks

•The Data path is the IDCT algorithmic engine. It consists of the memory to store the IDCT coefficients or the temporary results. It also has a 16x16-bit multiplier, a 16-bit shifter, four 16-bit adders and several pipeline registers.

•The Decode and sequencer Block. It is hardwired and is implemented as a state machine with a look up table.

•A permutation and scaling stage is implemented in the inverse quantizer block before storage in the IDCT memory

Key Features

- *The architecture implements a two dimensional IDCT*
- *The design uses one multiplier and several adders*
- *Configurable design (data path width, four or eight adders and custom or register implementation of the two memory banks)*
- *Two banks of memories are used to pipeline the VLD, IDCT and FR stages. The interface is simple and similar to a memory read/write*

Configuration	1	2
Number of cycles	237	173
Number of Adders	4	8
Number of multipliers	1	1
NOC Theoretical Maximum	175	117

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