INNOVATIVE SEMICONDUCTORS, INC.

PRODUCT BRIEF

ISI-300

Huffman Decoder Synthesizable IP

Overview

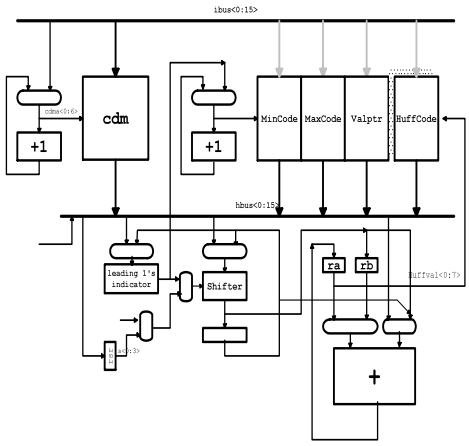
Chip manufacturers that are developing decoders for MPEG-2, MPEG-1, JPEG, H261, H263 and H264 video standards need three main building blocks: a variable length decoder, an IDCT and a frame reconstruction block. The ISI-300 is a Huffman Decoder Synthesizable block that meets the video standards requirements using commercially available process technology.

Architecture

• The ISI-300 architecture achieves high performance, flexibility and low gate count.

• The architecture balances gate count and speed to achieve optimum design. It is implemented using an adder, shifter, random logic and lookup table for the coefficients.

Block Diagram

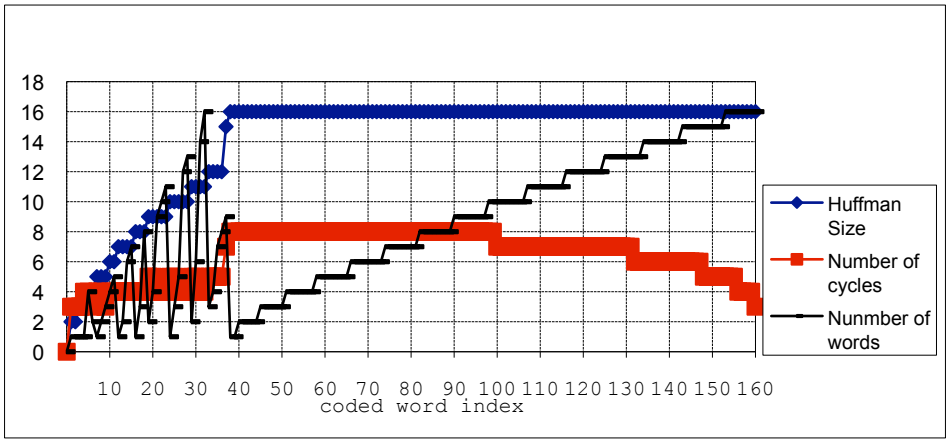


Interface

Two banks of memories are used to pipeline the VLD, IDCT and FR stages. The interface is simple and similar to a memory read/write

Key Features

- *The architecture implements a two dimensional IDCT*
- *The design uses one adder an incrementer, a shifter and memory*
- *Novel memory architecture*
- *Two banks of memories are used to pipeline the VLD, IDCT and FR stages. The interface is simple and similar to a memory read/write*
- *Low gate count*
- *High performance*



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