INNOVATIVE SEMICONDUCTORS, INC.

PRELIMINARY PRODUCT INFORMATION

ISI-210

Certified USB 2.0 High-Speed Transceiver OTG Core

Overview

The ISI-210 is a USB 2.0 OTG high-speed Physical Layer Hard Macro Transceiver. It allows System On a Chip (SOC) designers to quickly integrate the transceiver into their chip. It fully supports USB 2.0 UTMI + Specifications. It has been verified in silicon using different process technologies. It requires minimal number of external components. The core supports 8 bit parallel, 16 bit parallel and/or full/low speed serial data interfaces.

Deliverables

- GDSII Layout file
- Library Exchange Format (LEF) of the Macro-cell.
- Encrypted Verilog model
- Timing Model File (.LIB)
- SOC Integration/Test Document

Testability

- The Design Support all the UTMI test modes.
- Four additional test modes:
- No Test
- No Frequency Check
- Test at lower frequency
- Scan Mode
- Receive Snoop test
- Special Analog Test Modes
- Loop Back Test Supported

Innovative Edge

- The design has been ported several times to different process technologies. The quality of the design and the quality of the porting process improved every time the design was ported.
- First IP company with a USB 2.0 OTG PHY Prototype Silicon IP
- Impressive list of Licensees.
- Has been in production in millions of chips in TSMC 0.25u, .18u, 15u, and .13u process technologies among others.
- Established and trained a network of Design Services Partners to port the design quickly to new processes.

Functional Blocks

Analog Front End

- High Speed/Full Speed/Low Speed Transmitter/Receiver.
- The VBUS Comparators provide indications about the voltage level on VBUS.
- The Pull–up/pull–down Resistors
- Termination Resistors with auto calibration
- A US patent was issued for our novel implementation of the calibration resistor.
- Oscillator and PLL circuit
- Band-gap voltage reference and associated bias generation circuits.

Digital Back End

- Clock and Data Recovery (CDR). The all digital CDR maintains stable operation over a wide variation in Process, Voltage and Temperature
- SERDES: SERializer/DESerializer. It includes: the Bit Stuffer, the Bit unstuffer, the NRZ encoder and the NRZ Decoder.

USB Product Line

- ISI-75: USB full-speed Transceiver
- ISI-88: USB OTG full-speed Transceiver
- ISI-200: Device USB 2.0 high-speed Transceiver Macro-cell (UTMI)
- ISI-205: Host USB 2.0 high-speed Transceiver Macro-cell
- ISI-210: OTG USB 2.0 high-speed Transceiver Macro-cell (UTMI+)

Key Features

- *Digital CMOS Process Technology.*
- *Supports 480 Mbits/s, 12Mbits/s "full speed" and 1.5Mbits/s "low speed" operation.*
- *Can be configured as Device/Host/OTG*
- *Supports On The Go Standard (OTG)*
- *Low Power Consumption*
- *On chip oscillator, termination resistor and DP/DM Short Circuit protection.*
- *On chip OTG comparators*
- *5v tolerance Circuitry*
- *Design can be mapped into different process technologies.*
- *Supports Power down mode.*
- *Supports data line VBUS pulsing session request*

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