Flash

4 Mbit Serial Flash Memory with Dual and Quad

■ FEATURES

- Single supply voltage 1.65~2V
- Speed
  - Fast Read for SPI mode
    - Read max frequency: 33MHz
    - Fast Read max frequency: 104MHz
    - Fast Read Dual/Quad max frequency: 84MHz/104MHz (168MHz equivalent Dual SPI; 416MHz equivalent Quad SPI)
  - Fast Read for QPI mode
    - Fast Read max frequency: 84MHz
    - Fast Read Quad max frequency: 104MHz (416MHz equivalent Quad QPI)
- Low power consumption
  - Active current: 20 mA (max.)
  - Standby current: 30 μA (max.)
  - Deep Power Down current: 5 μA (max.)
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Page programming time: 0.7 ms (typical)
- Page Programming
  - 256 byte per programmable page
- Program/Erase Suspend
- Erase
  - Chip Erase time 3 sec (typical)
  - 64K bytes Block Erase time 0.5 s (typical)
  - 32K bytes Block Erase time 250 ms (typical)
  - 4K bytes Sector Erase time 60 ms (typical)
- Status and Security Register Feature
- Command Reset
- Advanced Security Features
  - Flexible Block Protection (BP0-BP3)
- Lockable 512 bytes OTP security sector
- SPI Serial Interface
  - SPI Compatible: Mode 0 and Mode 3
- End of program or erase detection
- Write Protect ($\overline{WP}$)
- Hold Pin ($\overline{HOLD}$)
- All Pb-free products are RoHS-Compliant

■ ORDERING INFORMATION

Product ID	Speed	Package		Comments
F25D04QA-104PIG	104MHz	8-lead SOIC	150 mil	Pb-free
F25D04QA-104VIG	104MHz	8-lead VSOP	150 mil	Pb-free
F25D04QA -104HIG	104MHz	8-contact WSON	6x5 mm	Pb-free

■ GENERAL DESCRIPTION

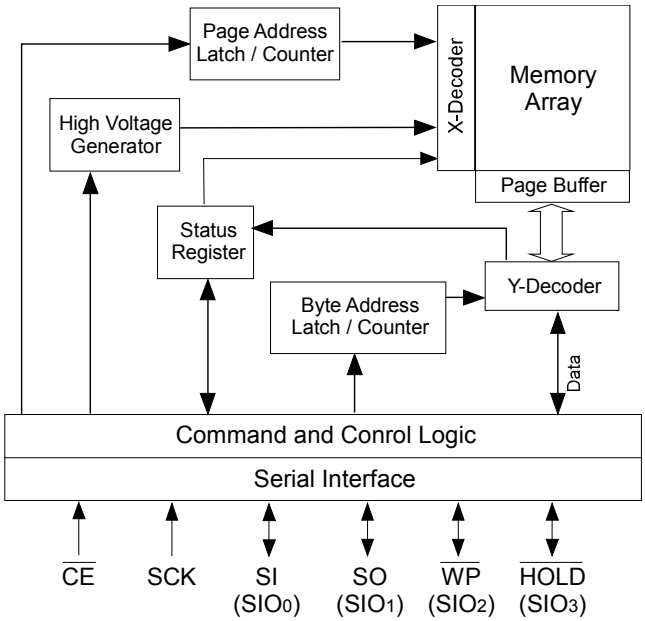
The F25D04QA is a 4 Megabit, 1.8V only CMOS Serial Flash memory device. The device supports the standard Serial Peripheral Interface (SPI), a Dual/Quad SPI and QPI. ESMT's memory devices reliably store memory data even after 100,000 programming and erase cycles.

The memory array can be organized into 2,048 programmable pages of 256 byte each. 1 to 256 byte can be programmed at a time with the Page Program instruction.

The device features sector erase architecture. The memory array is divided into 128 uniform sectors with 4K byte each; 16 uniform blocks with 32K byte each; 8 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device. The device has Sector, Block or Chip Erase but no page erase.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

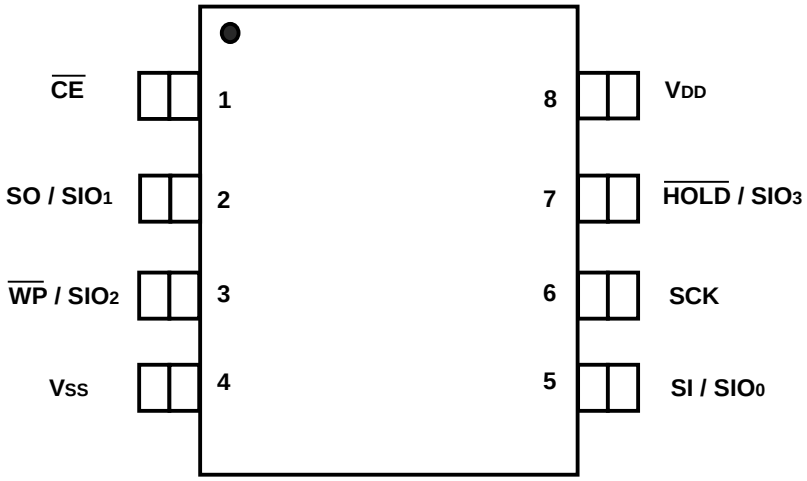
■ FUNCTIONAL BLOCK DIAGRAM



■ PIN CONFIGURATIONS

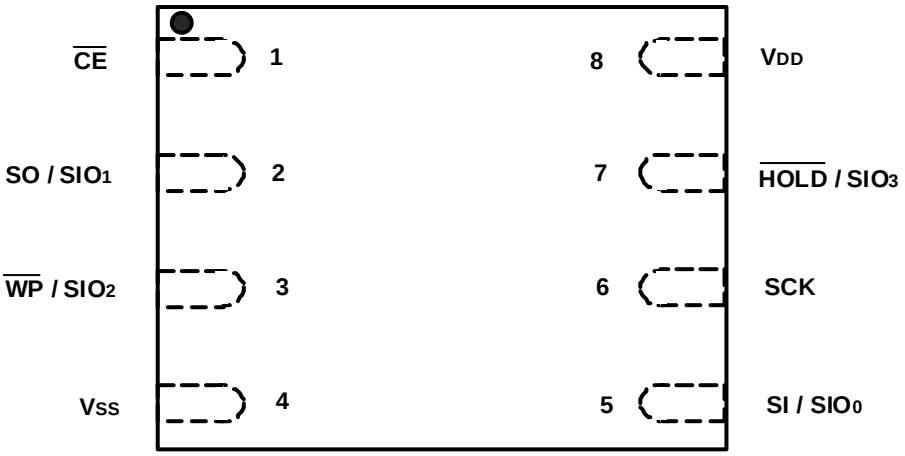
8-Lead SOIC / 8-Lead VSOP

(SOIC 8L, 150mil Body, 1.27mm Pin Pitch)
(SOIC 8L, 150mil Body with thickness 0.88mm, 1.27mm Pin Pitch)



8- Contact WSON

(WSON 8C, 6mmX5mm Body, 1.27mm Contact Pitch)



■ PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing for serial input and output operations
SI / SIO_0	Serial Data Input / Serial Data Input Output 0	To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK (for Standard read mode). / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK(for Dual/Quad mode).
SO / SIO_1	Serial Data Output / Serial Data Input Output 1	To transfer data serially out of the device. Data is shifted out on the falling edge of SCK (for Standard read mode). / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Dual/Quad mode).
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{WP}$ / SIO_2	Write Protect / Serial Data Input Output 2	The Write Protect ($\overline{WP}$) pin is used to enable/disable BPL bit in the Status Register. / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Quad mode).
$\overline{HOLD}$ / SIO_3	Hold / Serial Data Input Output 3	To temporality stop serial communication with SPI flash memory without resetting the device. / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Quad mode).
V_{DD}	Power Supply	To provide power.
V_{SS}	Ground	

■ SECTOR STRUCTURE

Table 1: Sector Address Table

64KB Block	32KB Block	Sector	Sector Size (Kbytes)	Address range	
7	15	127	4KB	07F000h – 07FFFFh	individual 16 sectors unit: 4KB
		:	:	:	
		120	4KB	078000h – 078FFFh	
	14	119	4KB	077000h – 077FFFh	
		:	:	:	
		112	4KB	070000h – 070FFFh	
6	13	111	4KB	06F000h – 06FFFFh	
		:	:	:	
		104	4KB	068000h – 068FFFh	
	12	103	4KB	067000h – 067FFFh	
		:	:	:	
		96	4KB	060000h – 060FFFh	
5	11	95	4KB	05F000h – 05FFFFh	
		:	:	:	
		88	4KB	058000h – 058FFFh	
	10	87	4KB	057000h – 057FFFh	
		:	:	:	
		80	4KB	050000h – 050FFFh	
2	5	47	4KB	02F000h – 02FFFFh	
		:	:	:	
		40	4KB	028000h – 028FFFh	
	4	39	4KB	027000h – 027FFFh	
		:	:	:	
		32	4KB	020000h – 020FFFh	
1	3	31	4KB	01F000h – 01FFFFh	
		:	:	:	
		24	4KB	018000h – 018FFFh	
	2	23	4KB	017000h – 017FFFh	
		:	:	:	
		16	4KB	010000h – 010FFFh	
0	1	15	4KB	00F000h – 00FFFFh	individual 16 sectors unit: 4KB
		:	:	:	
		8	4KB	008000h – 008FFFh	
	0	7	4KB	007000h – 007FFFh	
		:	:	:	
		0	4KB	000000h – 000FFFh	

individual block unit: 64KB

■ STATUS REGISTER

The Software Status Register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation, the Status Register may be read only to determine the completion of an operation in progress. Table 2 describes the function of each bit in the Software Status Register.

Table 2: Software Status Register

Bit	Name	Function	Default at Power-up	Read/Write
Status Register				
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 3)	0	R/W
3	BP1	Indicate current level of block write protection (See Table 3)	0	R/W
4	BP2	Indicate current level of block write protection (See Table 3)	0	R/W
5	BP3	Indicate current level of block write protection (See Table 3)	0	R/W
6	QE	1 = Quad enabled 0 = Quad disabled	0	R/W
7	BPL	1 = BP3, BP2,BP1,BP0 are read-only bits 0 = BP3, BP2,BP1,BP0 are read/writable	0	R/W

Note:
1. BUSY and WEL are read only.
2. BP0~3, QE and BPL bits are non-volatile.

Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If this bit is set to "1", it indicates the device is Write enabled. If the bit is set to "0" (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. This bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instructions

BUSY

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A "1" for the BUSY bit indicates the device is busy with an operation in progress. A "0" indicates the device is ready for the next valid operation.

Quad Enable (QE)

When the Quad Enable bit is reset to "0" (factory default), $\overline{WP}$ and $\overline{HOLD}$ pins are enabled. When QE pin is set to "1", Quad SIO_2 and SIO_3 are enabled. (The QE should never be set to "1" during standard and Dual SPI operation if the $\overline{WP}$ and $\overline{HOLD}$ pins are tied directly to the V_{DD} or V_{SS}.). When in QPI mode, QE bit is not required for setting.

Table 3: Block Protection Table

Protection Level	Status Register Bit				Protected Memory Area
	BP3	BP2	BP1	BP0	64KB Block Range
0	0	0	0	0	None
Upper 1/8	0	0	0	1	Block 7
Upper 1/4	0	0	1	0	Block 6~7
Upper 1/2	0	0	1	1	Block 4~7
All Blocks	0	1	0	0	Block 0~7
Upper 6/8	0	1	0	1	Block 2~7
Upper 7/8	0	1	1	0	Block 1~7
All Blocks	0	1	1	1	Block 0~7
0	1	0	0	0	None
Bottom 1/8	1	0	0	1	Block 0
Bottom 1/4	1	0	1	0	Block 0~1
Bottom 1/2	1	0	1	1	Block 0~3
All Blocks	1	1	0	0	Block 0~7
Bottom 6/8	1	1	0	1	Block 0~5
Bottom 7/8	1	1	1	0	Block 0~6
All Blocks	1	1	1	1	Block 0~7

Block Protection (BP3, BP2, BP1, BP0)

The Block-Protection (BP3, BP2, BP1, BP0) bits define the memory area, as defined in Table 3, to be software protected against any memory Write (Program or Erase) operations. The Write Status Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as $\overline{WP}$ is high or the Block- Protection-Look (BPL) bit is 0. Chip Erase can only be executed if BP3, BP2, BP1 and BP0 bits are all 0. The factory default setting for Block Protection Bit (BP3 ~ BP0) is 0.

Block Protection Lock-Down (BPL)

$\overline{WP}$ pin driven low (V_{IL}), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP3, BP2, BP1 and BP0 bits. When the $\overline{WP}$ pin is driven high (V_{IH}), the BPL bit has no effect and its value is “Don’t Care”.

■ HOLD OPERATION

$\overline{HOLD}$ pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the $\overline{HOLD}$ mode, $\overline{CE}$ must be in active low state. The $\overline{HOLD}$ mode begins when the SCK active low state coincides with the falling edge of the $\overline{HOLD}$ signal. The HOLD mode ends when the $\overline{HOLD}$ signal's rising edge coincides with the SCK active low state.

If the falling edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state.

Similarly, if the rising edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 1 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If $\overline{CE}$ is driven active high during a Hold condition, it resets the internal logic of the device. As long as $\overline{HOLD}$ signal is low, the memory remains in the Hold condition. To resume communication with the device, $\overline{HOLD}$ must be driven active high, and $\overline{CE}$ must be driven active low. See Figure 30 for Hold timing.

The $\overline{HOLD}$ function is only available for Standard SPI and Dual SPI operation, not during Quad SPI because this pin is used for SIO_3 when the QE bit of Status Register is set for Quad I/O or during QPI mode.

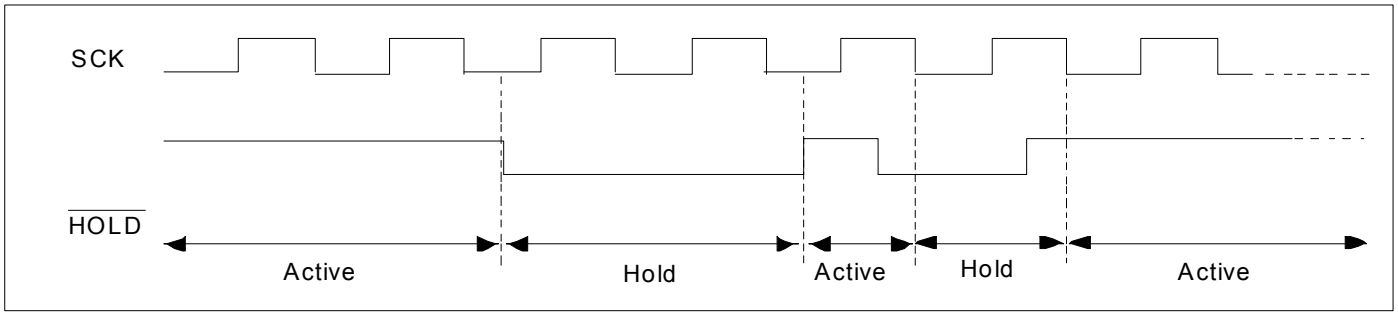


Figure 1: HOLD Condition Waveform

■ WRITE PROTECTION

The device provides software Write Protection.

The Write-Protect pin ($\overline{WP}$) enables or disables the lock-down function of the Status Register. The Block-Protection bits (BP3, BP2, BP1, BP0 and BPL) in the Status Register provide Write protection to the memory array and the Status Register. When the QE bit of Status Register is set for Quad I/O or the system enter QPI mode, the $\overline{WP}$ pin function is not available since this pin is used for SIO_2.

Write Protect Pin ($\overline{WP}$)

The Write-Protect ($\overline{WP}$) pin enables the lock-down function of the BPL bit (bit 7) in the Status Register. When $\overline{WP}$ is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4). When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled.

Table 4: Conditions to Execute Write-Status- Register (WRSR) Instruction

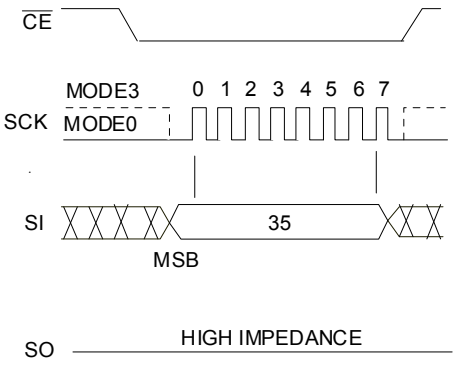
$\overline{WP}$	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enable.



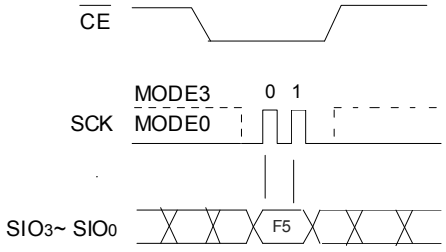
Quad Peripheral Interface (QPI) operation

To use QPI protocol, the host drives $\overline{CE}$ low then sends the Fast Read command, 0BH, followed by 6 address cycles and 4 dummy cycles. Most significant bit (MSB) comes first (Please refer to Figure 8-2).

After the dummy cycle, the Quad Peripheral Interface (QPI) Flash Memory outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on $\overline{CE}$. The internal address pointer automatically increases until the highest memory address is reached. When reached the highest memory address, the address pointer returns to the beginning of the address space.

Reset QPI mode

By issuing F5H command, the device is reset to 1-I/O SPI mode.



Fast Read Quad I/O mode (4READ)

To increase the code transmission speed, the device provides a "Fast Read Quad I/O Mode" (4READ). By issuing command code EBH, the 4READ mode is enable. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 84MHz to 104MHz. (Please refer to Figure 10-2)

■ INSTRUCTIONS

Instructions are used to Read, Write (Erase and Program), and configure the F25D04QA. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Page Program, Write Status Register, Sector Erase, Block Erase, or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of $\overline{CE}$. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. $\overline{CE}$ must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID, Read Status Register, Read Electronic Signature instructions). Any low to high transition on $\overline{CE}$, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

Table 5-1: Device Operation Instruction (SPI)

Operation	Max. Freq	SPI Bus Cycle [1~3]													
		1		2		3		4		5		6		N	
		S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read	33 MHz	03H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	D_{OUT0}	X	D_{OUT1}	X	cont.
Fast Read	104MHz	0BH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	X	X	D_{OUT0}	X	cont.
Fast Read Dual I/O[12, 13] (**2READ**)	84MHz	BBH		A_{23}-A_8		A_7-A_0, M_7-M_0		$D_{OUT0~1}$		cont.		-		-	
Fast Read Quad I/O[14] (4 dummy cycles) (**W4READ**)		E7H		A_{23}-A_0, M_7-M_0		X, $D_{OUT\ 0~2}$		Cont.		-		-		-	
Fast Read Quad I/O[12, 14] (**4READ**)	104MHz	EBH		A_{23}-A_0, M_7-M_0		X, $D_{OUT0~1}$		$D_{OUT2~6}$		cont.		-		-	
Sector Erase[4] - 4KB (**SE**)		20H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Block Erase 32KB[5] (**BE32K**)		52H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Block Erase[5] (**BE**)		D8H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Chip Erase (**CE**)		60H / C7H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Program / Erase Suspend		B0H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Program / Erase Resume		30H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Page Program (**PP**)		02H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN0}	Hi-Z	D_{IN1}	Hi-Z	Up to 256 bytes	Hi-Z
Quad Page Program (**4PP**)[15]		38h		A_{23}~A_0, $D_{IN\ 0}$		$D_{IN\ 1~4}$		$D_{IN\ 5~8}$		$D_{IN\ 9~12}$		$D_{IN\ 13~16}$		Up to 256 byte	
Mode Bit Reset[16]		FFH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Read Status Register (**RDSR**)[7]		05H	Hi-Z	X	D_{OUT} (S_7-S_0)	-	-	-	-	-	-	-	-	-	-
Write Status Register (**WRSR**)[10]		01H	Hi-Z	D_{IN} (S_7-S_0)	Hi-Z	-	-	-.	-	-	-	-	-	-	-
Write Enable (**WREN**)[10]		06H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Write Disable (**WRDI**)		04H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-

Table 5-1: Device Operation Instruction (SPI) - Continued

Operation	Max. Freq	SPI Bus Cycle [1~3]													
		1		2		3		4		5		6		N	
		S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read Electronic Signature (**RES**) [8]	104MHz	ABH	Hi-Z	X	X	X	X	X	X	X	12H	-	-	-	-
RES in secured OTP mode & not lock down		ABH	Hi-Z	X	X	X	X	X	X	X	52H	-	-	-	-
RES in secured OTP mode & lock down		ABH	Hi-Z	X	X	X	X	X	X	X	D2H	-	-	-	-
Read ID (**RDID**) [9]		9FH	Hi-Z	X	8CH	X	40H	X	13H	-	-	-	-	-	-
Read Electronic ID (**REMS**) [11]		90H	Hi-Z	00H	Hi-Z	00H	Hi-Z	00H	Hi-Z	X	8CH	X	12H	-	-
								01H	Hi-Z	X	12H	X	8CH	-	-
Deep Power Down (**DP**)		B9H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Release from Deep Power Down (**RDP**)		ABH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Enter secured OTP mode (**ENSO**)		B1H	Hi-Z	-	-	-	-	-.	-	-	-	-	-	-	-
Exit OTP (**EXSO**)		C1H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Read Security Register (**RDSCUR**)		2BH	Hi-Z	X	D_{OUT}	-	-	-	-	-	-	-	-	-	-
Write Security Register (**WRSCUR**)		2FH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Reset Enable (**RSTEN**)		66H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Reset Memory (**RST**) [6]		99H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Signal Block Lock (**SBLK**)		36H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Signal Block Unlock (**SBULK**)		39H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Block Protect Read (**RDBLOCK**)		3CH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Gang Block Lock (**GBLK**)		7EH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Gang Block Unlock (**GBULK**)		98H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Write Protect Selection (**WPSEL**)		68H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Set Burst Length (**SBL**)		C0H	Hi-Z	D_{IN}	Hi-Z	-	-	-	-	-	-	-	-	-	-
Enable Quad I/O (**EQIO**)		35H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
NOP		00H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-

Table 5-2: Device Operation Instruction (QPI)

Operation	Max. Freq	QPI Bus Cycle [1~3]								
		1	2	3	4	5	6	7	8	N
		S_{IO}	S_{IO}	S_{IO}	S_{IO}	S_{IO}	S_{IO}	S_{IO}	S_{IO}	S_{IO}
Fast Read	84MHz	0BH	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	X	X	D_{OUT0}	D_{OUT1}	cont.
Fast Read Quad I/O[12, 14] (**4READ**)	104MHz	EBH	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	M_7-M_0	X	X	D_{OUT0}	cont.
Sector Erase[4] - 4KB (**SE**)		20H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Block Erase 32KB[5] (**BE32K**)		52H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Block Erase[5] (**BE**)		D8H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Chip Erase (**CE**)		60H / C7H	-	-	-	-	-	-	-	-
Program / Erase Suspend		B0H	-	-	-	-	-	-	-	-
Program / Erase Resume		30H	-	-	-	-	-	-	-	-
Page Program (**PP**)		02H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	D_{IN0}	D_{IN1}	D_{IN2}	D_{IN3}	Up to 256 bytes
Mode Bit Reset[16]		FFH	FFH	FFH	FFH	-	-	-	-	-
Read Status Register (**RDSR**)[7]		05H	D_{OUT} (S_7-S_0)	-	-	-	-	-	-	-
Write Status Register (**WRSR**)[10]		01H	D_{IN} (S_7-S_0)	-	-	-	-	-	-	-
Write Enable (**WREN**)[10]		06H	-	-	-	-	-	-	-	-
Write Disable (**WRDI**)		04H	-	-	-	-	-	-	-	-
Read Electronic Signature (**RES**)[8]		ABH	X	X	X	12H	-	-	-	-
RES in secured OTP mode & not lock down		ABH	X	X	X	52H	-	-	-	-
RES in secured OTP mode & lock down		ABH	X	X	X	D2H	-	-	-	-
Deep Power Down (**DP**)		B9H	-	-	-	-	-	-	-	-
Release from Deep Power Down (**RDP**)		ABH	-	-	-	-	-	-	-	-
Exit OTP (**EXSO**)		C1H	-	-	-	-	-	-	-	-
Enter secured OTP mode (**ENSO**)		B1H	-	-	-	-	-	-	-	-
Read Security Register (**RDSCUR**)		2BH	D_{OUT}	-	-	-	-	-	-	-
Write Security Register (**WRSCUR**)		2FH	-	-	-	-	-	-	-	-
Reset Enable (**RSTEN**)		66H	-	-	-	-	-	-	-	-
Reset Memory (**RST**)[6]		99H	-	-	-	-	-	-	-	-
Signal Block Lock (**SBLK**)		36H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Signal Block Unlock (**SBULK**)		39H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Block Protect Read (**RDBLOCK**)		3CH	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	-	-	-	-	-
Gang Block Lock (**GBLK**)		7EH	-	-	-	-	-	-	-	-
Gang Block Unlock (**GBULK**)		98H	-	-	-	-	-	-	-	-
Write Protect Selection (**WPSEL**)		68H	-	-	-	-	-	-	-	-
Set Burst Length (**SBL**)		C0H	D_{IN}	-	-	-	-	-	-	-
QPI ID Read (**QPIID**)[9]		AFH	8CH	40H	13H	-	-	-	-	-
Reset Quad I/O (**RSTQIQ**)		F5H	-	-	-	-	-	-	-	-
NOP		00H	-	-	-	-	-	-	-	-

Notes:

1. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out, S_{IO} = Serial In/Out.
2. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary); cont. = continuous
3. One SPI bus cycle is eight clock periods; one QPI bus cycle is two clock periods.
4. 4K byte Sector Earse addresses: use A_{MS} -A_{12}, remaining addresses can be V_{IL} or V_{IH}.

5. 32K byte Block Earse addresses: use A_{MS} -A_{15}, remaining addresses can be V_{IL} or V_{IH}
   64K byte Block Earse addresses: use A_{MS} -A_{16}, remaining addresses can be V_{IL} or V_{IH}
6. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on $\overline{CE}$.
8. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on $\overline{CE}$.
9. The Read ID is output first byte 8CH as manufacture ID; second byte 40H as memory type; third byte 13H as memory capacity.
10. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. A successful WRSR can reset WREN.
11. The Manufacture ID and Device ID output will repeat continuously until $\overline{CE}$ terminates the instruction.
12. Dual and Quad commands use bidirectional IO pins. D_{OUT} and cont. are serial data out; others are serial data in.
13. M_7-M_0: Mode bits. Dual input address:

	Bus Cycle-2	Bus Cycle-3
IO_0 =	(A_{22}, A_{20}, A_{18}, A_{16}, A_{14}, A_{12}, A_{10}, A_8)	(A_6, A_4, A_2, A_0, M_6, M_4, M_2, M_0)
IO_1 =	(A_{23}, A_{21}, A_{19}, A_{17}, A_{15}, A_{13}, A_{11}, A_9)	(A_7, A_5, A_3, A_1, M_7, M_5, M_3, M_1)

14. M_7-M_0: Mode bits. Quad input address:

	Bus Cycle-2
IO_0 =	(A_{20}, A_{16}, A_{12}, A_8, A_4, A_0, M_4, M_0)
IO_1 =	(A_{21}, A_{17}, A_{13}, A_9, A_5, A_1, M_5, M_1)
IO_2 =	(A_{22}, A_{18}, A_{14}, A_{10}, A_6, A_2, M_6, M_2)
IO_3 =	(A_{23}, A_{19}, A_{15}, A_{11}, A_7, A_3, M_7, M_3)

Fast Read Quad I/O data:

	D_{OUT0}	D_{OUT1}	D_{OUT2}	D_{OUT3}	D_{OUT4}	D_{OUT5}
	Bus Cycle-3		Bus Cycle-4			
IO_0 =	(X, X), (X, X), (D_4, D_0),	(D_4, D_0)	(D_4, D_0),	(D_4, D_0),	(D_4, D_0),	(D_4, D_0)
IO_1 =	(X, X), (X, X), (D_5, D_1),	(D_5, D_1)	(D_5, D_1),	(D_5, D_1),	(D_5, D_1),	(D_5, D_1)
IO_2 =	(X, X), (X, X), (D_6, D_2),	(D_6, D_2)	(D_6, D_2),	(D_6, D_2),	(D_6, D_2),	(D_6, D_2)
IO_3 =	(X, X), (X, X), (D_7, D_3),	(D_7, D_3)	(D_7, D_3),	(D_7, D_3),	(D_7, D_3),	(D_7, D_3)

15. The instruction is initiated by executing command code, and then input data to bidirectional IO pins (SIO_0 ~ SIO_3).
    Quad input address and data:

	SPI Bus Cycle
IO_0 =	(A_{20}, A_{16}, A_{12}, A_8, A_4, A_0, D_4, D_0)
IO_1 =	(A_{21}, A_{17}, A_{13}, A_9, A_5, A_1, D_5, D_1)
IO_2 =	(A_{22}, A_{18}, A_{14}, A_{10}, A_6, A_2, D_6, D_2)
IO_3 =	(A_{23}, A_{19}, A_{15}, A_{11}, A_7, A_3, D_7, D_3)

16. This instruction is recommended when using the Dual or Quad Mode bit feature.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: $\overline{CE}$ goes low → sending WREN instruction code → $\overline{CE}$ goes high.
(Please refer to Figure 2-1 and Figure 2-2)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: $\overline{CE}$ goes low → sending WRDI instruction code → $\overline{CE}$ goes high.
(Please refer to Figure 3-1 and Figure 3-2)

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Program/Erase Suspend

(3) Read Identification (RDID)

The RDID instruction is to read the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The ESMT Manufacturer ID is 8CH, the memory type ID is 40H as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "ID Definitions". (Please refer to Table 7)

The sequence of issuing RDID instruction is: $\overline{CE}$ goes low → sending RDID instruction code → 24-bits ID data out on SO → to end RDID operation can drive $\overline{CE}$ to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When $\overline{CE}$ goes high, the device is at standby stage. (Please refer Figure 4)

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in Program/Erase/Write Status Register condition). It is recommended to check the BUSY bit before sending a new instruction when a Program, Erase, or Write Status Register operation is in progress.

The sequence of issuing RDSR instruction is: $\overline{CE}$ goes low → sending RDSR instruction code → Status Register data out on SO.
(Please refer to Figure 5-1 and Figure 5-2)

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in Table 3). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Block Protection Lock-Down (BPL) bit in accordance with Write Protection ($\overline{WP}$ /SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (BUSY) of the Status Register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: $\overline{CE}$ goes low→ sending WRSR instruction code→ Status Register data on SI→ $\overline{CE}$ goes high. (Please refer to Figure 6-1 and Figure 6-2)

The $\overline{CE}$ must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (t_W) is initiated as soon as Chip Enable ($\overline{CE}$) goes high. The BUSY bit still can be check out during the Write Status Register cycle is in progress. The BUSY sets 1 during the t_W timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

Mode	Status register condition	$\overline{WP}$ and BPL bit status	Memory
Software protection mode (SPM)	Status Register can be written in (WEL bit is set to "1") and the BPL, BP0-BP3 bits can be changed	$\overline{WP}$ =1 and BPL bit=0, or $\overline{WP}$ =0 and BPL bit=0, or $\overline{WP}$ =1 and BPL=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The BPL, BP0-BP3 of Status Register bits cannot be changed	$\overline{WP}$ =0, BPL bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 3.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When BPL bit=0, no matter $\overline{WP}$ /SIO_2 is low or high, the WREN instruction may set the WEL bit and can change the values of BPL, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When BPL bit=1 and $\overline{WP}$ /SIO_2 is high, the WREN instruction may set the WEL bit can change the values of BPL, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Note:

If BPL bit=1 but $\overline{WP}$ /SIO_2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When BPL bit=1, and then $\overline{WP}$ /SIO_2 is low (or $\overline{WP}$ /SIO_2 is low before BPL bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the $\overline{WP}$ /SIO_2 to against data modification.

Note:

To exit the hardware protected mode requires $\overline{WP}$ /SIO_2 driving high once the hardware protected mode is entered. If the $\overline{WP}$ /SIO_2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0. If the system set QE=1, the feature of HPM will be disabled.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCK, and data shifts out on the falling edge of SCK at a maximum frequency F_{RSCLK}. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: $\overline{CS}$ goes low → sending READ instruction code → 3-byte address on SI → data out on SO → to end READ operation can use $\overline{CS}$ to high at any time during data out. (Please refer to Figure 7)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The Fast Read instruction is for quickly reading data out. The address is latched on rising edge of SCK, and data of each bit shifts out on the falling edge of SCK at a maximum frequency F_{SCLK}. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached.

SPI mode

The sequence of issuing Fast Read instruction is: $\overline{CE}$ goes low → sending Fast Read instruction code → 3-byte address on SI → 1-dummy byte (default) address on SI → data out on SO → to end Fast Read operation can use $\overline{CE}$ to high at any time during data out. (Please refer to Figure 8-1)

QPI mode

The sequence of issuing Fast Read instruction is: $\overline{CE}$ goes low → sending Fast Read instruction code, 2 cycle → 24-bit address on SIO_3~SIO_0 → 4 dummy cycle → data out interleave on SIO_3~SIO_0 → to end QPI Fast Read operation can use $\overline{CE}$ to high at any time during data out. (Please refer to Figure 8-2)

In the performance-enhancing mode, M[7:4] must be toggling with M[3:0] ; likewise M[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once M[7:4] is no longer toggling with M[3:0]; likewise M[7:0]=FFh, 00h, AAh or 55h and afterwards $\overline{CE}$ is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, Fast Read instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Fast Read Dual I/O (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCK at a maximum frequency F_{TSCLK1}. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: $\overline{CE}$ goes low → sending 2READ instruction → 24-bit address interleave on SIO_1 & SIO_0 → 4 dummy cycles on SIO_1 & SIO_0 → data out interleave on SIO_1 & SIO_0 → to end 2READ operation can use $\overline{CE}$ to high at any time during data out (Please refer to Figure 9).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(9) Fast Read Quad I/O (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of Status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCK at a maximum frequency F_{TSCLK2}. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

SPI mode

The sequence of issuing 4READ instruction is: $\overline{CE}$ goes low → sending 4READ instruction→ 24-bit address interleave on SIO_3,~SIO_0 → 2+4 dummy cycles → data out interleave on SIO_3, SIO_2, SIO_1 & SIO_0 → to end 4READ operation can use $\overline{CE}$ to high at any time during data out. (Please refer to Figure 10-1)

W4READ instruction (E7) is also available is SPI mode for 4 I/O read. The sequence is similar to 4READ, but with only 4 dummy cycles. The clock rate runs at 84MHz.

QPI mode

The sequence of issuing 4READ instruction is: $\overline{CE}$ goes low → sending 4READ instruction→ 24-bit address interleave on SIO_3~SIO_0 → 2+4 dummy cycles → data out interleave on SIO_3~SIO_0 → to end 4READ operation can use $\overline{CE}$ to high at any time during data out. (Please refer to Figure 10-2)

Another sequence of issuing 4 READ instruction especially useful in random access is : $\overline{CE}$ goes low → sending 4READ instruction → 3-bytes address interleave on SIO_3, SIO_2, SIO_1 & SIO_0 → performance enhance toggling bit M[7:0] → 4 dummy cycles → data out still $\overline{CE}$ goes high → $\overline{CE}$ goes low (reduce 4 Read instruction) → 24-bit random access address (Please refer to Figure 22).

In the performance-enhancing mode, M[7:4] must be toggling with M[3:0] ; likewise M[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once M[7:4] is no longer toggling with M[3:0]; likewise M[7:0]=FFh, 00h, AAh or 55h and afterwards $\overline{CE}$ is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) Burst Read

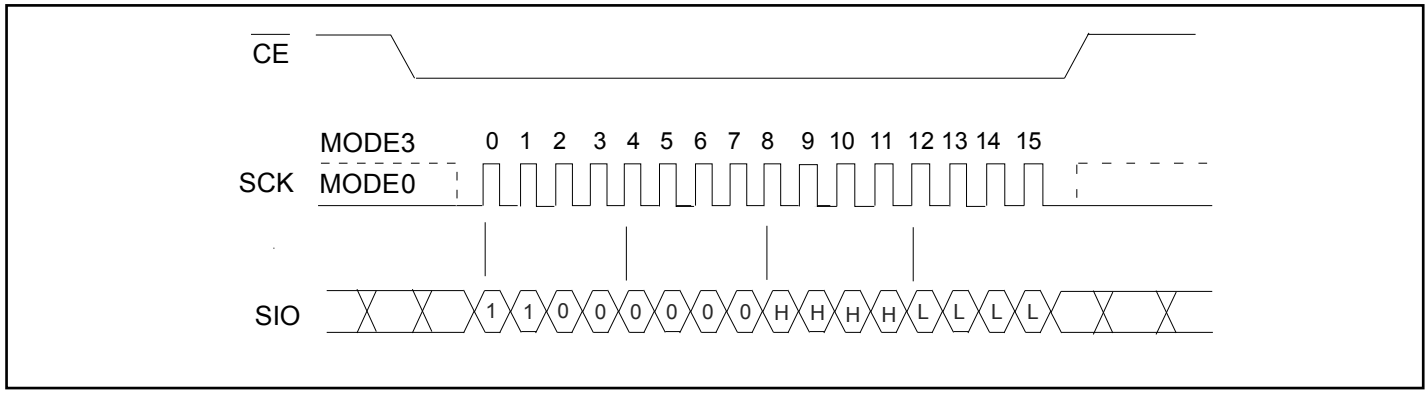
The device supports Burst Read in both SPI and QPI mode. To set the Burst length, following command operation is required Issuing command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with“1h”.

Next 4 clocks is to define wrap around depth. Definition as following table:

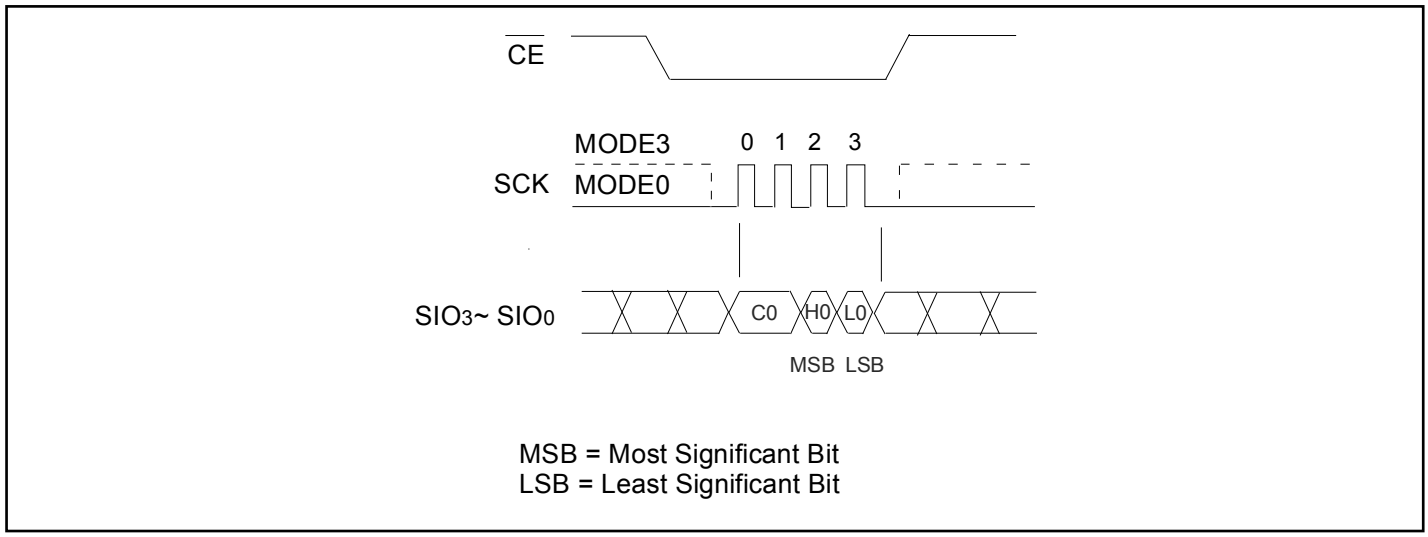
Data	Wrap Around	Wrap Depth	Data	Wrap Around	Wrap Depth
1xh	No	X	00h	Yes	8-byte
1xh	No	X	01h	Yes	16-byte
1xh	No	X	02h	Yes	32-byte
1xh	No	X	03h	Yes	64-byte

The wrap around unit is defined within the 256-byte page, with random initial address. It’s defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0” command in which data=‘1xh”. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is required to issue another “C0” command in which data=“0xh”. QPI “0Bh” “EBh” and SPI “EBh” “E7h” support wrap around feature after wrap around enable. The device id default without Burst read.

SPI Mode



QPI Mode



(11) Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note Figure 11-1 and Figure 11-2)

Performance enhance mode is supported in both SPI and QPI mode. In QPI mode, “EBh” “0Bh” and SPI “EBh” “E7h” commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

After entering enhance mode, following $\overline{CE}$ go high, the device will stay in the read mode and treat $\overline{CE}$ go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue ”FFh” command to exit enhance mode.

(12) Mode Bit Reset (FFh)

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh command code, 8 clocks, should be issued in Signal I/O sequence. In QPI mode, FFFFFFFFh command code, 8 clocks, in 4 I/O should be issue (Please refer to Figure 23)

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

Upon Reset of main chip, SPI instruction would be issued from the system. Instructions like Read ID (9Fh) or Fast Read (0Bh) would be issued.

(13) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table of memory organization) is a valid address for Sector Erase (SE) instruction. The $\overline{CE}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [A_{MS}-A_{12}] (A_{MS} is the most significant address) select the sector address.

The sequence of issuing SE instruction is: $\overline{CE}$ goes low → sending SE instruction code → 3-byte address on SI → $\overline{CE}$ goes high. (Please refer to Figure 14-1 and Figure 14-2)

The self-timed Sector Erase Cycle time (T_{SE}) is initiated as soon as $\overline{CE}$ goes high. The BUSY bit still can be check out during the Sector Erase cycle is in progress. The BUSY sets 1 during the T_{SE} timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

(14) 32K Byte Block Erase (BE32K)

The 32K Byte Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see table of memory organization) is a valid address for Block Erase (BE32K) instruction. The $\overline{CE}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: $\overline{CE}$ goes low → sending BE32K instruction code → 3-byte address on SI → $\overline{CE}$ goes high. (Please refer to Figure 15-1 and Figure 15-2)

The self-timed Block Erase Cycle time (T_{BE1}) is initiated as soon as Chip Enable ($\overline{CE}$) goes high. The BUSY bit still can be check out during the Block Erase cycle is in progress. The BUSY sets 1 during the T_{BE1} timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE32K) instruction will not be executed on the block.

(15) 64K Byte Block Erase (BE)

The 64K Byte Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to table of memory organization) is a valid address for Block Erase (BE) instruction. The $\overline{CE}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: $\overline{CE}$ goes low → sending BE instruction code → 3-byte address on SI → $\overline{CE}$ goes high. (Please refer to Figure 16-1 and Figure 16-2)

The self-timed Block Erase Cycle time (T_{BE2}) is initiated as soon as $\overline{CE}$ goes high. The BUSY bit still can be check out during the Block Erase cycle is in progress. The BUSY sets 1 during the T_{BE2} timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

(16) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The $\overline{CE}$ must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: $\overline{CE}$ goes low → sending CE instruction code → $\overline{CE}$ goes high.
(Please refer to Figure 17-1 and Figure 17-2)

The self-timed Chip Erase Cycle time (T_{CE}) is initiated as soon as $\overline{CE}$ goes high. The BUSY bit still can be check out during the Chip Erase cycle is in progress. The BUSY sets 1 during the T_{CE} timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

(17) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A_7-A_0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A_7-A_0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A_7-A_0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: $\overline{CE}$ goes low → sending PP instruction code → 3-byte address on SI → at least 1-byte on data on SI → $\overline{CE}$ goes high. (Please refer to Figure 12-1 and Figure 12-2)

The $\overline{CE}$ must be kept to low during the whole Page Program cycle; The $\overline{CE}$ must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (T_{PP}) is initiated as soon as $\overline{CE}$ goes high. The BUSY bit still can be check out during the Page Program cycle is in progress. The BUSY sets 1 during the T_{PP} timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(18) Quad Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO_0, SIO_1, SIO_2, and SIO_3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 33MHz. For system with faster clock, the Quad Page Program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 33MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: $\overline{CE}$ goes low → sending 4PP instruction code → 3-byte address on SIO[3:0] → at least 1-byte on data on SIO[3:0] → $\overline{CE}$ goes high.

(19) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from I_{SB1} to I_{SB2}). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When $\overline{CE}$ goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: $\overline{CE}$ goes low → sending DP instruction code → $\overline{CE}$ goes high.
(Please refer to Figure 18-1 and Figure 18-2)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and software reset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction, the $\overline{CE}$ must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as $\overline{CE}$ goes high, a delay of T_{DP} is required before entering the Deep Power-down mode.

(20) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving $\overline{CE}$ High. When $\overline{CE}$ is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by T_{RES2}, and $\overline{CE}$ must remain High for at least T_{RES2} (max), as specified in Table 14. AC Characteristics. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The sequence is shown as Figure 19-1, Figure 19-2, Figure 20-1 and Figure 20-2. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The RES instruction is ended by $\overline{CE}$ goes high after the ID has been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCK while $\overline{CE}$ is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of T_{RES2} to transit to standby mode, and $\overline{CE}$ must remain high at least T_{RES2} (max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

(21) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the $\overline{CE}$ pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A_7~A_0). After which, the Manufacturer ID for ESMT (8Ch) and the Device ID are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 21. The Device ID values are listed in Table 7 of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CE}$ high.

(22) QPI ID Read (QPIID)

The QPIID Read instruction identifies the devices as F25D04QA and manufacturer as ESMT. The sequence of issue QPIID instruction is $\overline{CE}$ goes low → sending QPI ID instruction → Data out on SO → $\overline{CE}$ goes high. Most significant bit (MSB) first.

Immediately following the command cycle the device outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of $\overline{CE}$. The device outputs three bytes of data: manufacturer, device type, and device ID.

Table 7. ID Definitions

Command Type	F25D04QA		
RDID (JEDEC ID)	manufacturer ID	memory type	memory density
	8C	**40**	**13**
RES	electronic ID	in secured OTP mode & non lock down	in secured OTP mode & lock down
	12	**52**	**D2**
REMS	manufacturer ID	device ID	
	8C	**12**	

(23) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512 bytes secured OTP mode. The additional 512 bytes secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: $\overline{CE}$ goes low → sending ENSO instruction to enter Secured OTP mode → $\overline{CE}$ goes high.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(24) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512 bytes secured OTP mode.
The sequence of issuing EXSO instruction is: $\overline{CE}$ goes low→ sending EXSO instruction to exit Secured OTP mode→ $\overline{CE}$ goes high.

(25) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in Program/Erase/Write Status Register/Write Security Register condition) and continuously.

The sequence of issuing RDSCUR instruction is: $\overline{CE}$ goes low → sending RDSCUR instruction → Security Register data out on SO→ $\overline{CE}$ goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512 bytes Secured OTP area cannot be update any more. While it is in 512 bytes secured OTP mode, main array access is not allowed.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	Erase Suspend bit	Program Suspend bit	LDSO (indicate if lock-down)	Secured OTP indicator bit
0 = normal WP mode 1 = individual mode (default = 0)	0 = normal Erase succeed 1 = individual Erase failed (default = 0)	0 = normal Program succeed 1= indicate Program failed (default = 0)	-	0 = Erase is not suspended 1= Erase suspended (default = 0)	0 = Program is not suspended 1= Program suspended (default = 0)	0 = not lock-down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

(26) Write Security Register (WRSCUR)

The WRSCUR instruction is for setting the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512 bytes Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more. The LDSO bit is an OTP bit. Once the LDSO bit is set, the value of LDSO bit can not be altered any more.

The sequence of issuing WRSCUR instruction is: $\overline{CE}$ goes low → sending WRSCUR instruction → $\overline{CE}$ goes high.

The $\overline{CE}$ must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

(27) Write Protection Selection (WPSEL)

When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. The WREN (Write Enable) instruction is required before issuing WPSEL instruction. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods.

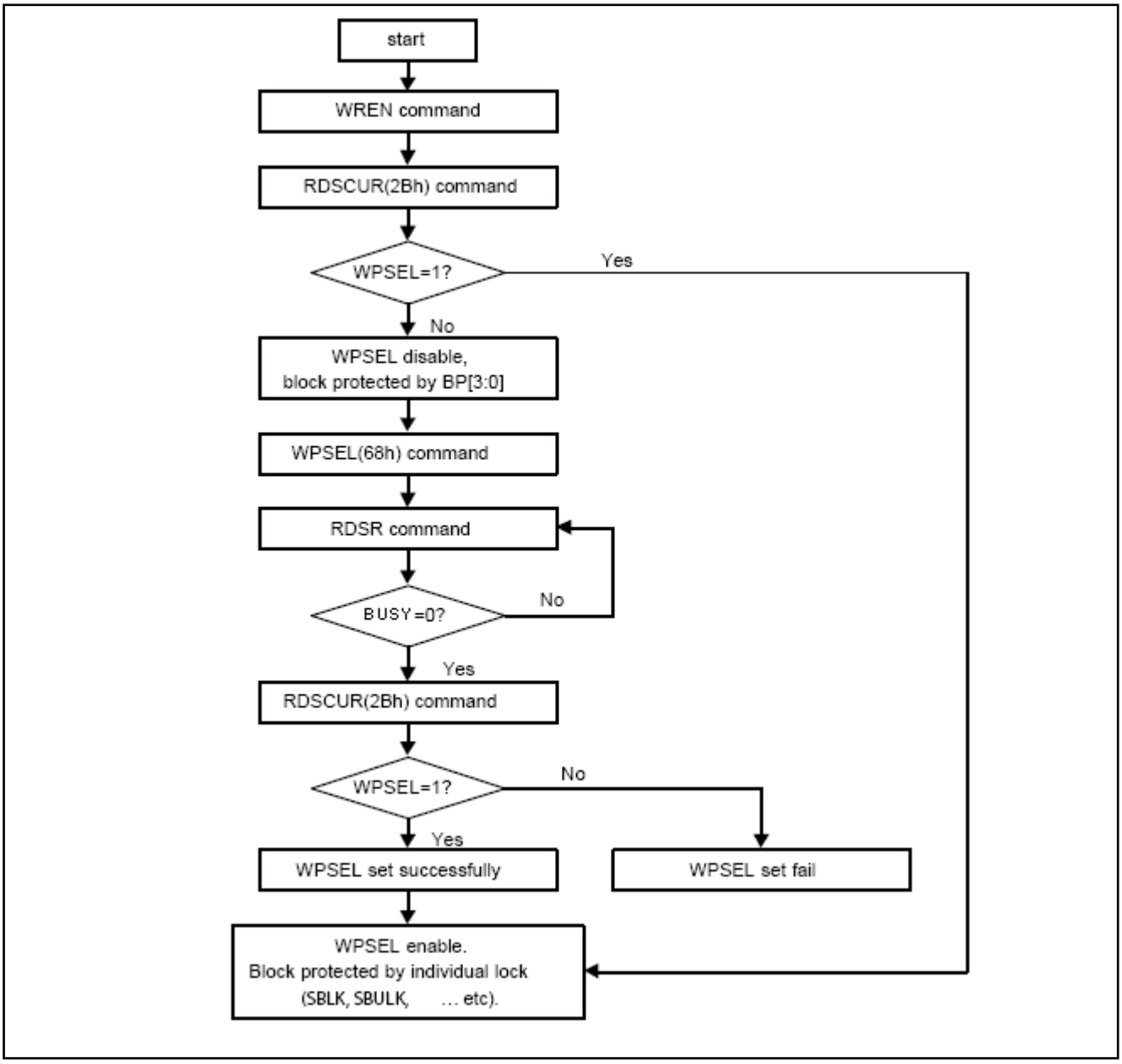
The sequence of issuing WPSEL instruction is: $\overline{CE}$ goes low → sending WPSEL instruction to enter the individual block protect mode → $\overline{CE}$ goes high.

Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

Once WPSEL is set, it cannot be changed.

WPSEL instruction function flow is as follows:

WPSEL Flow



(28) Single Block Lock/Unlock Protection (SBLK/SBULK)

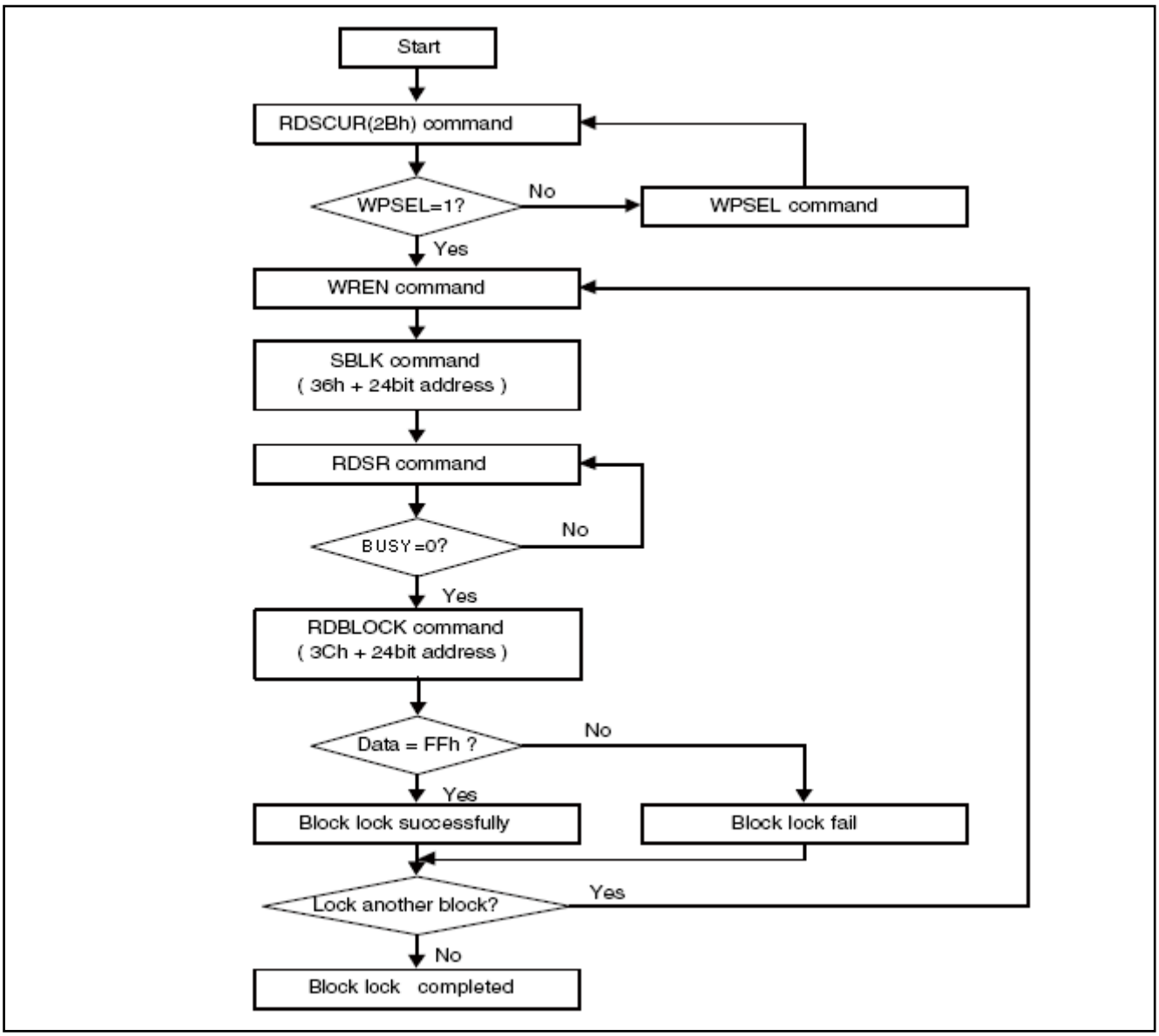
These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block (or sector) of memory, using A_{MS}-A_{16} or (A_{MS}-A_{12}) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.

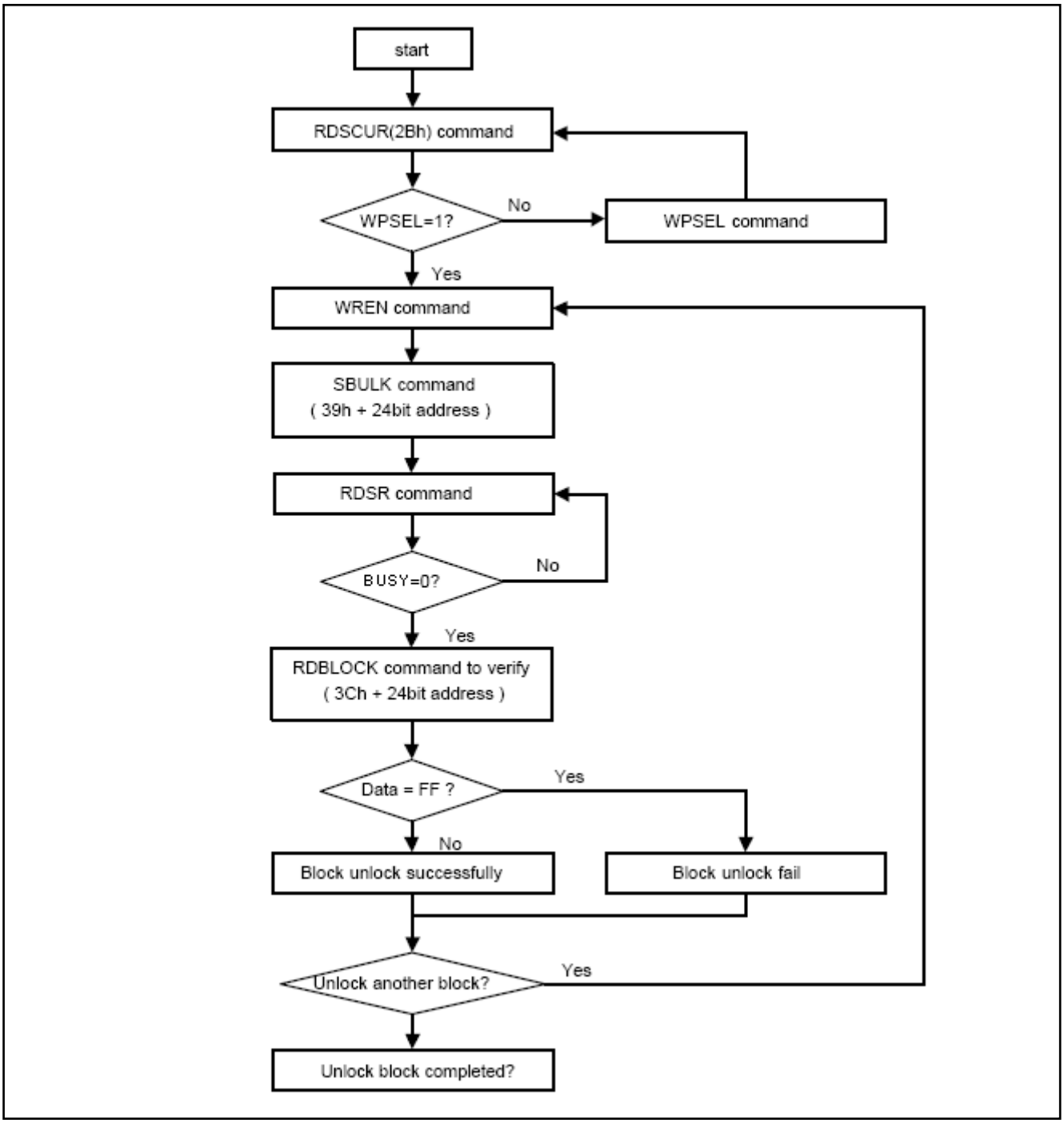
The sequence of issuing SBLK/SBULK instruction is: $\overline{CE}$ goes low → send SBLK/SBULK (36h/39h) instruction → send 3 address bytes assign one block (or sector) to be protected on SI pin → $\overline{CE}$ goes high. The $\overline{CE}$ must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

SBLK/SBULK instruction function flow is as follows:

Block Lock Flow



Block Unlock Flow



(29) Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using A_{MS}-A_{16} (or A_{MS}-A_{12}) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has been protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: $\overline{CE}$ goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → $\overline{CE}$ goes high.

(30) Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.

The sequence of issuing GBLK/GBULK instruction is: $\overline{CE}$ goes low → send GBLK/GBULK (7Eh/98h) instruction → $\overline{CE}$ goes high.

The $\overline{CE}$ must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

(31) Program/ Erase Suspend/ Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations. Details as follows.

To enter the suspend / resume mode: issuing B0h for suspend; 30h for resume (SPI/QPI all acceptable).
Read security register bit2 (PSB) and bit3 (ESB) (please refer to Table 8) to check suspend ready information.
Suspend to suspend ready timing: 20us.
Resume to another suspend timing: 1ms.

ESB bit (Erase Suspend Bit) indicates the status of Erase suspend operation. When issue a suspend command during erase operation ESB=1, when erase operation resumes, ESB will be reset to "0".

(31-1) Erase Suspend

Erase suspend allow the interruption of all erase operations.

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, BBh, EBh, E7h, 9Fh, 90h, 05h, 2Bh, B1h, C1h, 3Ch, 30h, 66h, 99h, C0h, 00h, ABh)

After issue erase suspend command, latency time 20us is needed before issue another command. For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note Figure 26-1, Figure 26-2 and Figure 26-3.

ESB bit (Erase Suspend Bit) indicates the status of Erase suspend operation. When issue a suspend command during program operation ESB=1, when erase operation resumes, ESB will be reset to "0".

When ESB bit is issued, the Write Enable Latch (WEL) bit will be reset. See Figure 26-1 for Suspend to Read latency.

(31-2) Program Suspend

Program suspend allows the interruption of all program operations.

After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, BBh, EBh, E7h, 9Fh, 90h, 05h, 2Bh, B1h, C1h,3Ch, 30h, 66h, 99h, C0h, 00h, ABh)

After issue program suspend command, latency time 20us is needed before issue another command.
For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note Figure 26-1, Figure 26-2 and Figure 26-3.

PSB bit (Program Suspend Bit) indicates the status of Program suspend operation. When issue a suspend command during program operation PSB=1, when program operation resumes, PSB will be reset to "0".

(32) Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status Register will be changed back to “0”

The operation of Write-Resume is as follows: $\overline{CE}$ drives low → send write resume command cycle (30h) → drive $\overline{CE}$ high. By polling Busy Bit in Status Register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of T_{SE}, T_{BE}, T_{PP} for Sector-erase, Block-erase or Page-programming. WREN (command "06" is not required to issue before resume. Resume to another suspend operation requires latency time of 1ms.

When Erase Suspend is being resumed, the WEL bit need to be set again if user desire to conduct the program or erase operation.

Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resume. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disable, the write-resume command is effective.

(33) No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

(34) Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

To reset the F25D04QA the host drives $\overline{CE}$ low, sends the Reset-Enable command (66h), and drives $\overline{CE}$ high. Next, the host drives $\overline{CE}$ low again, sends the Reset command (99h), and drives $\overline{CE}$ high.

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

A successful command execution will reset the device to SPI stand-by read mode, which are their respective default states, see Figure 27. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the V_{DD} achieves below correct level:
- V_{DD} minimum at power-up stage and then after a delay of T_{VSL}
- GND at power-down

Please note that a pull-up resistor on $\overline{CE}$ may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When V_{DD} is lower than V_{WI} (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after V_{DD} reaching the V_{WI} level, a T_{PUW} time delay is required before the device is fully accessible for commands like Write Enable (WREN), Page Program (PP), Quad Page Program (4PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE), Chip Erase (CE), WRSCUR and Write Status Register (WRSR). If the V_{DD} does not reach the V_{DD} minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- T_{PUW} after V_{DD} reached V_{WI} level
- T_{VSL} after V_{DD} reached V_{DD} minimum level

The device can accept read command after V_{DD} reached V_{DD} minimum and a time delay of T_{VSL}, even time of T_{PUW} has not passed. Please refer to the figure of "power-up timing".

Note:
- To stabilize the V_{DD} level, the V_{DD} rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the V_{DD} drops below V_{WI} level, all operations are disabled and device has no response to any command.

The data corruption might occur during the stage while a write, program, erase cycle is in progress.

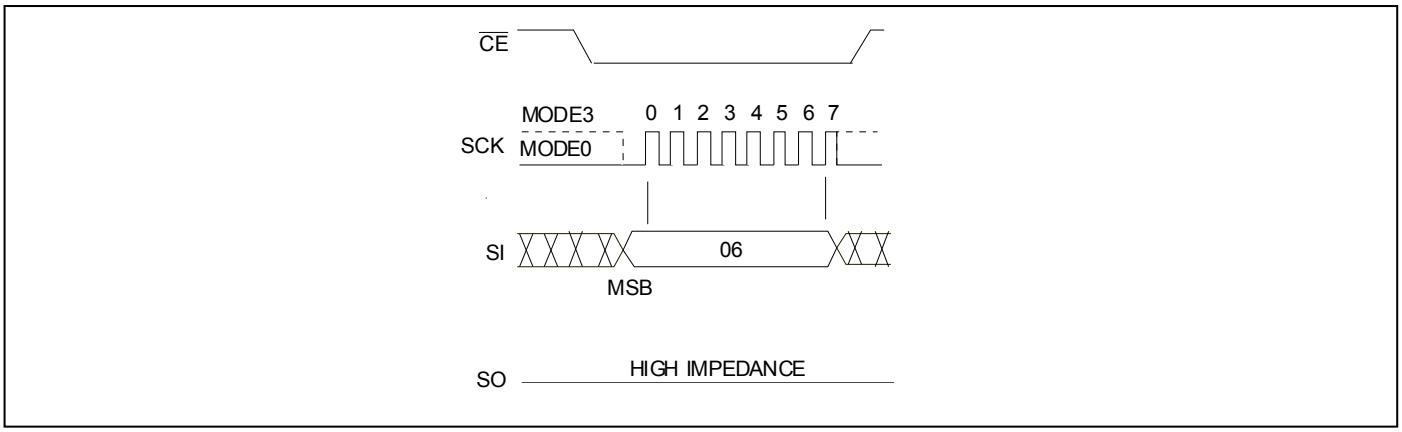


Figure 2-1: Write Enable (WREN) Sequence (SPI Mode)

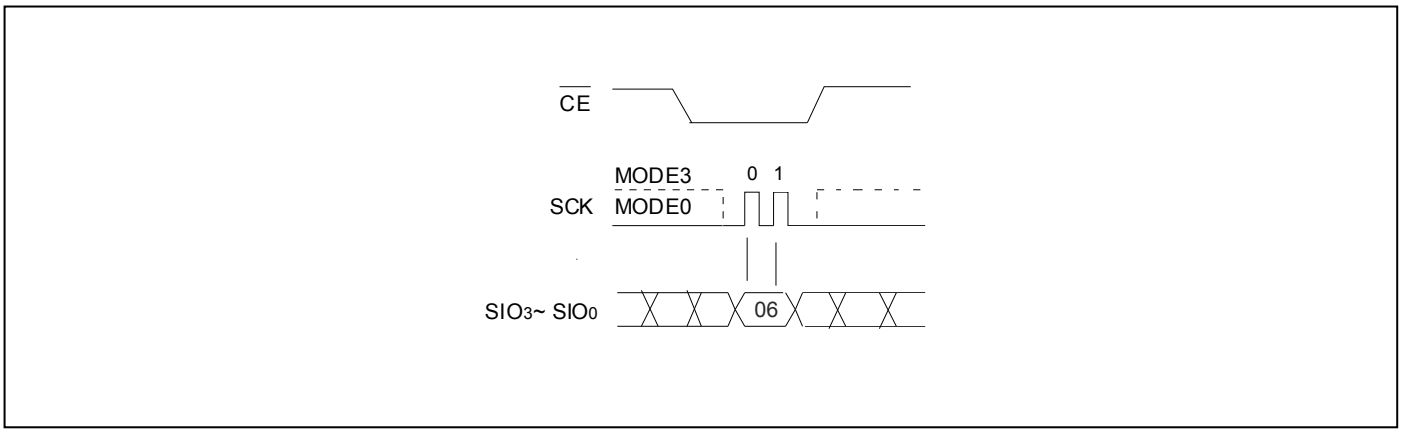


Figure 2-2: Write Enable (WREN) Sequence (QPI Mode)

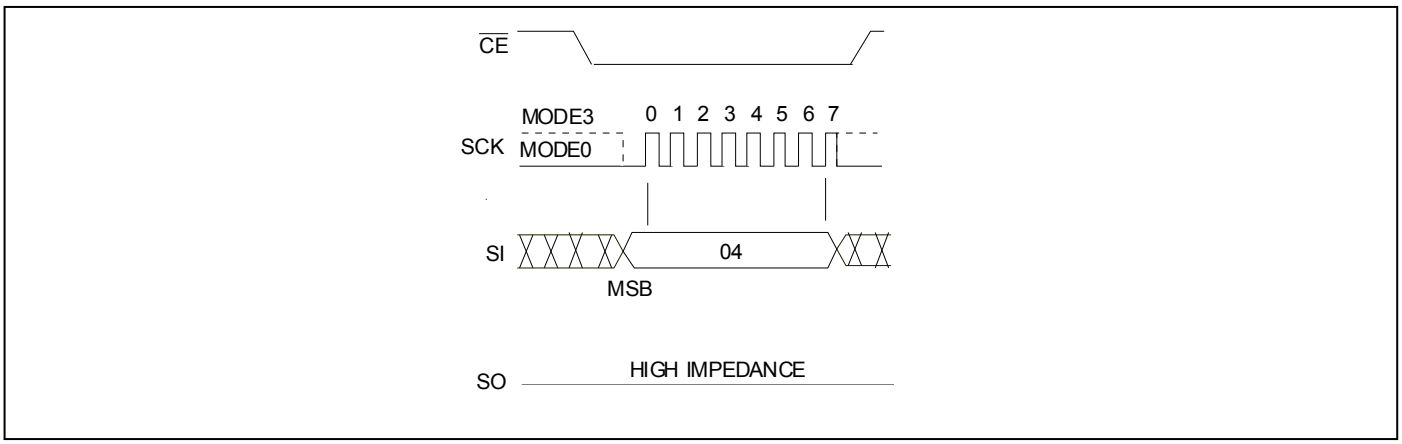


Figure 3-1: Write Disable (WRDI) Sequence (SPI Mode)

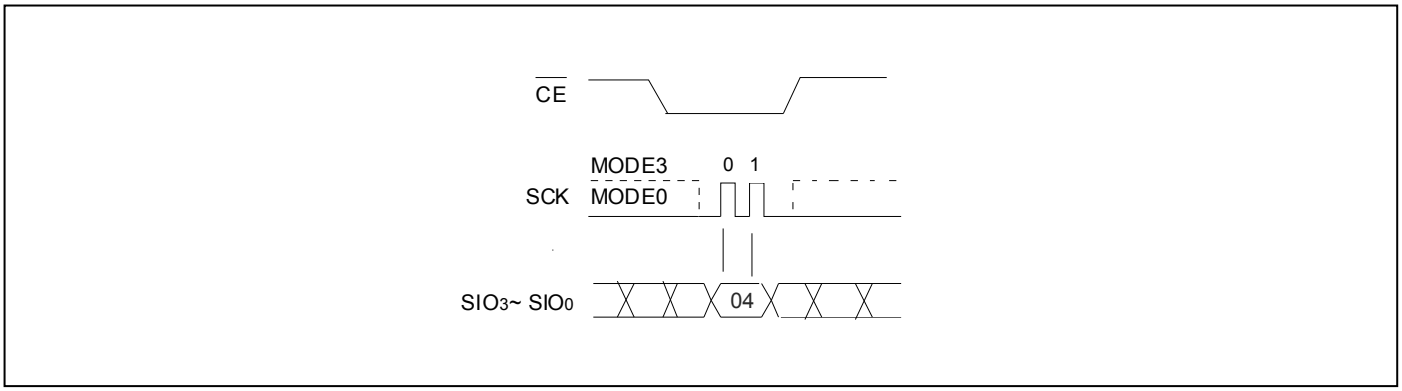


Figure 3-2: Write Disable (WRDI) Sequence (QPI Mode)

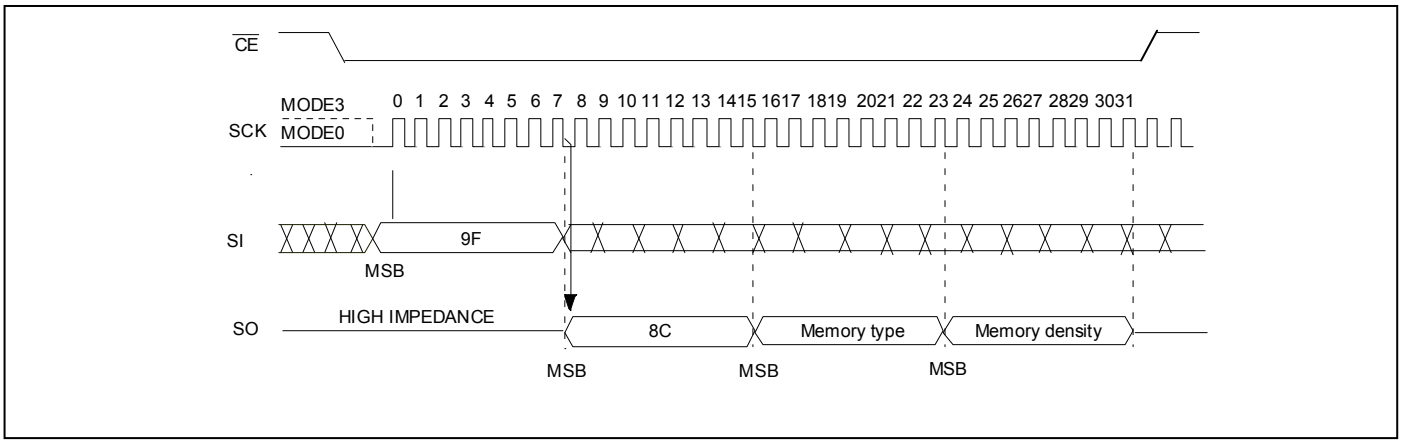


Figure 4: Read Identification (RDID) Sequence (SPI Mode)

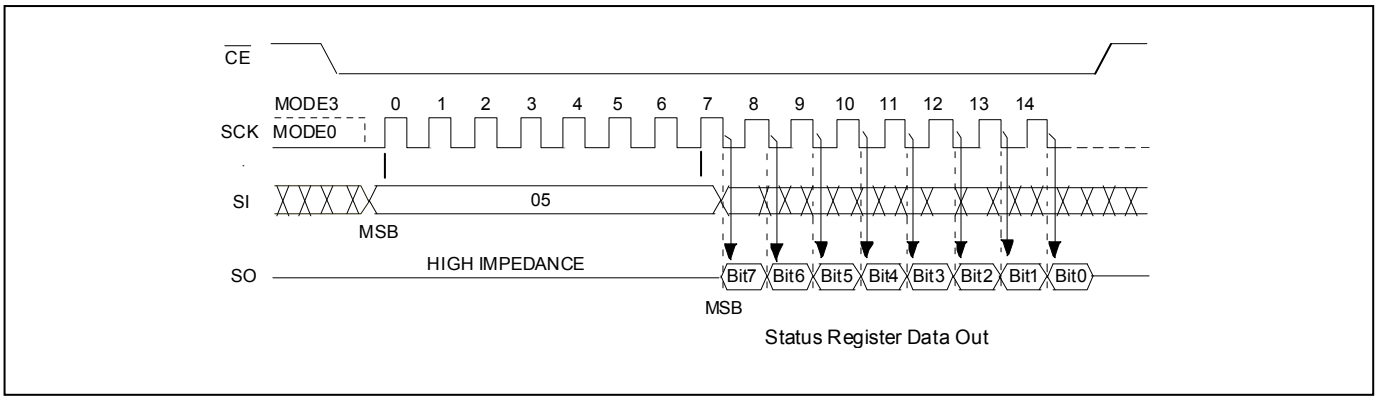


Figure 5-1: Read Status Register (RDSR) Sequence (SPI Mode)

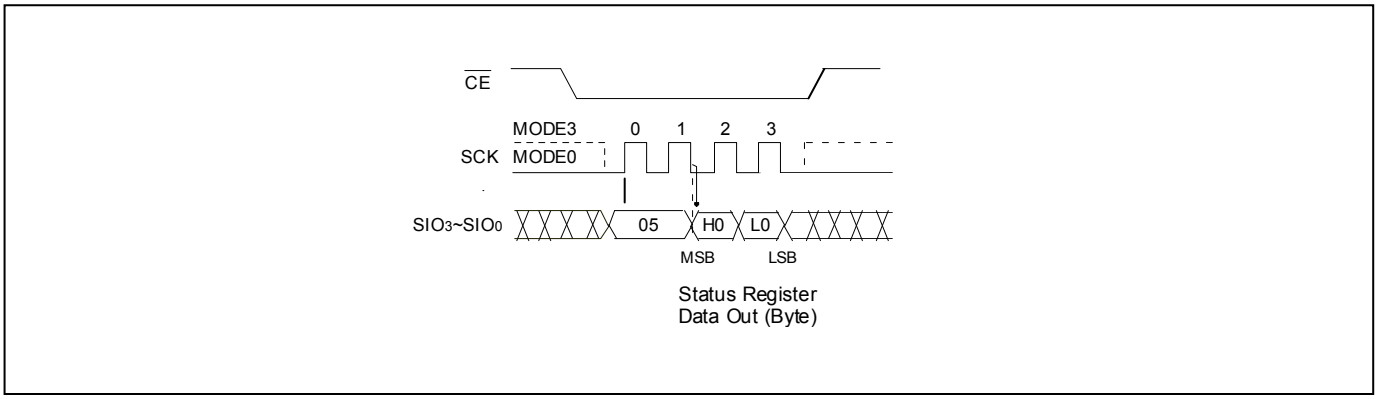


Figure 5-2: Read Status Register (RDSR) Sequence (QPI Mode)

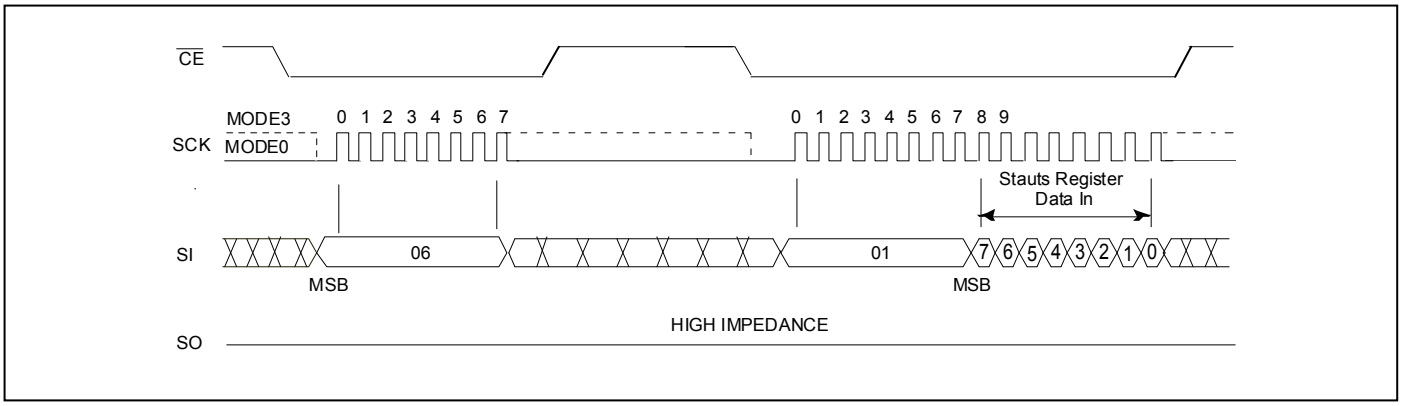


Figure 6-1: Write Enable (WREN) and Write Status Register (WRSR) Sequence (SPI Mode)

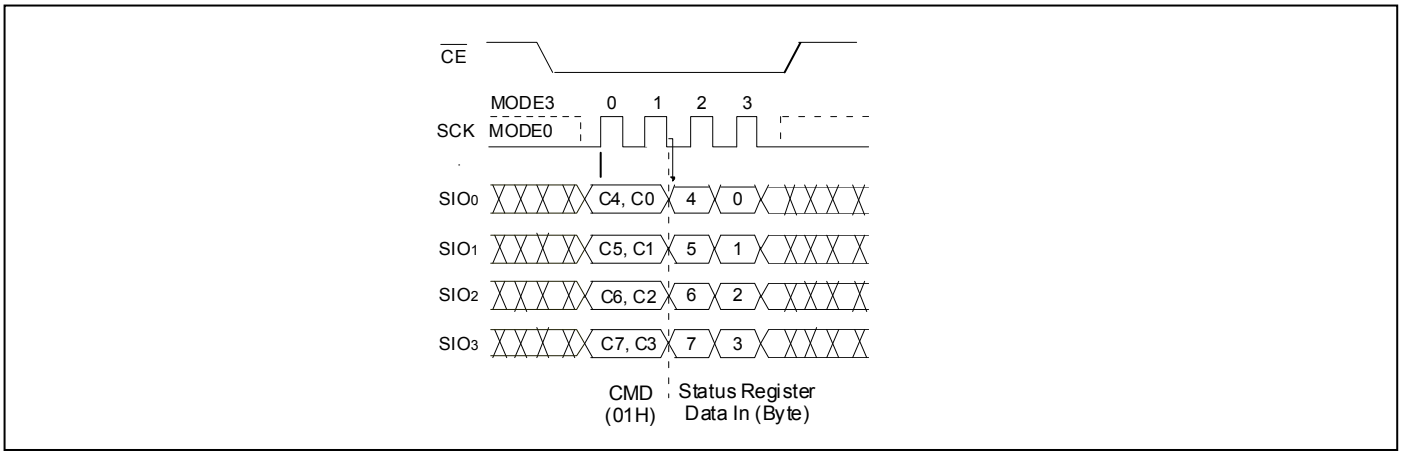


Figure 6-2: Write Status Register (WRSR) Sequence (QPI Mode)

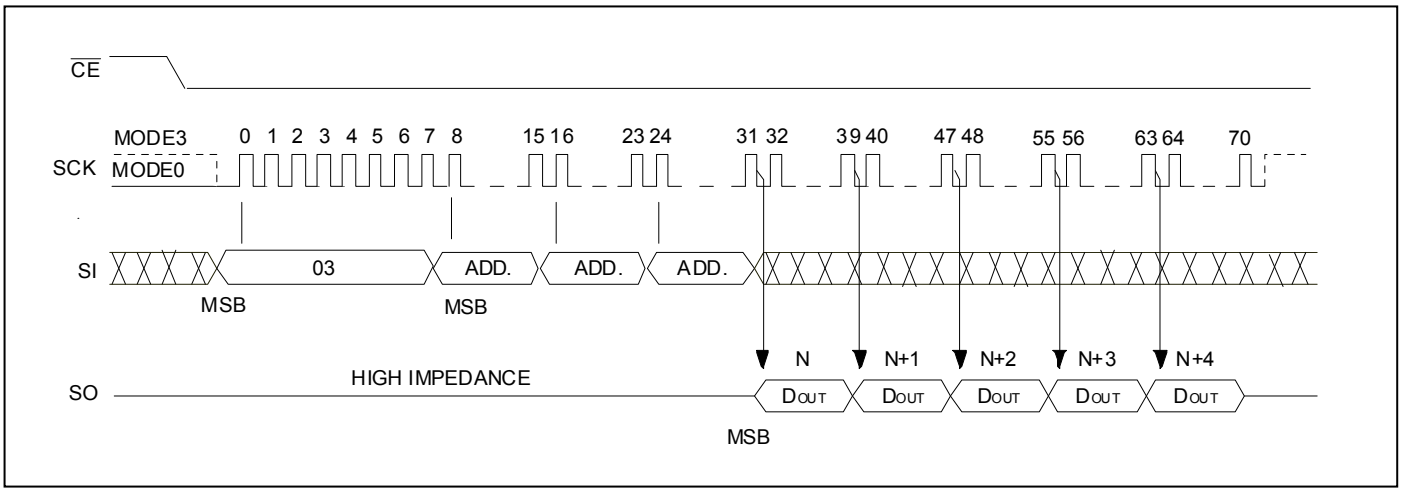


Figure 7: Read Sequence

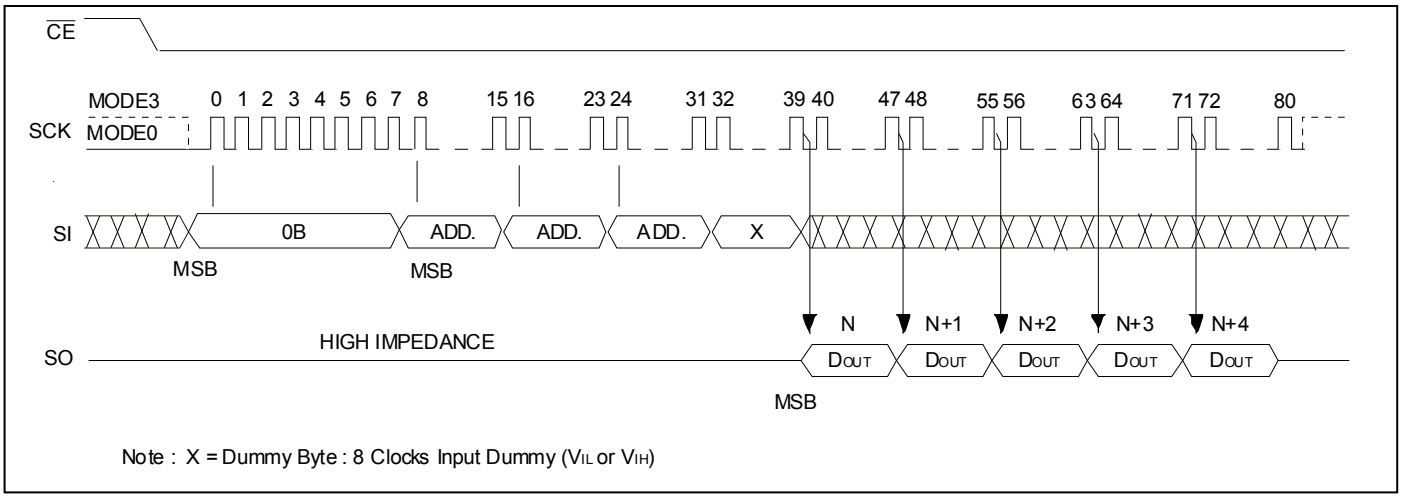


Figure 8-1: Fast Read Sequence (SPI Mode)

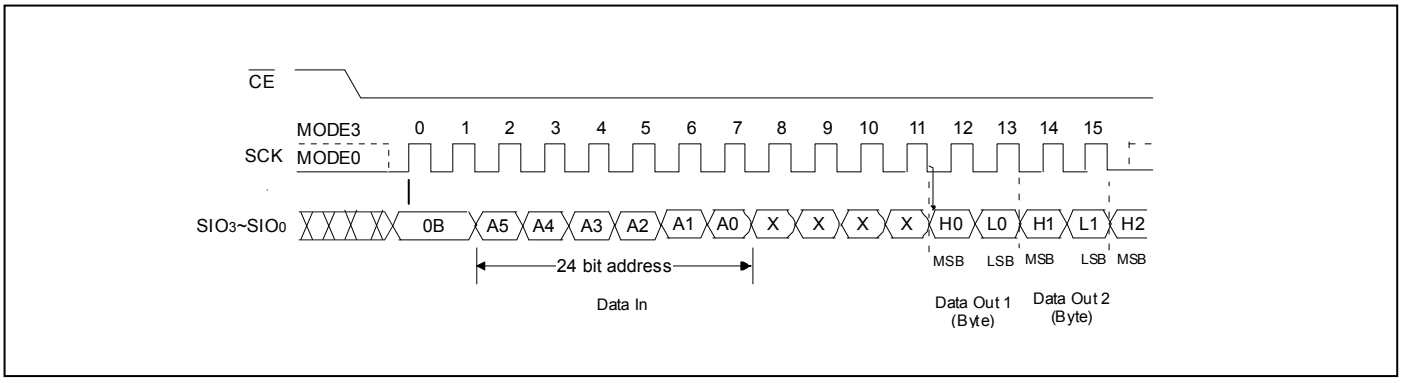


Figure 8-2: Fast Read Sequence (QPI Mode)

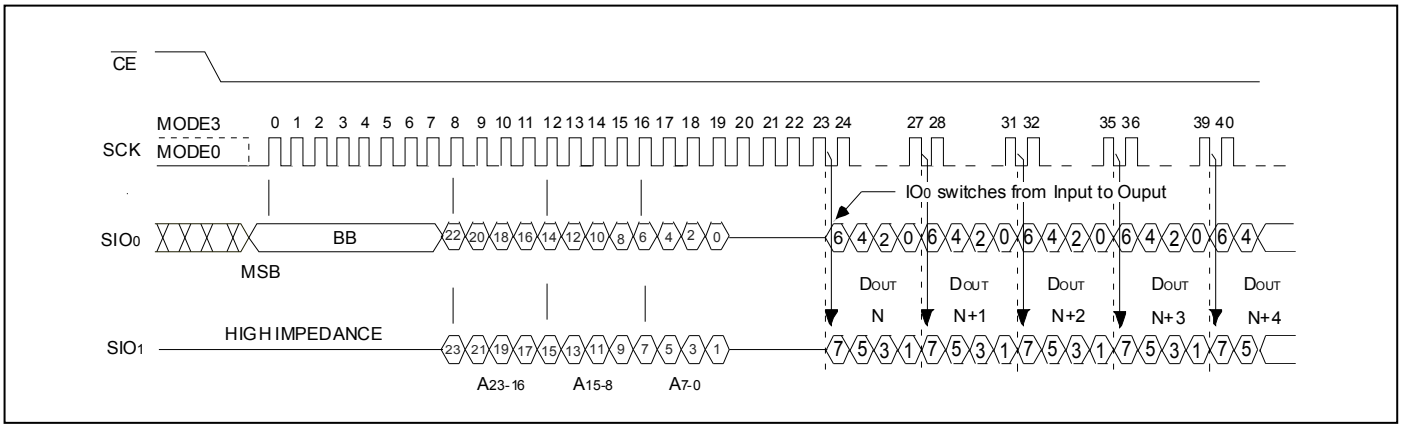


Figure 9: Fast Read Dual I/O (2READ) Sequence

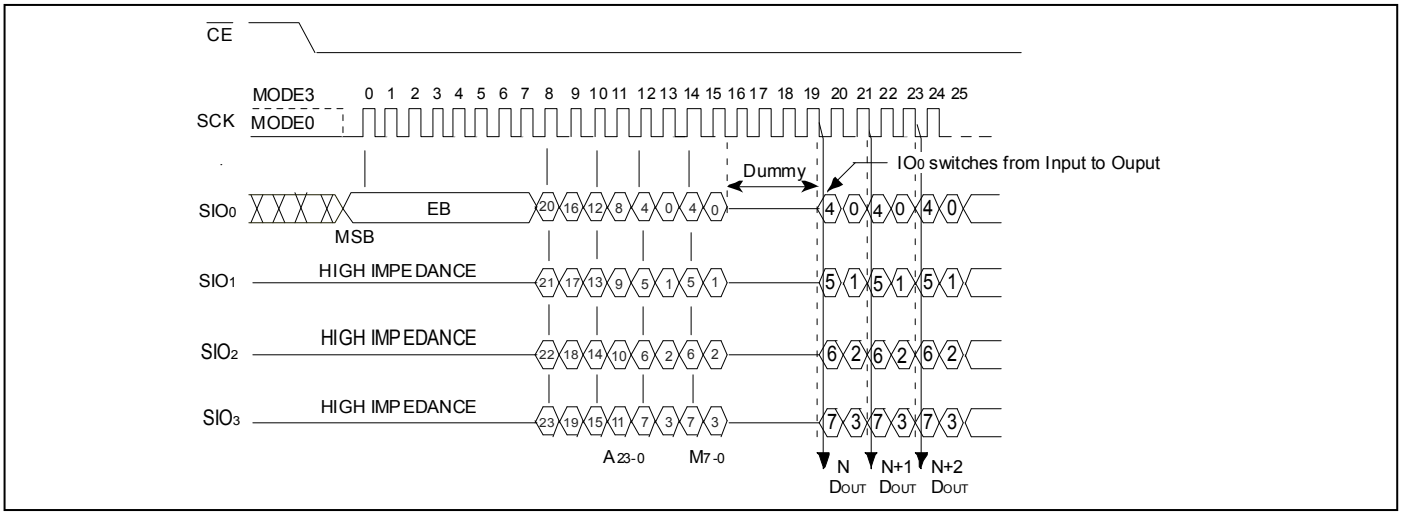


Figure 10-1: Fast Read Quad I/O (4READ) Sequence (SPI Mode)

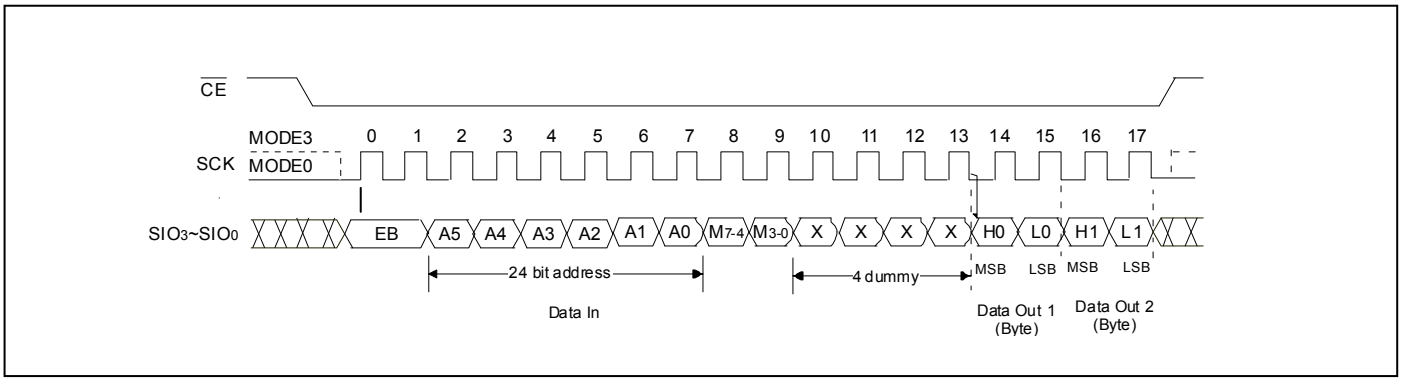


Figure 10-2: Fast Read Quad I/O (4READ) Sequence (QPI Mode)

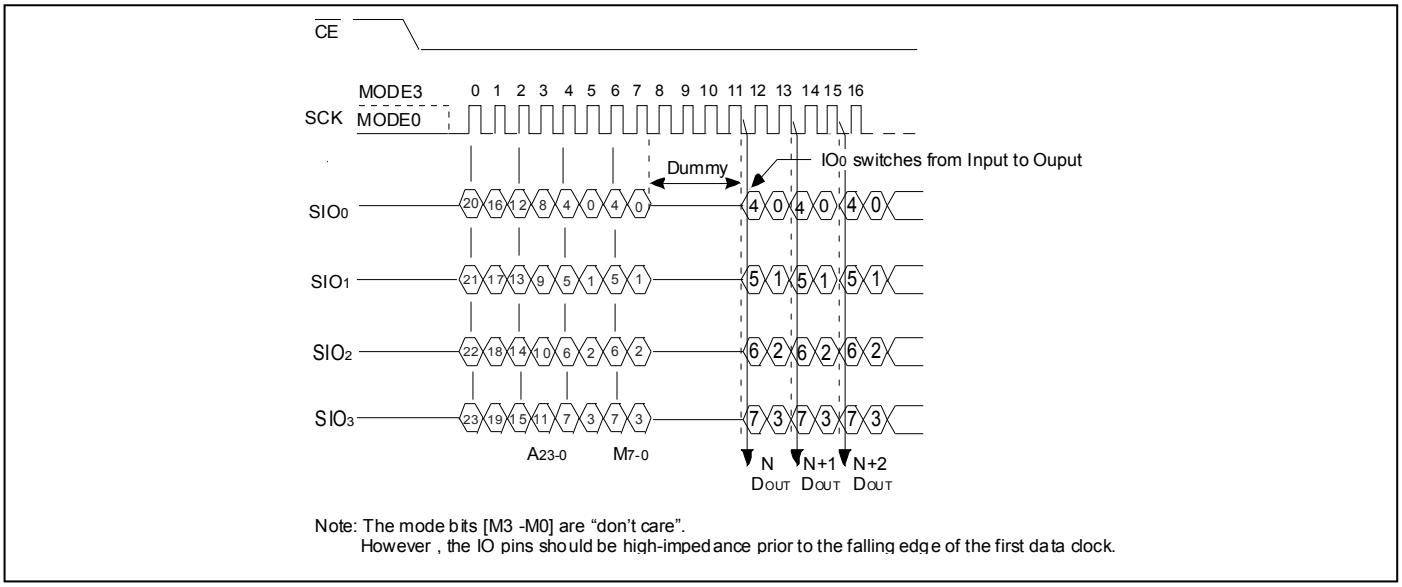


Figure 11-1: Fast Read Quad I/O (4READ) enhance performance Sequence (SPI Mode)

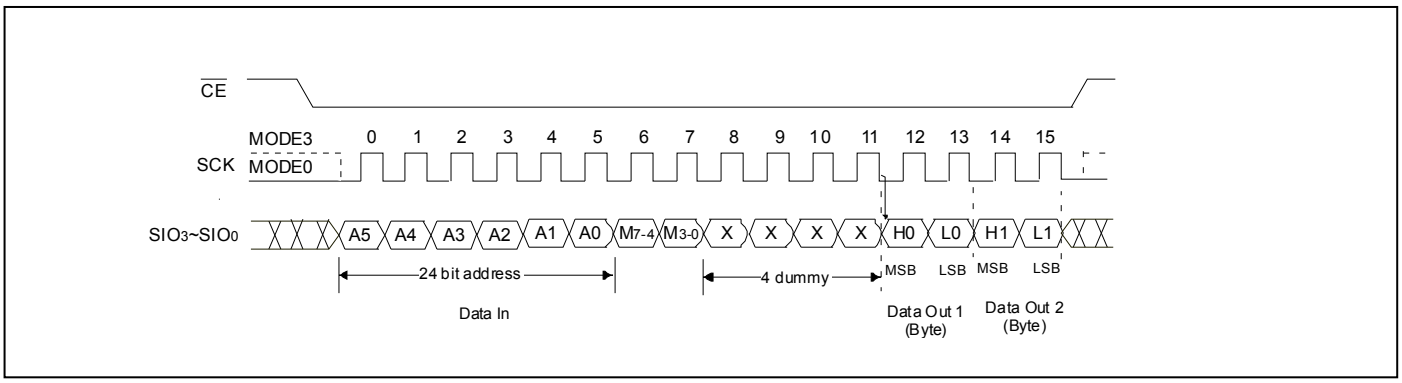


Figure 11-2: Fast Read Quad I/O (4READ) enhance performance Sequence (QPI Mode)

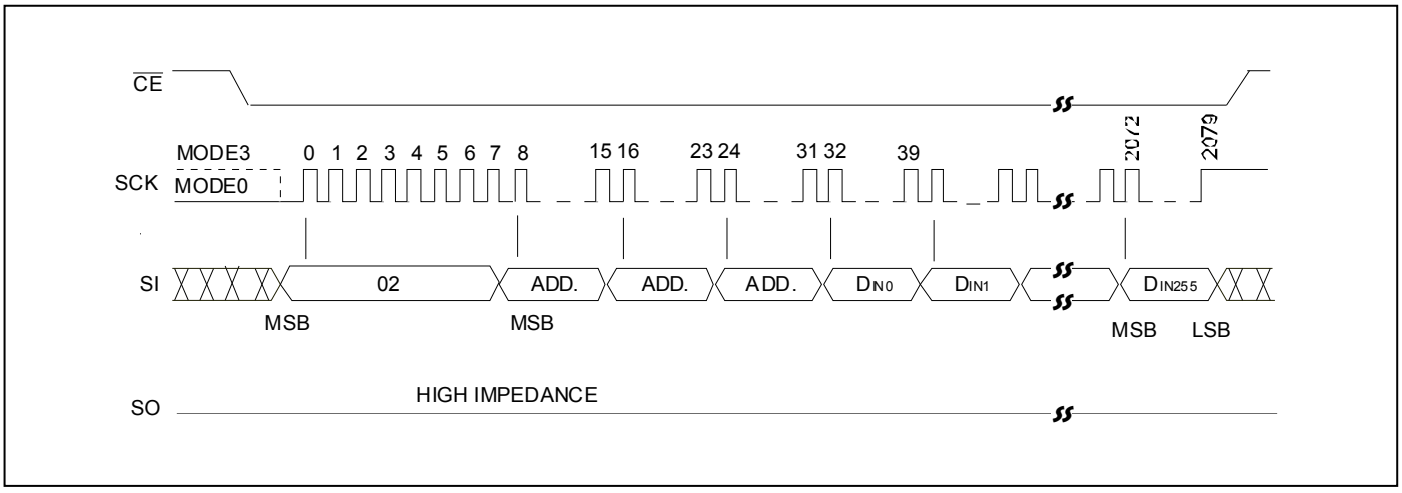


Figure 12-1: Page Program (PP) Sequence (SPI Mode)

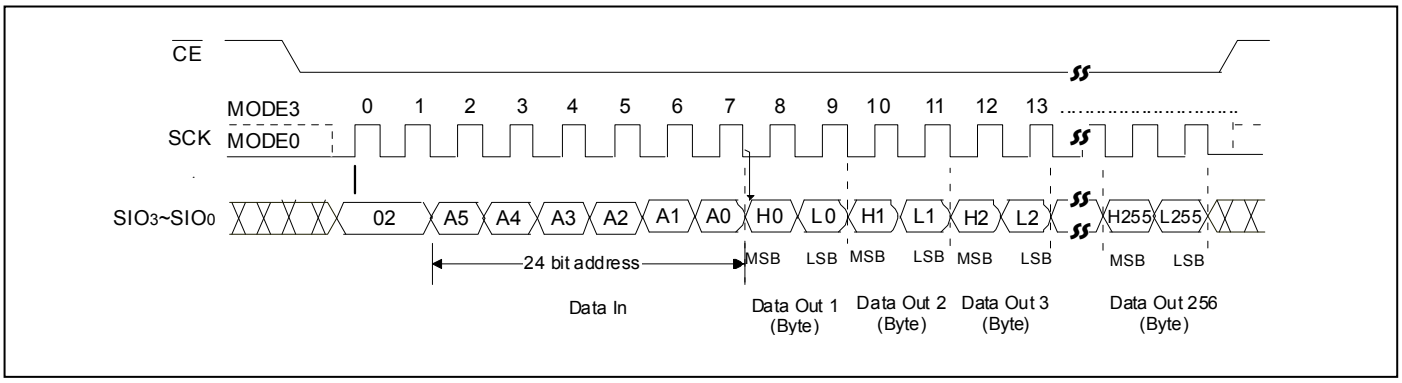


Figure 12-2: Page Program (PP) Sequence (QPI Mode)

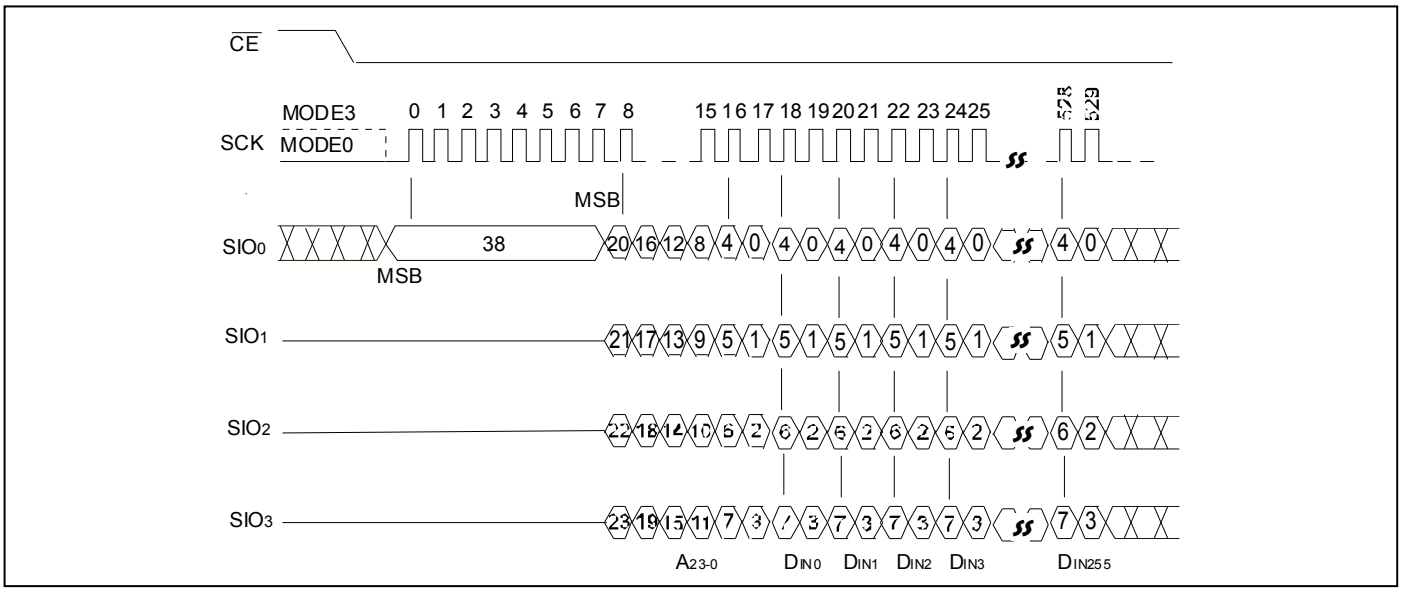


Figure 13: Quad Page Program (4PP) Sequence

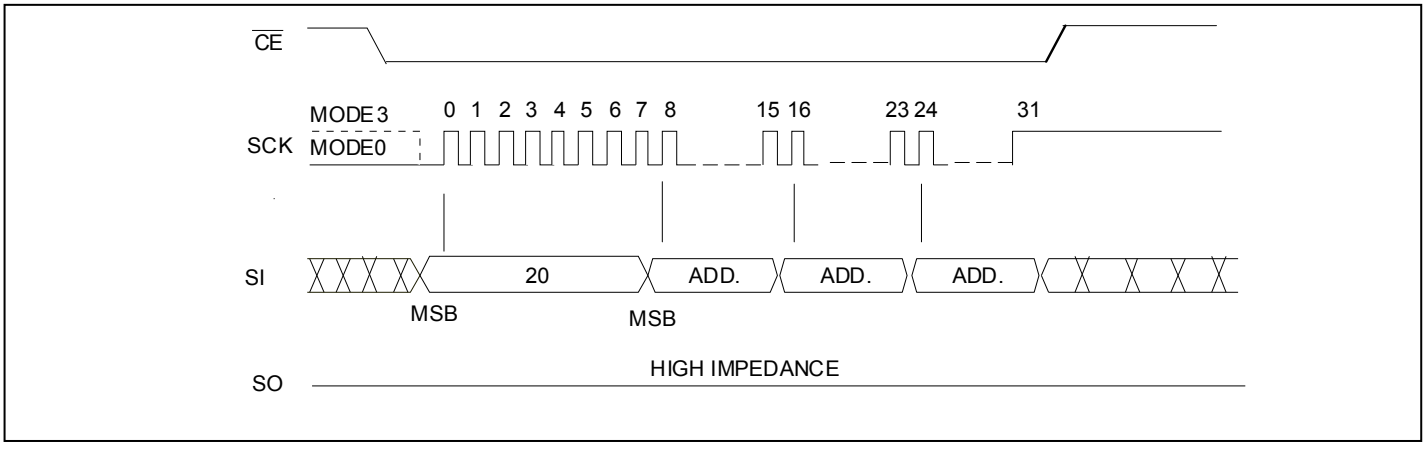


Figure 14-1: Sector Erase (SE) Sequence (SPI Mode)

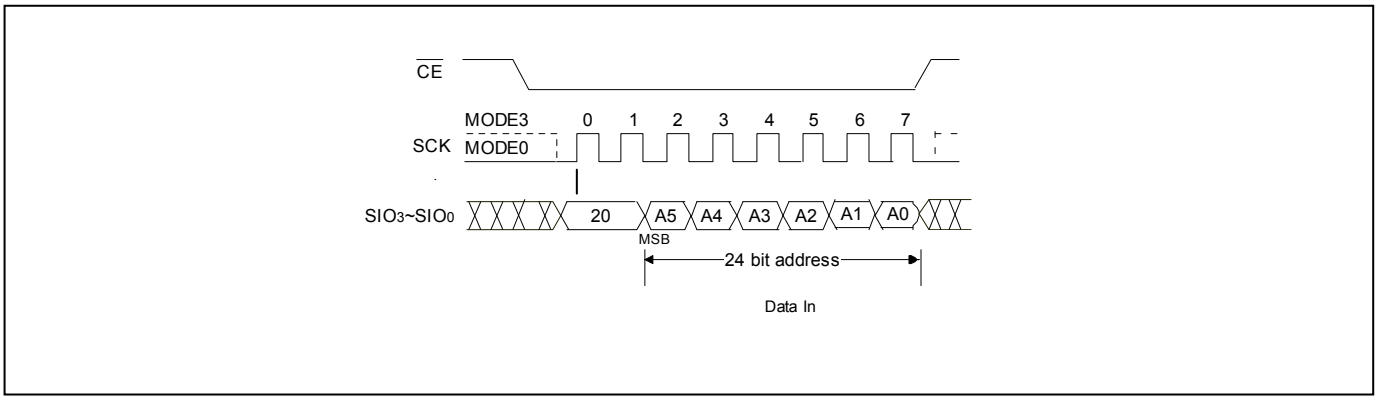


Figure 14-2: Sector Erase (SE) Sequence (QPI Mode)

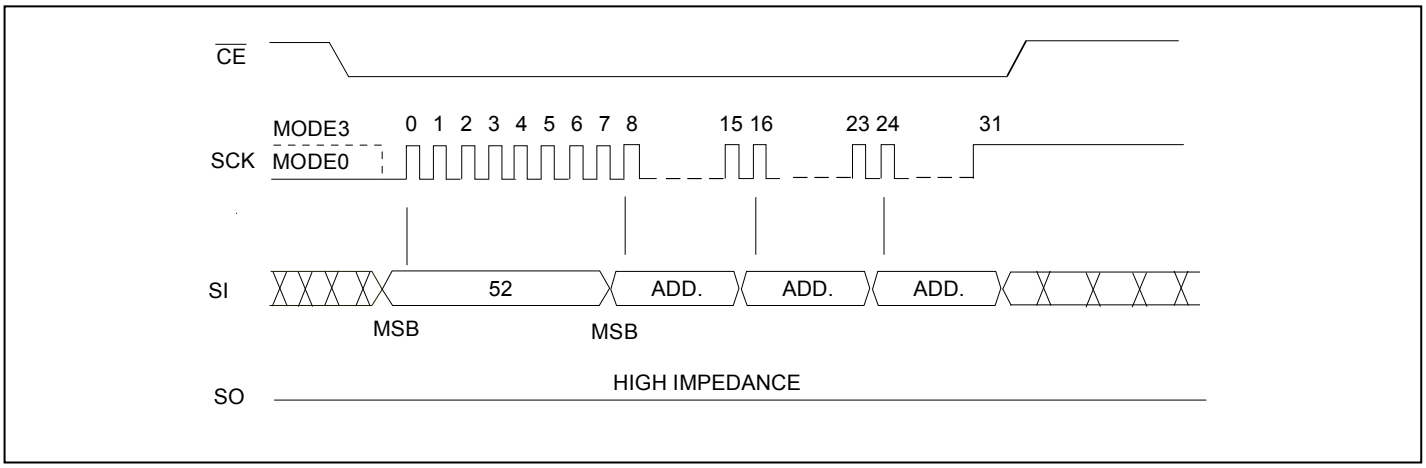


Figure 15-1: 32K-byte Block Erase (BE32K) Sequence (SPI Mode)

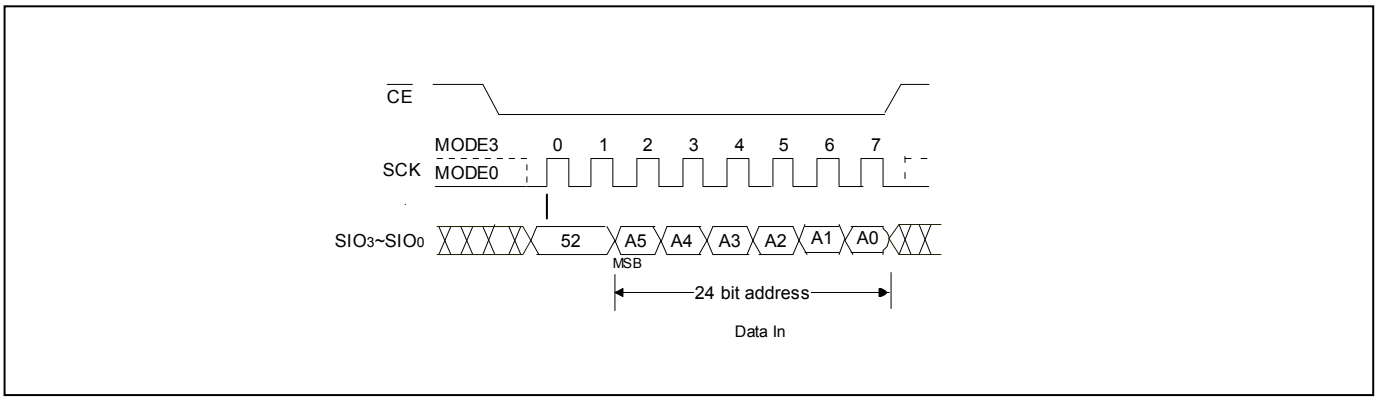


Figure 15-2: 32K-byte Block Erase (BE32K) Sequence (QPI Mode)

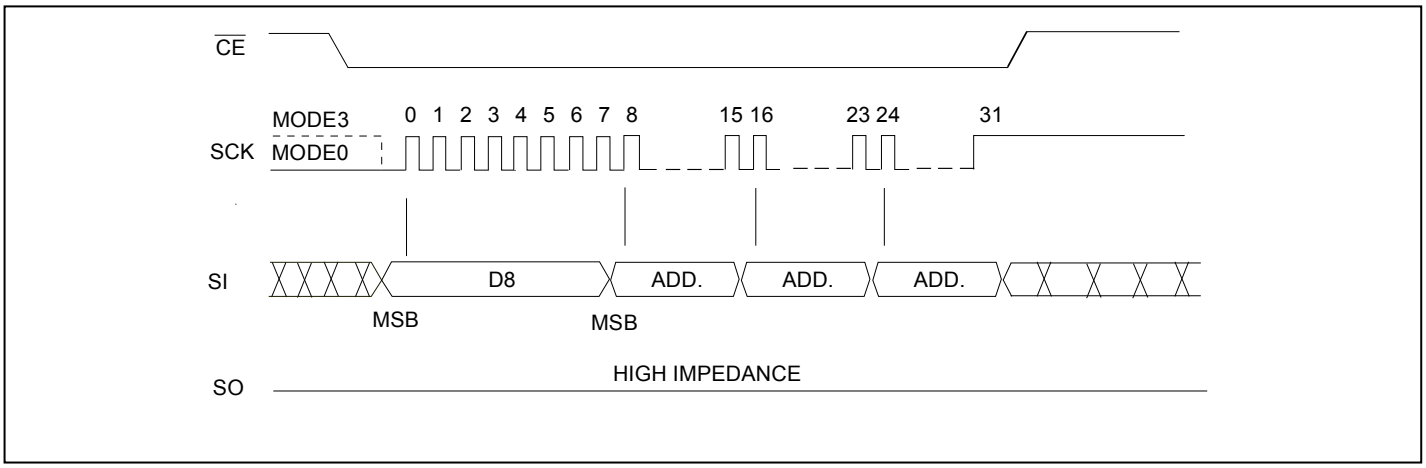


Figure 16-1: 64K-byte Block Erase (BE) Sequence (SPI Mode)

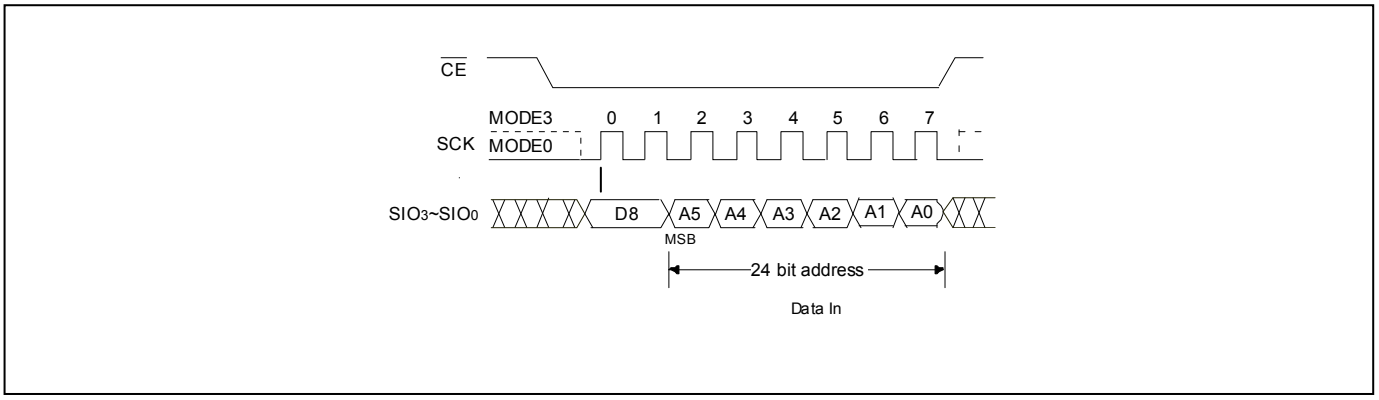


Figure 16-2: 64K-byte Block Erase (BE) Sequence (QPI Mode)

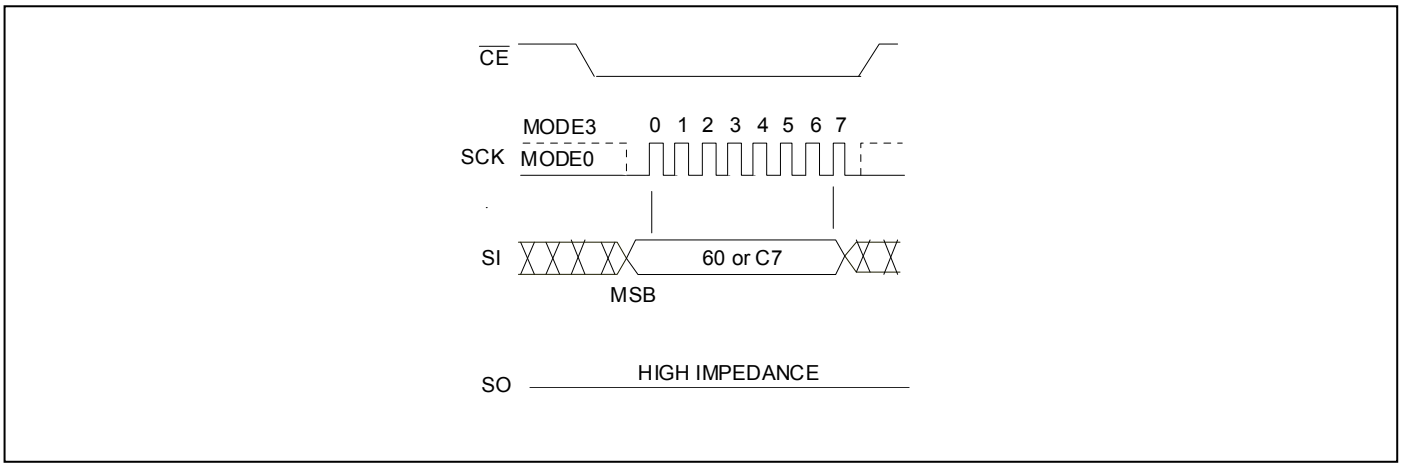


Figure 17-1: Chip Erase (CE) Sequence (SPI Mode)

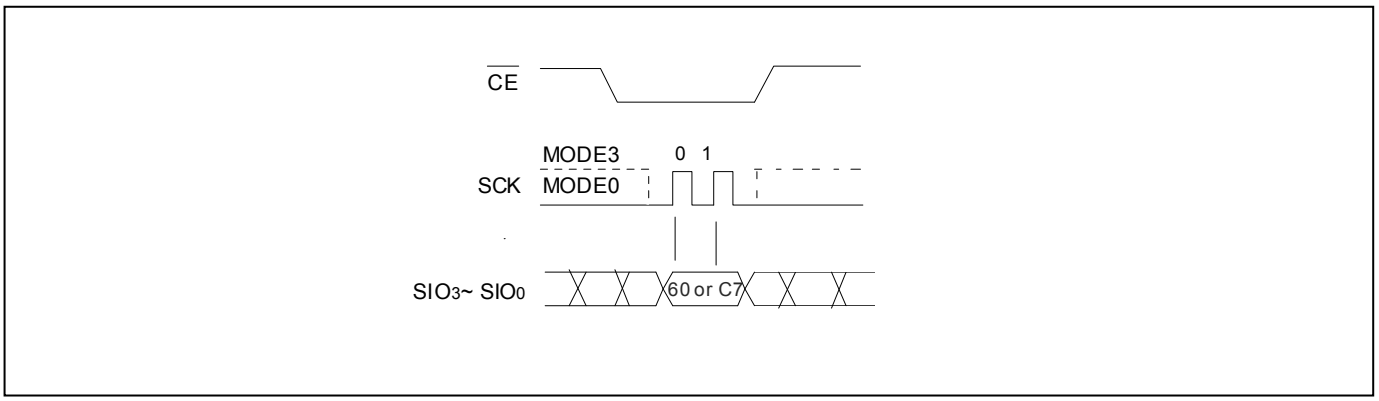


Figure 17-2: Chip Erase (CE) Sequence (QPI Mode)

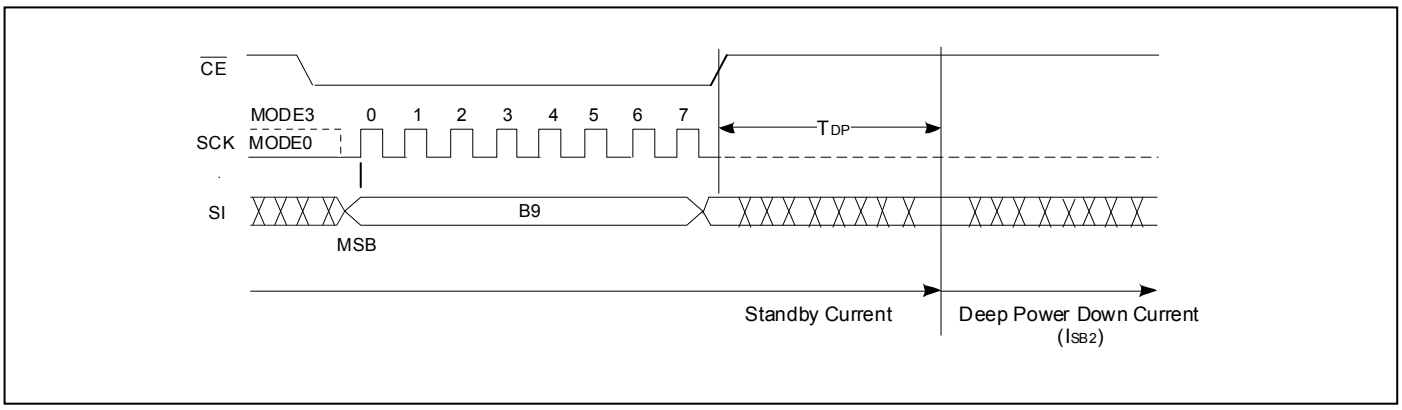


Figure 18-1: Deep Power-down (DP) Instruction (SPI Mode)

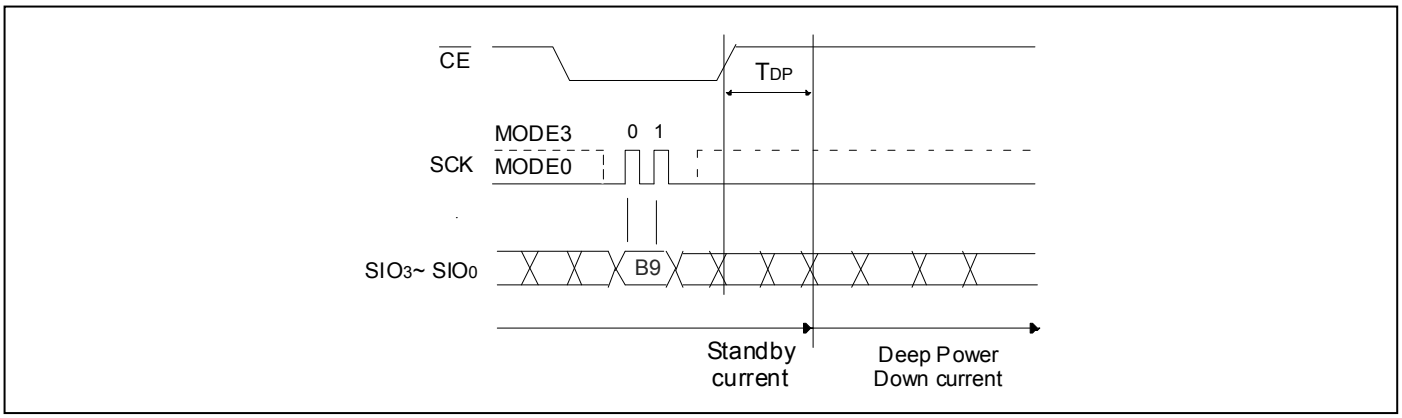


Figure 18-2: Deep Power-down (DP) Instruction (QPI Mode)

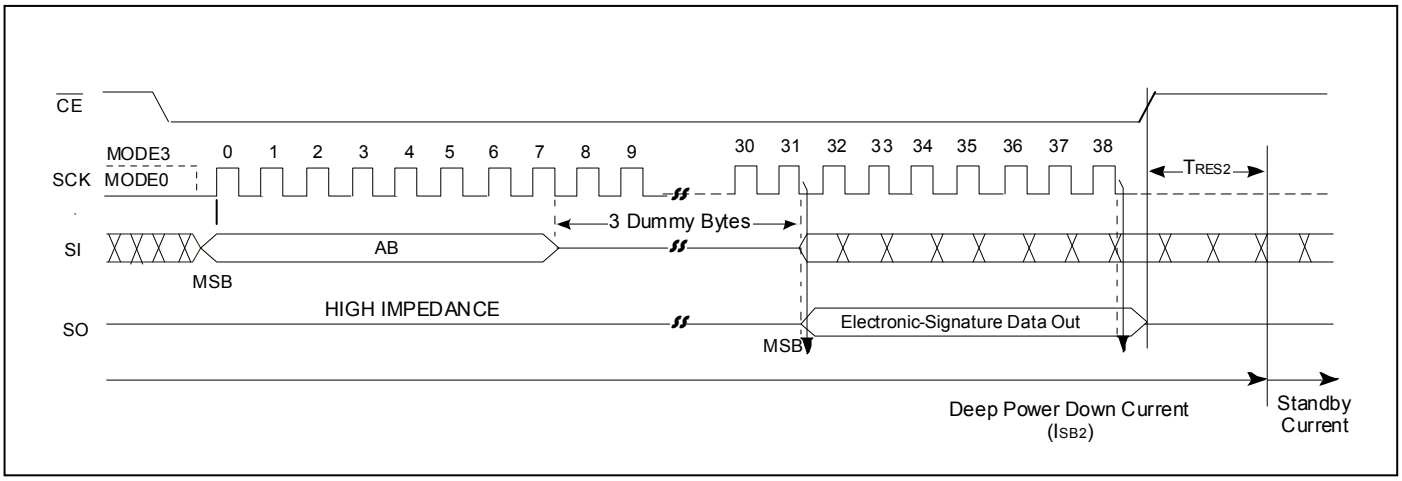


Figure 19-1: Read Electronic Signature (RES) Sequence (SPI Mode)

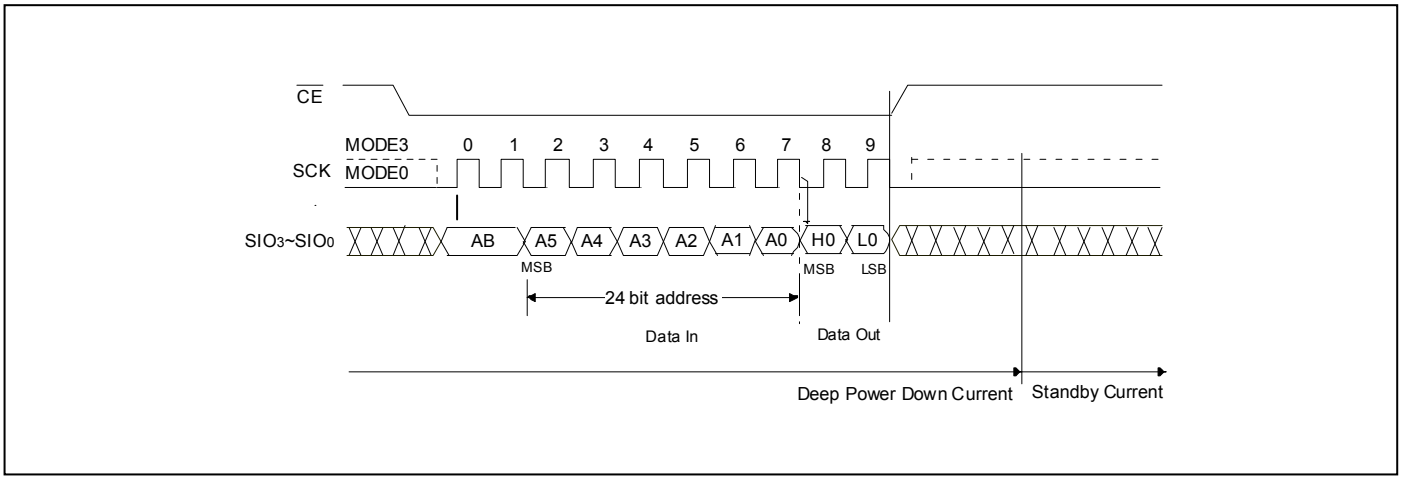


Figure 19-2: Read Electronic Signature (RES) Sequence (QPI Mode)

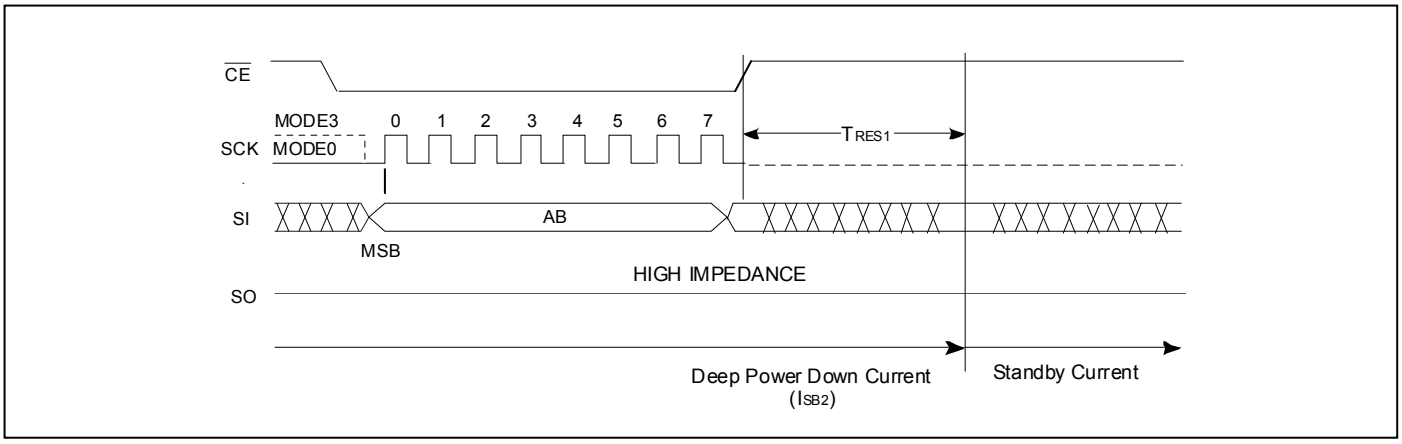


Figure 20-1: Release from Deep Power Down (RDP) Instruction (SPI Mode)

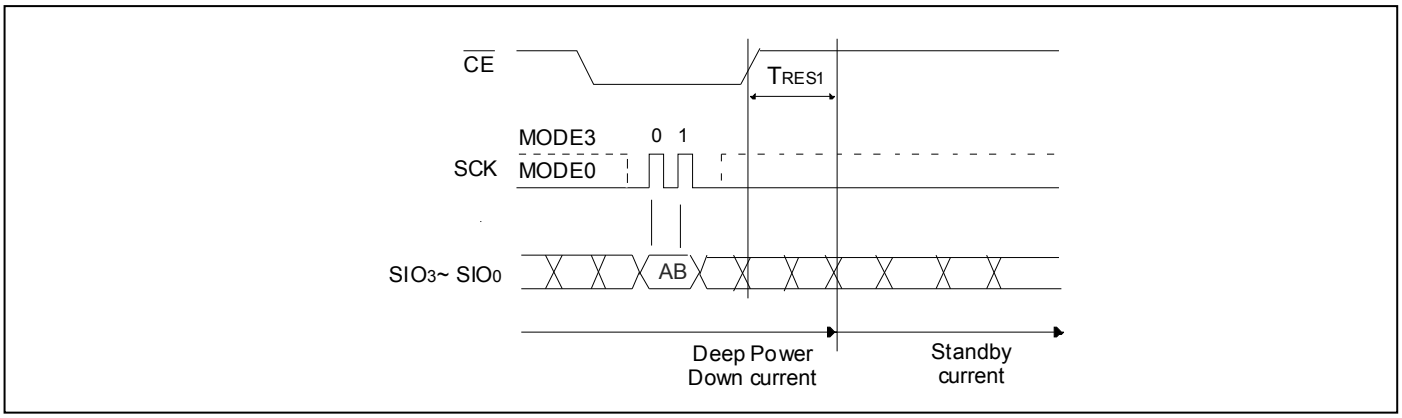
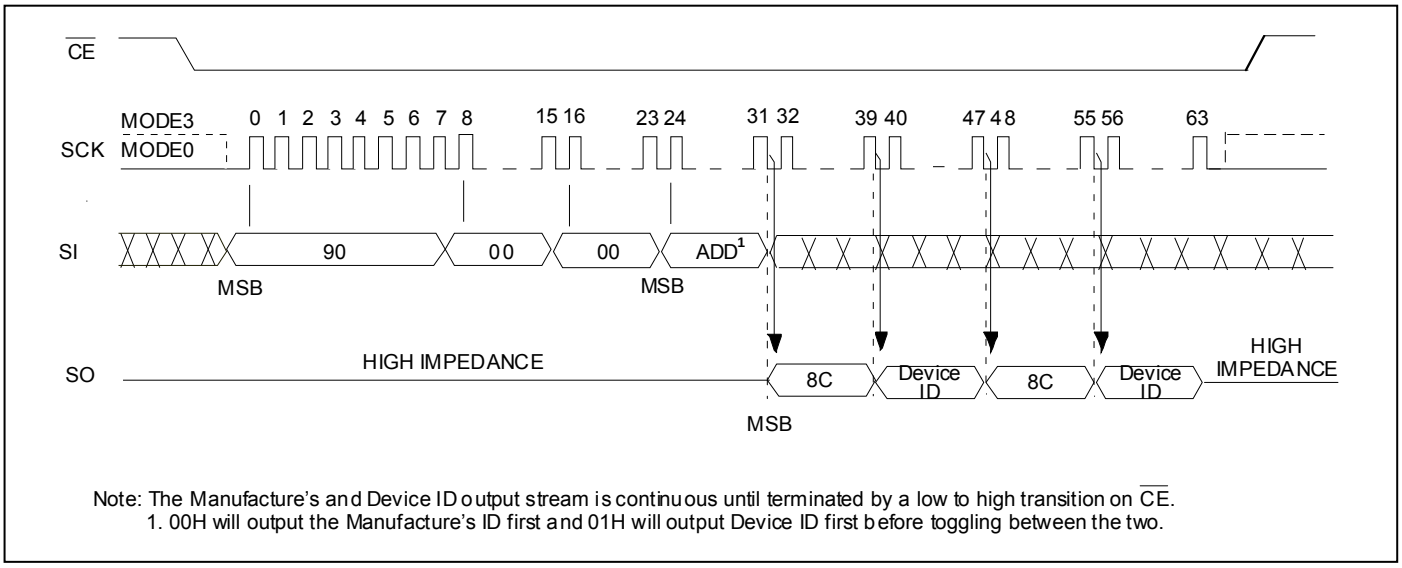


Figure 20-2: Release from Deep Power Down (RDP) Instruction (QPI Mode)



Note: The Manufacture's and Device ID output stream is continuous until terminated by a low to high transition on $\overline{CE}$.
1. 00H will output the Manufacture's ID first and 01H will output Device ID first before toggling between the two.

Figure 21: Read Electronic Manufacture ID and Device ID (REMS) Sequence (SPI Mode)

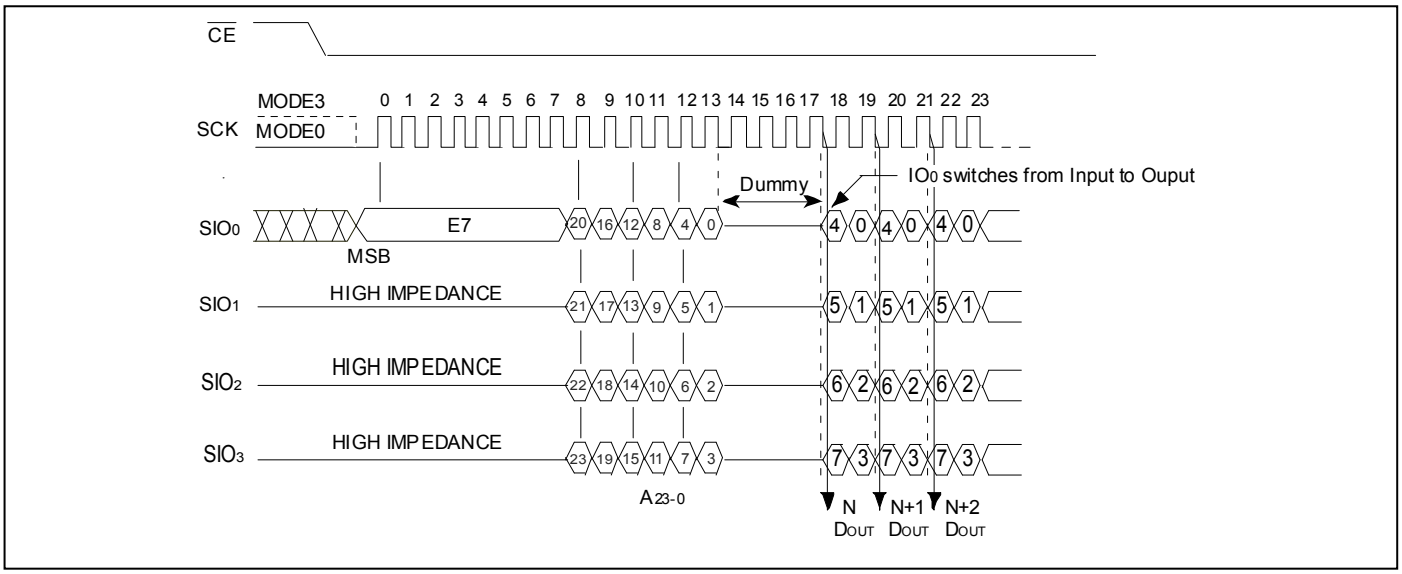


Figure 22: Fast Read Quad I/O (4 dummy cycles) Sequence (SPI Mode)

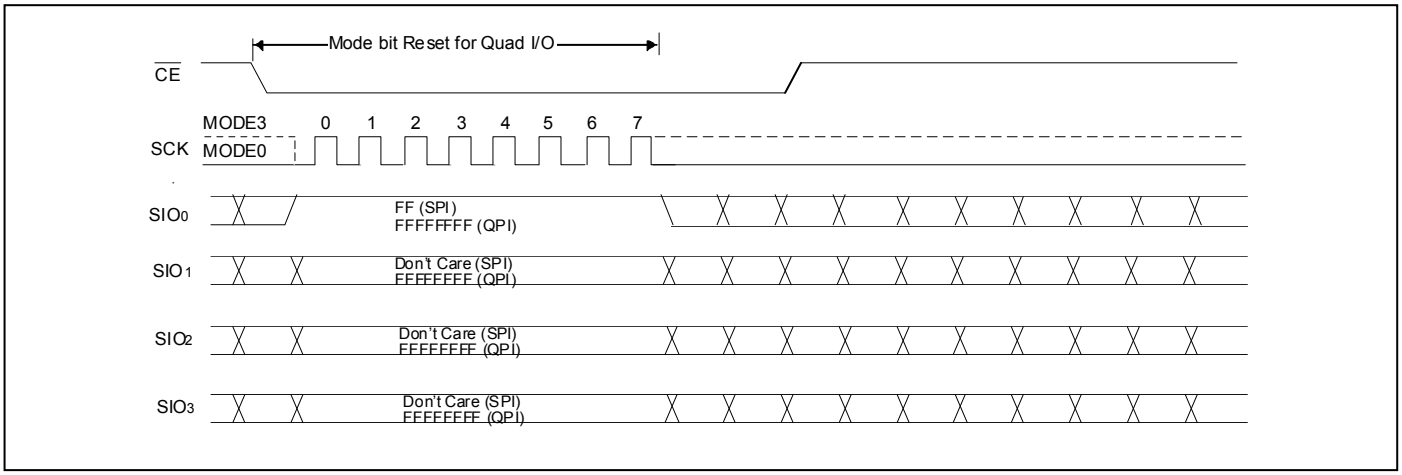


Figure 23: Mode Bit Reset Sequence (SPI and QPI Mode)

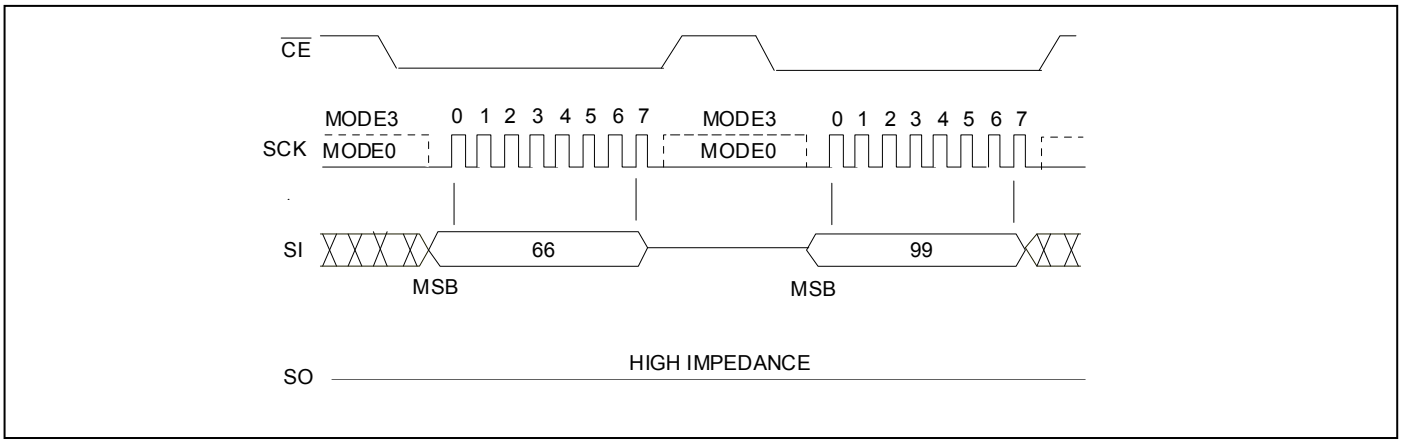


Figure 24-1: Reset Sequence (SPI Mode)

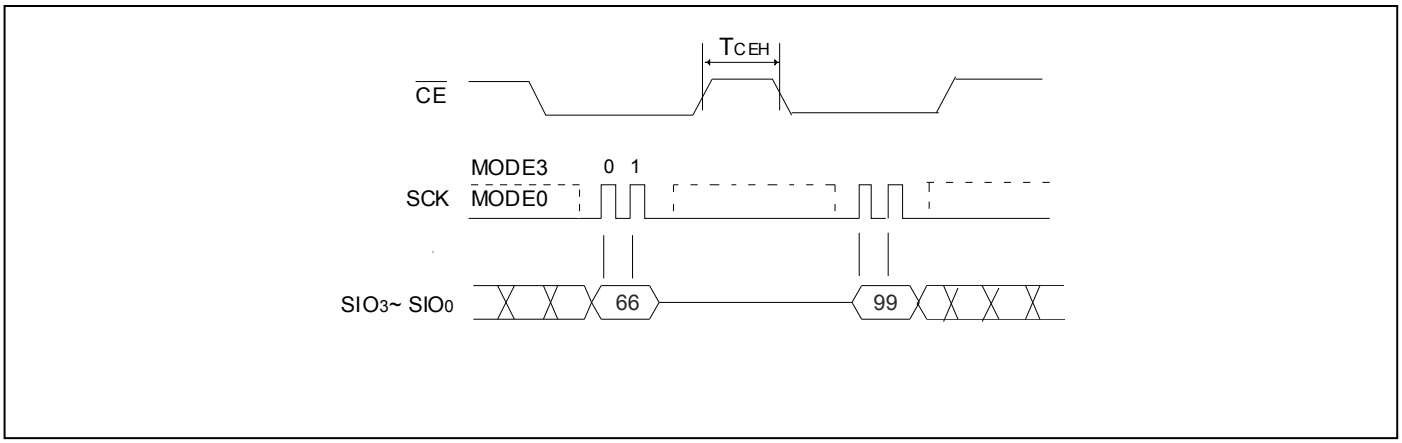


Figure 24-2: Reset Sequence (QPI Mode)

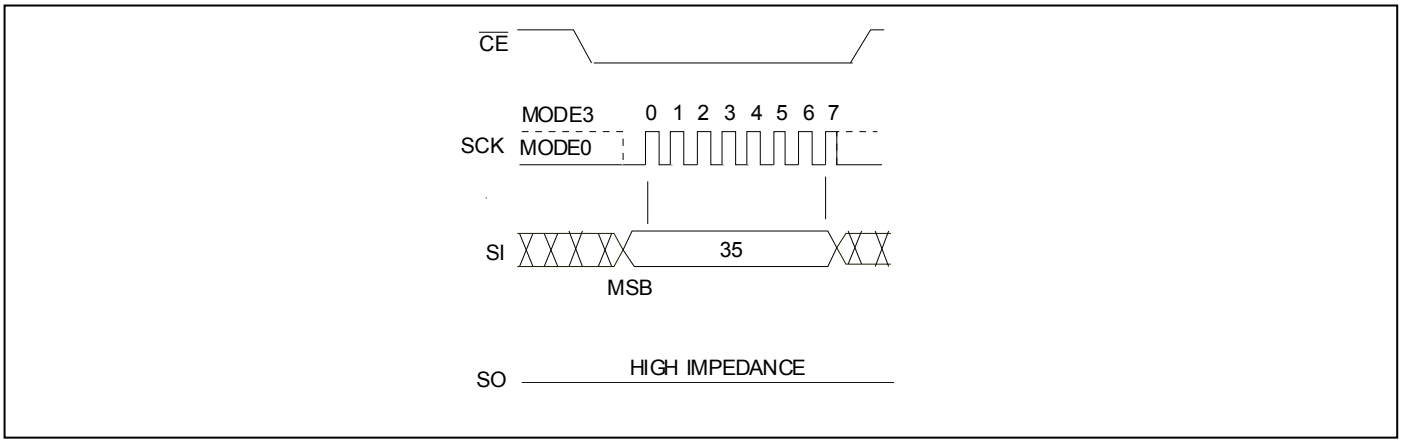


Figure 25: Enable Quad I/O (EQIQ) Sequence

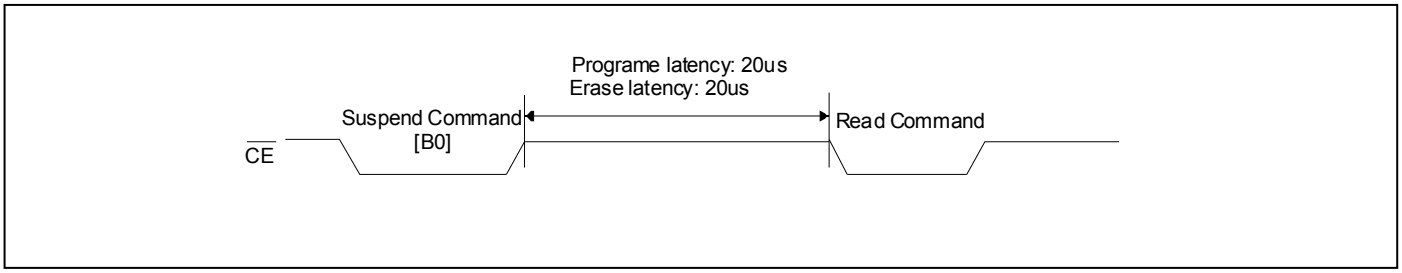


Figure 26-1: Suspend to Read Latency

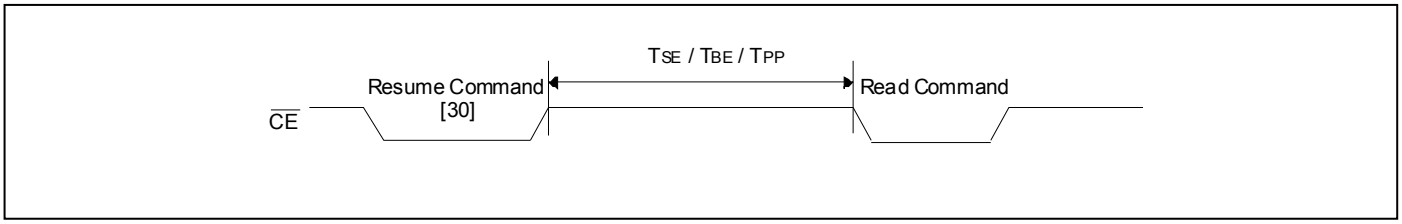


Figure 26-2: Resume to Read Latency

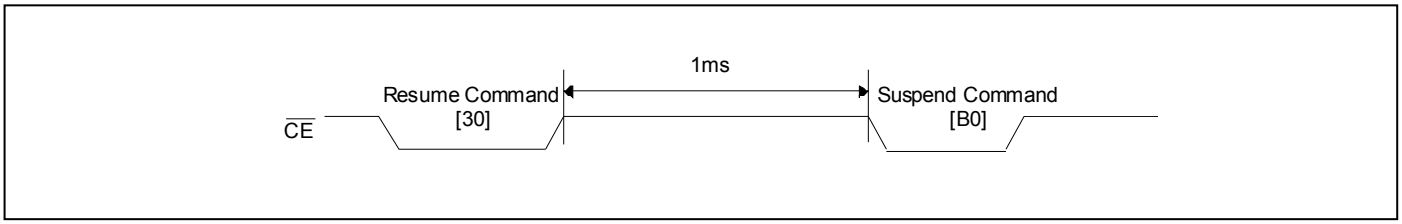


Figure 26-3: Resume to Suspend Latency

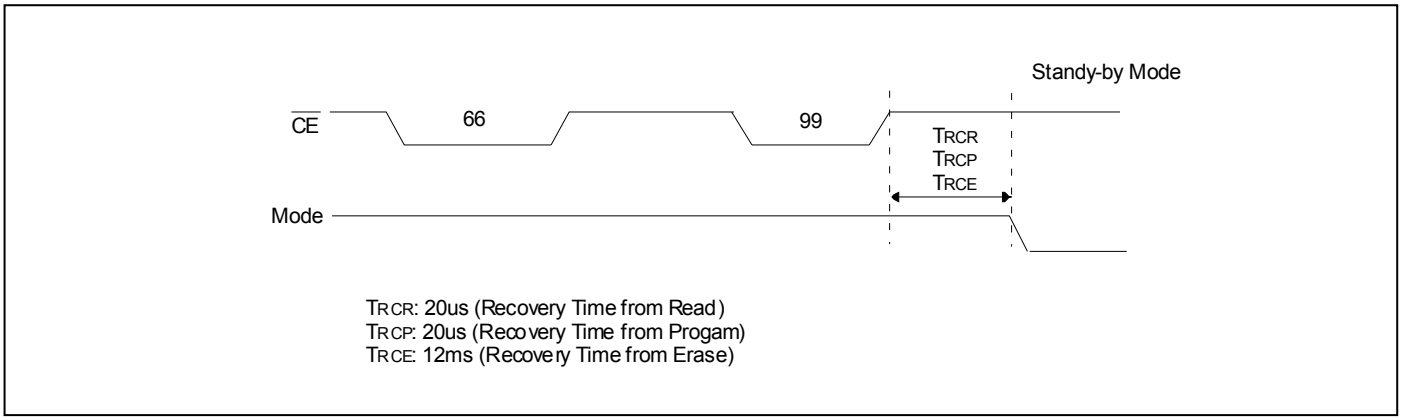


Figure 27: Software Reset Recovery

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings

(Applied conditions are greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -0.5V to VDD+1.0V

TABLE 12: AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . C_L = 15 pF for ≧75MHz
. . . . . .C_L = 30 pF for ≦50MHz
See Figures 33 and 34

TABLE 13: OPERATING RANGE

Parameter	Symbol	Value	Unit
Operating Supply Voltage	V_{DD}	1.65~2	V
Ambient Operating Temperature	T_A	-40 ~ +85	℃

TABLE 14: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Test Condition
		Min	Max	Unit	
I_{DDR1}	Read Current @ 84MHz		15	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}, SO=open
I_{DDR2}	Read Current @ 104MHz		20	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}, SO=open
I_{DDW}	Program and Write Status Register Current		20	mA	$\overline{CE}$ =V_{DD}
I_{DDE}	Sector and Block Erase Current		20	mA	$\overline{CE}$ =V_{DD}
	Chip Erase Current		20	mA	$\overline{CE}$ =V_{DD}
I_{SB1}	Standby Current	30	100	µA	$\overline{CE}$ =V_{DD}, V_{IN} =V_{DD} or V_{SS}
I_{SB2}	Deep Power Down Current		5	µA	$\overline{CE}$ =V_{DD}, V_{IN} =V_{DD} or V_{SS}
I_{LI}	Input Leakage Current		±2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		±2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	-0.5	0.2 x V_{DD}	V	
V_{IH}	Input High Voltage	0.8 x V_{DD}	V_{DD} +0.4	V	
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100uA
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA

TABLE 15: LATCH UP CHARACTERISTIC

Symbol	Parameter	Minimum	Unit	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 16: CAPACITANCE (T_A = 25℃, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 17: AC OPERATING CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
F_{SCLK}	Serial Clock Frequency for FAST_READ, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR instruction				104	MHz
F_{RSCLK}	Serial Clock Frequency for READ instruction				33	MHz
F_{TSCLK1}	Serial Clock Frequency for 2READ instruction				84	MHz
F_{TSCLK2}[5]	Serial Clock Frequency for 4READ instruction				84/ 104	MHz
T_{SCKH}	Serial Clock High Time	Serial (F_{SCLK})	4.5			ns
		4PP and Normal Read (F_{RSCLK})	15			ns
T_{SCKL}	Serial Clock Low Time	Serial (F_{SCLK})	4.5			ns
		4PP and Normal Read (F_{RSCLK})	15			ns
T_{CLCH}[2]	Clock Rise Time (peak to peak)		0.1			V/ns
T_{CHCL}[2]	Clock Fall Time (peak to peak)		0.1			V/ns
T_{CES}[1]	$\overline{CE}$ Active Setup Time		5			ns
T_{CEH}[1]	$\overline{CE}$ Active Hold Time		5			ns
T_{CHS}[1]	$\overline{CE}$ Not Active Setup Time		5			ns
T_{CHH}[1]	$\overline{CE}$ Not Active Hold Time		5			ns
T_{CPH}	$\overline{CE}$ High Time	Read	12			ns
		Write / Erase / Program	30			ns
T_{CHZ}	$\overline{CE}$ High to High-Z Output				8	ns
T_{CLZ}	SCK Low to Low-Z Output		0			ns
T_{DS}	Data In Setup Time		2			ns
T_{DH}	Data In Hold Time		5			ns
T_{HLS}	$\overline{HOLD}$ Low Setup Time		5			ns
T_{HHS}	$\overline{HOLD}$ High Setup Time		5			ns

TABLE 17: AC OPERATING CHARACTERISTICS - Continued

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_{HLH}	$\overline{HOLD}$ Low Hold Time		5			ns
T_{HHH}	$\overline{HOLD}$ High Hold Time		5			ns
T_{HZ}[3]	$\overline{HOLD}$ Low to High-Z Output				8	ns
T_{LZ}[3]	$\overline{HOLD}$ High to Low-Z Output				8	ns
T_{OH}	Output Hold from SCK Change		0			ns
T_V	Output Valid from SCK	Loading: 30pF			8	ns
		Loading: 15pF			6	ns
T_{WHSL}[4]	Write Protect Setup Time before $\overline{CE}$ Low				20	ns
T_{SHWL}[4]	Write Protect Hold Time after $\overline{CE}$ High				100	ns
T_{DP}[3]	$\overline{CE}$ High to Deep Power Down Mode				10	us
T_{RES1}[3]	$\overline{CE}$ High to Standby Mode (for DP)				10	us
T_{RES2}[3]	$\overline{CE}$ High to Standby Mode (for RES)				10	us
T_{SUS}[3]	$\overline{CE}$ High to next Instruction after Suspend				20	us
T_{RCR}	Recovery time to read				20	us
T_{RCP}	Recovery time to program				20	ms
T_{RCE}	Recovery time to erase				12	ms

Note:

1. Relative to SCK.
2. $T_{SCKH} + T_{SCKL}$ must be less than or equal to 1/ F_{CLK}.
3. Value guaranteed by characterization, not 100% tested in production.
4. Only applicable as a constraint for a Write Status Register instruction when Block- Protection-Look (BPL) bit is set at 1.
5. When dummy cycle = 4, clock rate = 84 MHz; when dummy cycle = 6, clock rate = 104 MHz

■ **TABLE 18: ERASE AND PROGRAMMING PERFORMANCE**

Parameter	Symbol	Limit		Unit
		Typ[2]	Max[3]	
Sector Erase Time (4KB)	T_{SE}	60	200	ms
Block Erase Time (32KB)	T_{BE1}	250	1000	ms
Block Erase Time (64KB)	T_{BE2}	0.5	1	s
Chip Erase Time	T_{CE}	3	5	s
Write Status Register Time	T_W		40	ms
Page Programming Time	T_{PP}	0.7	1	ms
Erase/Program Cycles[1]		100,000	-	Cycles
Data Retention		20	-	Years

Notes:
1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 1.8V.
3. Maximum values measured at 85°C, 1.65V.

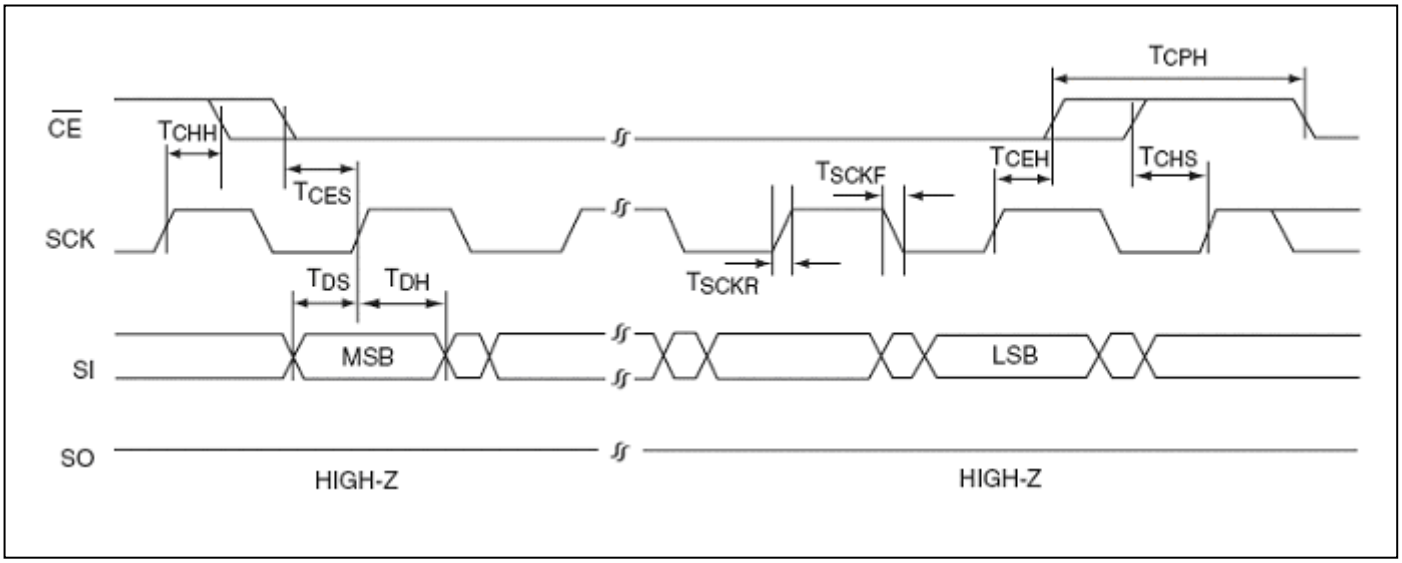


Figure 28: Serial Input Timing Diagram

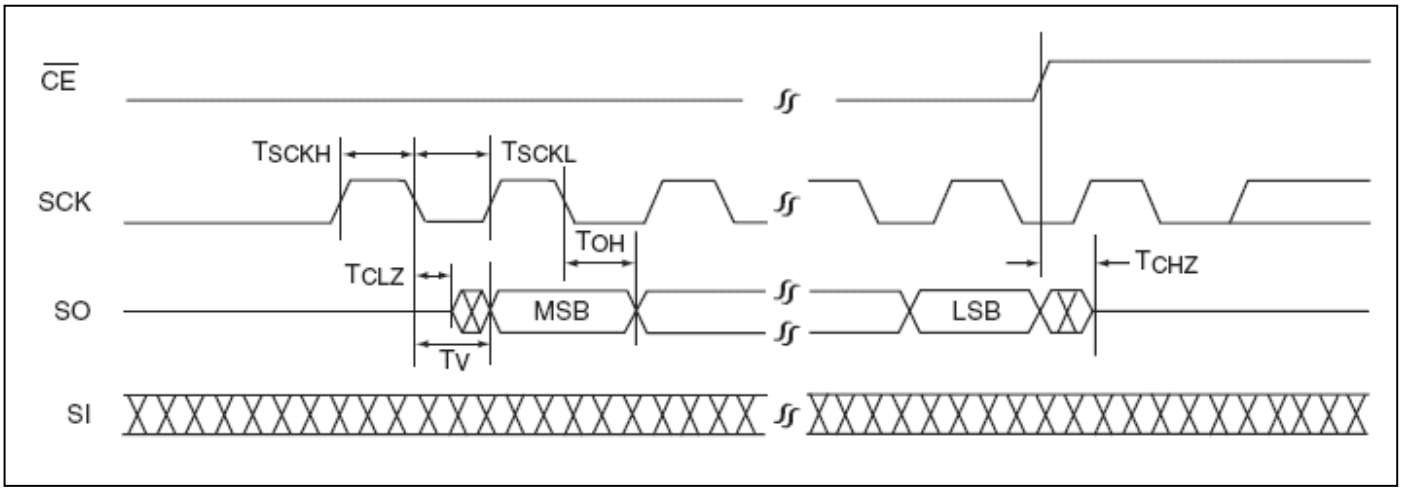


Figure 29: Serial Output Timing Diagram

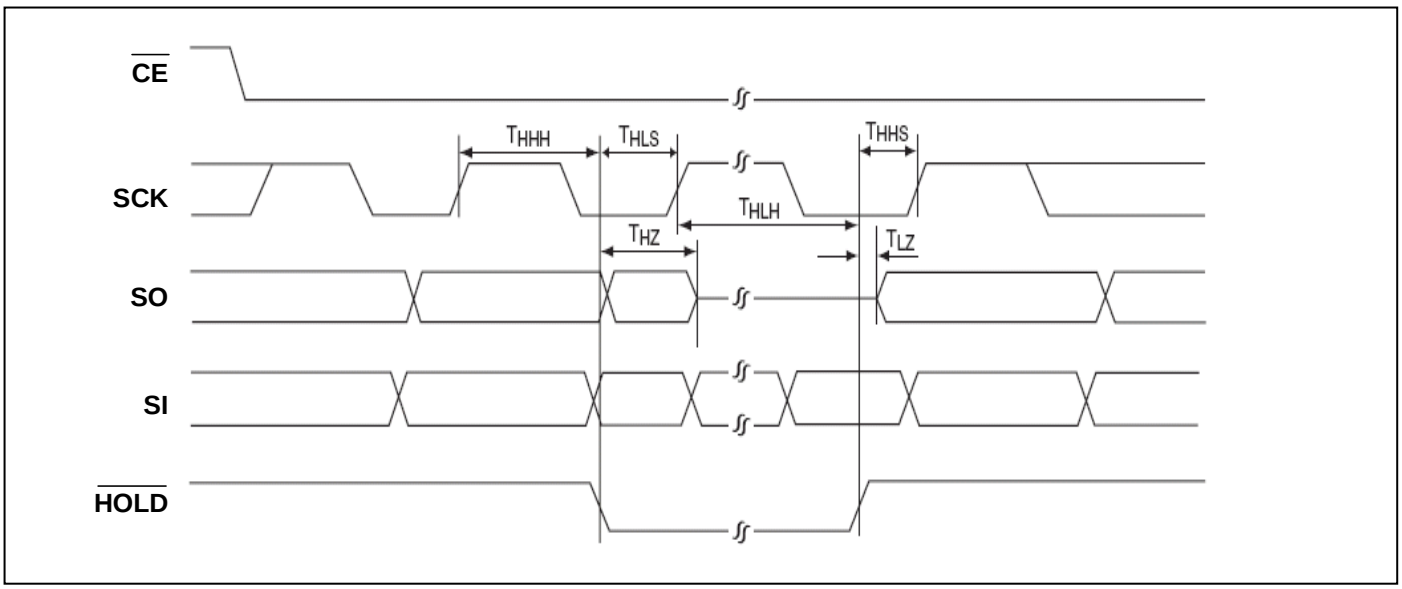


Figure 30: HOLD Timing Diagram

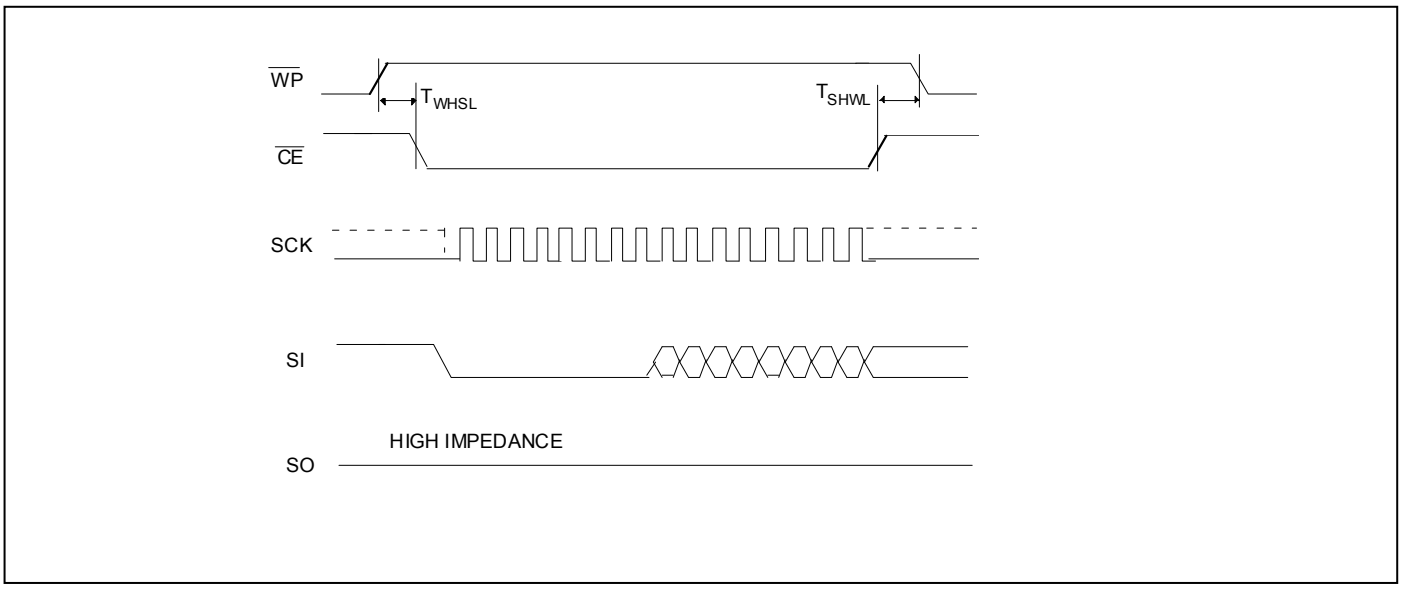


Figure 31: Write Protect setup and hold timing during WRSR when BPL = 1

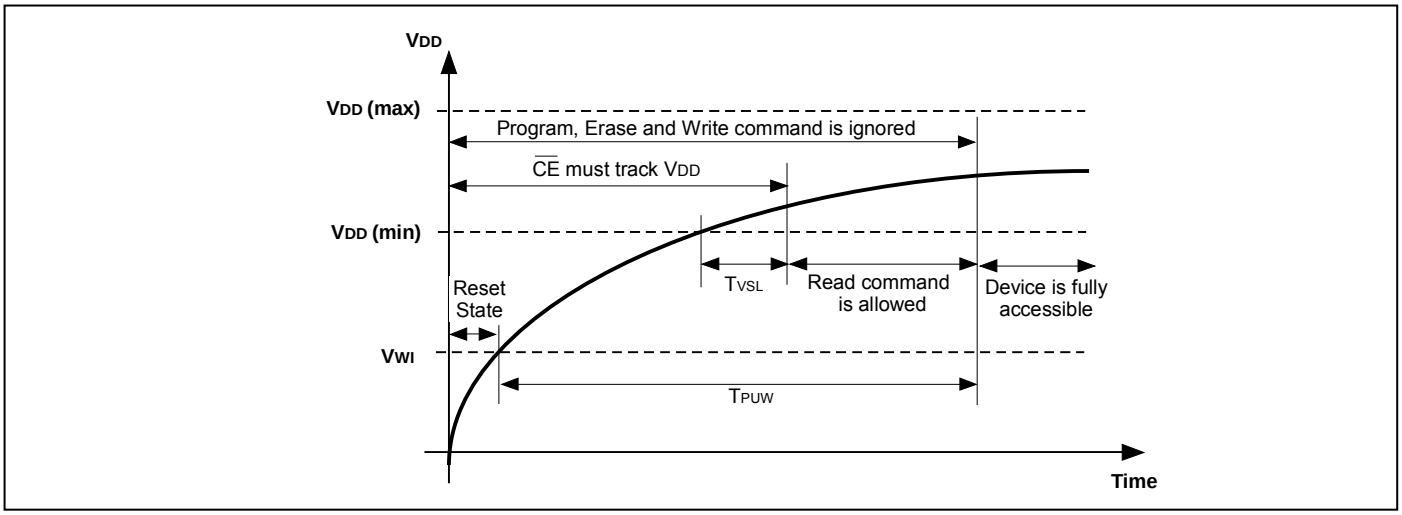


Figure 32: Power-Up Timing Diagram

Table 19: Power-Up Timing and V_{WI} Threshold

Parameter	Symbol	Min.	Max.	Unit
V_{DD}(min) to $\overline{CE}$ low	T_{VSL}	300		us
Time Delay before Write instruction	T_{PUW}	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}	1	1.4	V

Note: These parameters are characterized only.

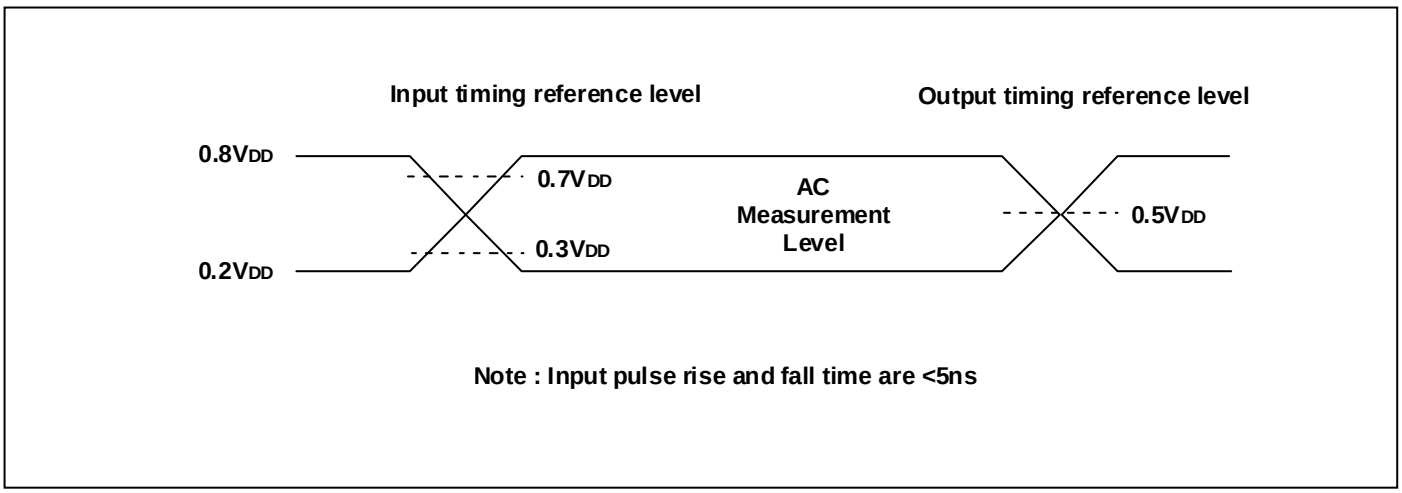


Figure 33: AC Input/Output Reference Waveforms

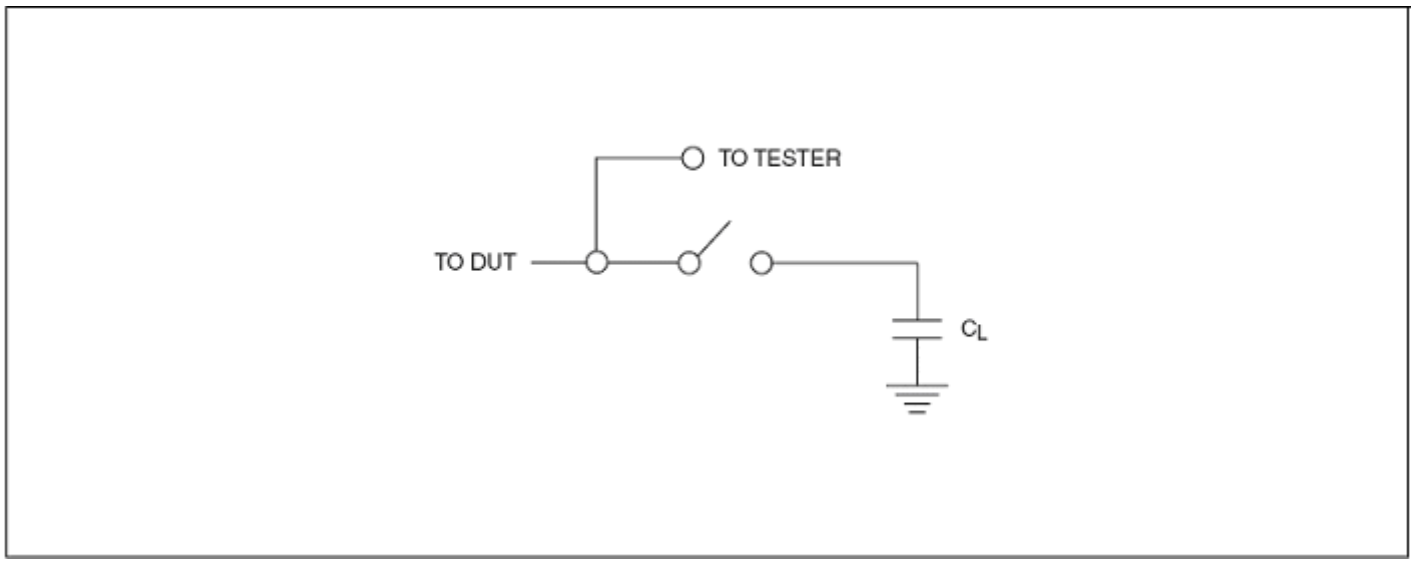
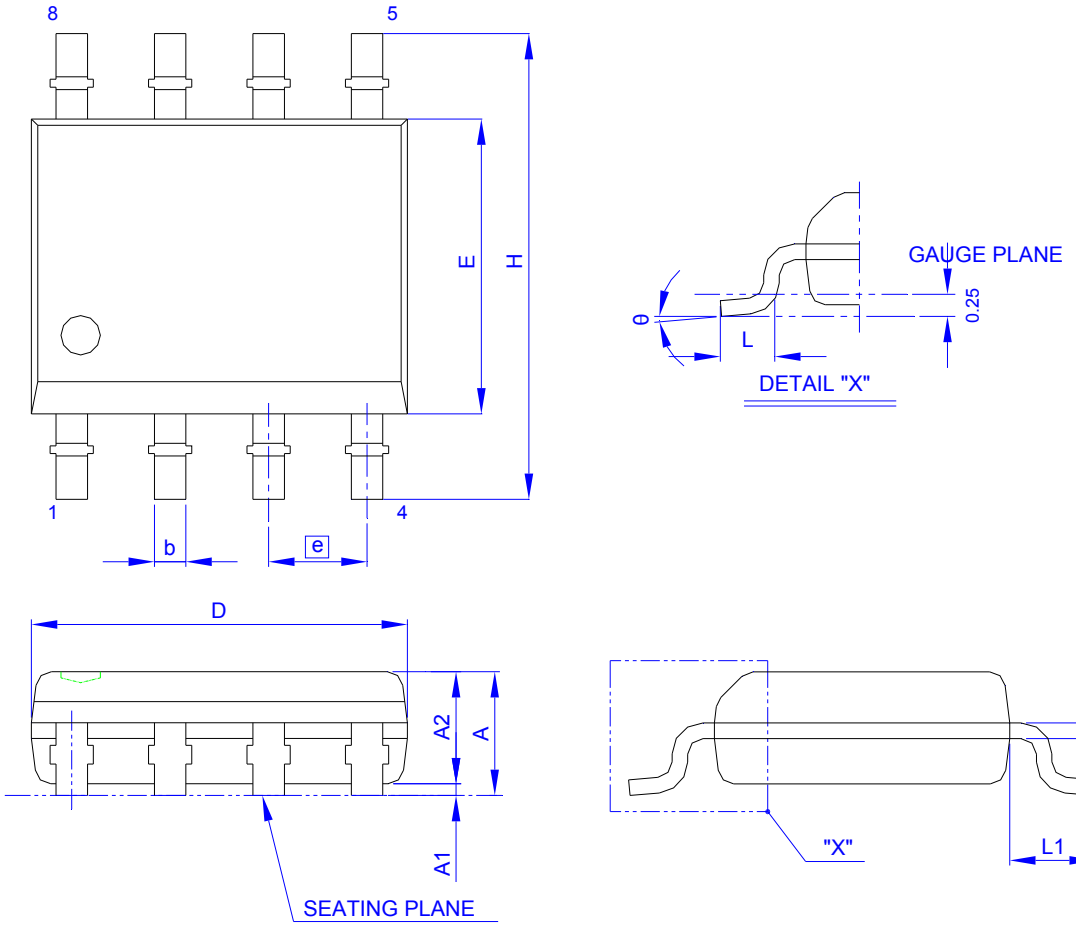


Figure 34: A Test Load Example

PACKING DIMENSIONS
8-LEAD SOIC (150 mil)

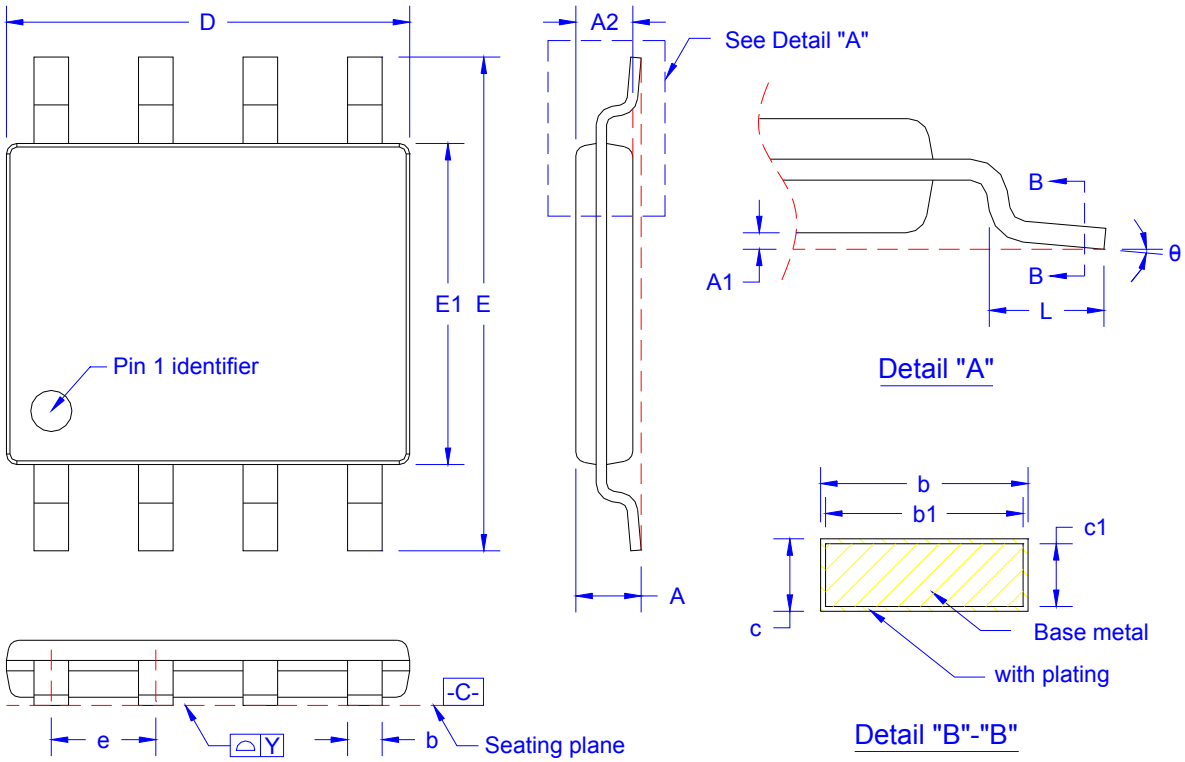


Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	1.35	1.60	1.75	0.053	0.063	0.069	D	4.80	4.90	5.00	0.189	0.193	0.197
A_1	0.10	0.15	0.25	0.004	0.006	0.010	E	3.80	3.90	4.00	0.150	0.154	0.157
A_2	1.25	1.45	1.55	0.049	0.057	0.061	L	0.40	0.66	0.86	0.016	0.026	0.034
b	0.33	0.406	0.51	0.013	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.203	0.25	0.0075	0.008	0.010	L_1	1.00	1.05	1.10	0.039	0.041	0.043
H	5.80	6.00	6.20	0.228	0.236	0.244	θ	0°	---	8°	0°	---	8°

Controlling dimension : millimenter

PACKING DIMENSIONS

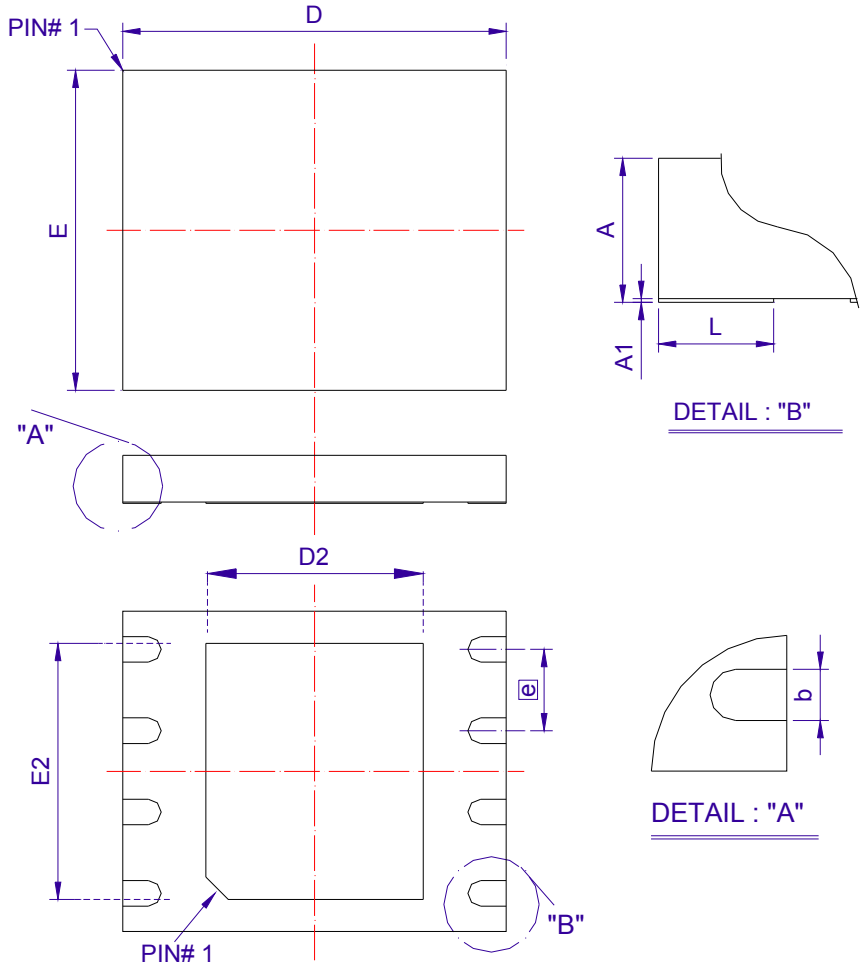
8-LEAD VSOP (150 mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.88	-	-	0.034
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.65	0.70	0.75	0.026	0.028	0.030
b	0.35	0.42	0.48	0.014	0.017	0.019
b1	0.35	-	0.46	0.014	-	0.018
c	0.09	-	0.16	0.004	-	0.006
c1	0.09	-	0.16	0.004	-	0.006
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
L	0.40	0.71	1.27	0.016	0.028	0.050
e	1.27 BSC			0.050 BSC		
Y	-	-	0.10	-	-	0.004
Θ	0°	-	10°	0°	-	10°

(Revision date : Jan 03 2013)

PACKING DIMENSIONS
8-CONTACT WSON (6x5 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.30	3.40	3.50	0.130	0.134	0.138
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.90	4.00	4.10	0.154	0.157	0.161
e		1.27 BSC			0.050 BSC	
L	0.55	0.60	0.65	0.022	0.024	0.026

Controlling dimension : millimeter

Revision History

Revision	Date	Description
0.1	2012.05.02	Original
0.2	2012.08.08	1. Modify speed from 100MHz to 104MHz 2. Modify Product ID and Ambient Operating Temperature 3. Modify the specification of T_{PP}, T_{BE2}(max) and T_{CE}(typ) 4. Correct D2(Min), D2(Max), E2(Min) and E2(Max) value of WSON packing dimensions
0.3	2012.09.11	Add VVSOP package
0.4	2012.10.29	1. Modify VVSOP to VSOP 2. Correct the description of Block Protection, Block Protection Lock-Down
0.5	2012.11.06	Modify the thickness of VSOP
0.6	2013.01.09	Modify Product ID of VSOP (150mil)

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.