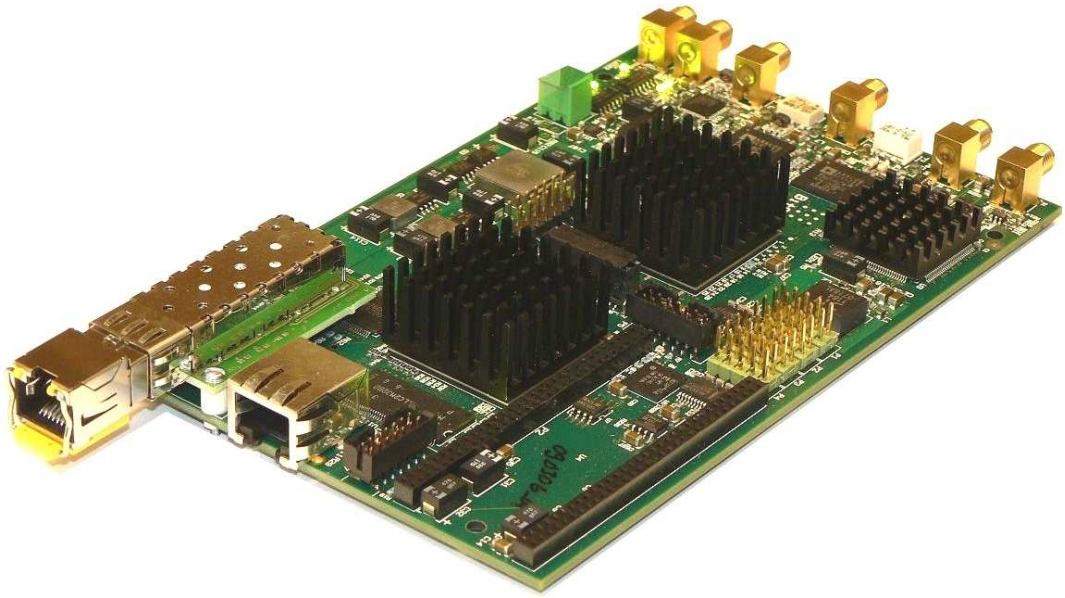
Ultra High-Speed Acquisition Board – Real Time Signal Processing



General

The UHAB (Ultra High-speed Acquisition Board) has both analog to digital and digital to analog converters on board as well as two Virtex-4 SX35 FPGAs, one for DSP and the other for data communication.

Features

- Dual 8bit 1.5 GSps ADC
- Two 14bit 1.2 GSps DACs
- Two Virtex-4 SX35 FPGAs
- Single 5V DC supply (typ. 15W)
- 100x160 mm (Eurocard) form factor (excl. backplane connector)
- Flexible communication solutions (optical & electrical Ethernet, RS232)
- Numerous number of digital I/O (>50 signals)
  - Commercial temperature range
  - Supervision of temperature and power for all key components
  - 2Mx32 (optional 4Mx32 or 8Mx32) 167MHz SDRAM & 4Mbit Serial FLASH (SPI) on board
  - Optional memory: SD Card

APPLICATIONS

- Broadband communication systems
- Instrumentation, automatic test equipment
- Electronic Warfare (e.g. Radar)
- Direct RF Down Conversion
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communication Systems
- Test Instrumentation

Analog In

One ADC08D1520 dual channel 8bit 1.5 GSps ADC. Possible to use in interleave mode to get a single channel 3 GSps converter.

BW = 2.0 GHz.

The two inputs are single ended AC coupled through SMA connectors.

Analog Out
Two 14bit AD9736 DACs capable of 1200 MSps conversion rate.

Single ended SMA connector out. Optionally differential MMCX connectors.

DSP FPGA
There is one Xilinx Virtex-4 SX35 FPGA dedicated for DSP, featuring 192 MACS in HW, possible to run at 500MHz, 34,560 Logic Cells, 3.456 Mbit memory. It provides an interface to the ADC and the DAC.

COM FPGA
There is one FPGA, of the same type as the DSP FPGA, dedicated to data communication. It can also be used to extend the DSP capabilities of the DSP FPGA. The COM FPGA is connected to the SFP cage and the piggy-back connector as well as all the memories, i.e. the SDRAM, serial FLASH and the SD Card socket. The two FPGAs are inter-connected through 20 high-speed LVDS pairs.

Digital I/O
SERCOM - Synchronous serial communication using LVDS via RJ-45 at 500 Mbps. An extra single ended signal is provided for e.g. flow control.

DIG_SMA - The DSP FPGA has an MMCX connector that can be used as digital input/output, e.g. as trigger.

DIG_MMCX - Each FPGA has a MMCX connector that can be used as digital input/output.

INTERCOM - A fine pitch (1.27) 26pin header provides 12 LVDS 250 Mbps pairs (3 Gbps total capacity) for inter-connection to a second UHAB board, for e.g. synchronous handling of several channels.

I/O Header - Each FPGA has a 14pin header used for e.g. test purposes, e.g. carrying 6 differential pairs or 12 single ended signals.

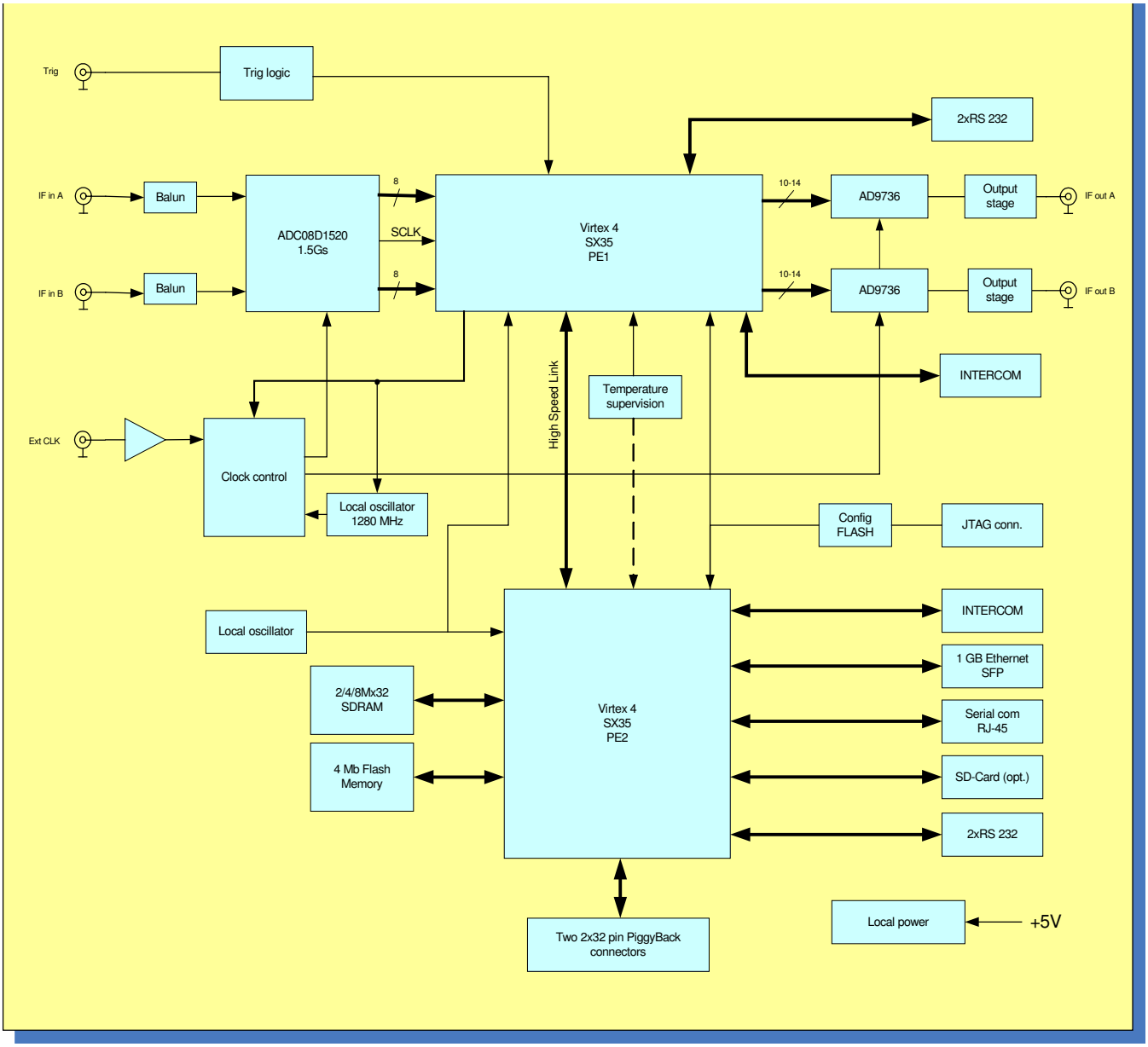
Data Communication
RS232 - Two on each FPGA.

SFP – 1 Gbps Ethernet optical or electrical link for data transfer of acquisition data to e.g. a PC over UDP protocol. The UDP protocol (optional) is implemented in HW in the COM FPGA, available as IP from BitSim.

FPGA Programming
The FPGAs can be programmed in one of several ways, from the on-board configuration PROM at power-on, via the JTAG chain to facilitate remote update of the FPGAs.

BSP (Board Support Package)
BitSim provides a BSP that implements all of the framework needed to build a complete data acquisition system. The BSP consists of IPs for the interface blocks to the ADC & DACs. Optional IPs are available such as UDP (in HW), RS232 and SERCOM etc. Other IPs can be added on request.

Block Diagram



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Rev E November 2009

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