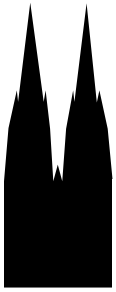
DATA SHEET



Cologne Chip Designs

HFC - S 2BDS0

ISDN HDLC FIFO controller with S/T interface

March 1997

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Features

- Independent Read and Write HDLC-Channels for 2 ISDN B-channels and one ISDN D-channel
- B1 and B2 transparent mode independently selectable
- FIFO-depth: 4x 7.5 KByte (B-channel) and 2x 512 Byte (D-channel)
- max. 31 HDLC frames (B-channel) and 15 HDLC fra mes (D-channel) per channel and direction in FIFO
- 56 kbit/s restricted mode for U.S. ISDN lines selectable
- full I.430 ITU S/T ISDN support in TE and NT mode
- PCM30 interface configurable to interface MITEL ST ™ bus (MVIP™), Siemens IOM2™ or GCI™ for external codecs
- direct 8 bit ISA-PC bus interface with buffers for ISA-databus
- One of 6 interrupt channels on ISA-PC bus selectable by software
- Only 2 I/O-addresses used on ISA-PC bus
- programmable ISA-I/O-addresses
- microprocessor int erface compatible to Motorala bus and Siemens/Intel bus
- simple DMA access to PCM30 interface for tone synthetisation
- Timer with interrupt and watchdog capability in processor mode
- 3-5V supply voltage
- rectangular QFP 100 case

1 General description

The HFC-S is an ISDN S/T HDLC basic rate controller for so called „passive“ ISDN PC cards with integrated S/T interface and PCM30 highway interface. It only needs an external SRAM to form a high performance ISDN PC card. Most problems with passive ISDN PC cards as small FIFOs and massive interrupt load for the host CPU are overcome by the HFC-S. So we call ISDN cards with the HFC-S „semi-active“.

Additionally the HFC-S can be used as a microprocessor peripheral in non-PC applications.

The FIFOs of the HFC-S are realized with an external SRAM. Also an industrial standard serial interface for telecom peripheral ICs is implemented. Codecs are normally connected to this interface.

1.1 Applications

- ISDN PC card
- ISDN terminal adapter
- ISDN PABX
- ISDN modems

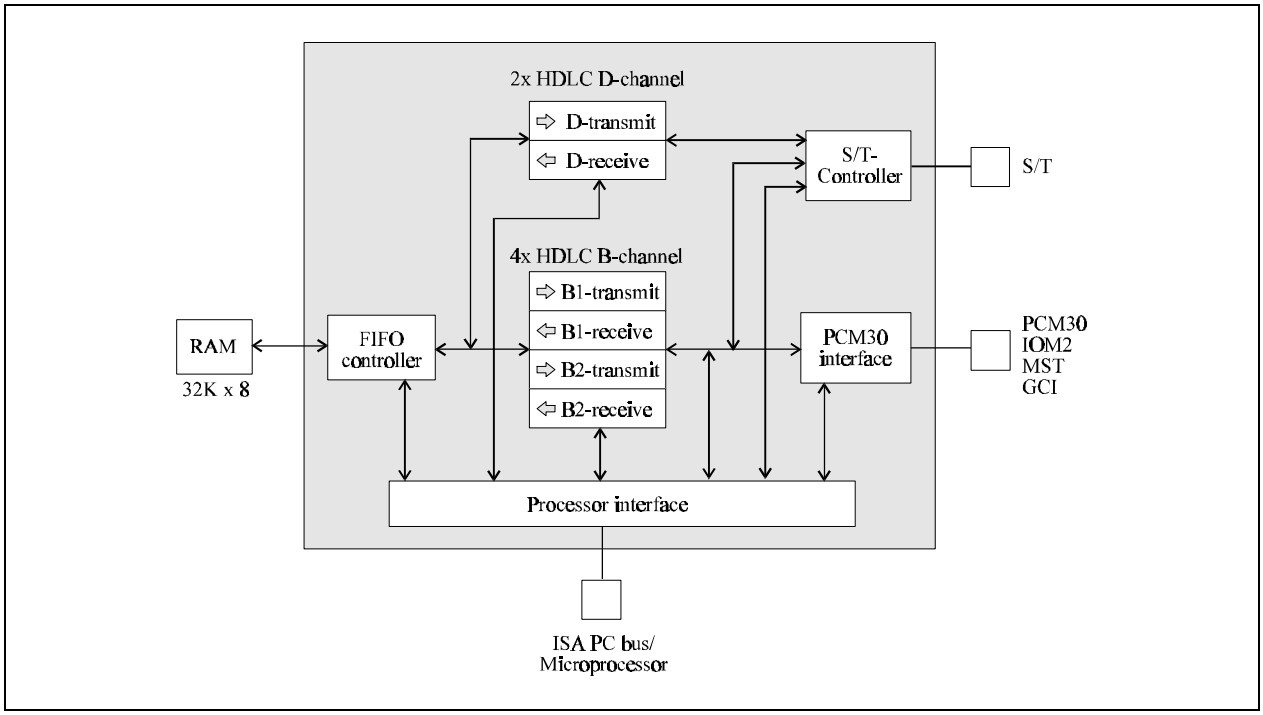


Figure 1: HFC-S block diagram

1.2 Mode description

The HFC-S has 4 different bus modes, which can be selected by the lines ALE and IIOSEL0-IIOSEL3. Depending on the selected mode the function of several pins is different (see: Pin description).

1.2.1 ISA-PC mode

Mode 1: ALE to GND, IIOSEL3-0 from 0001 to 1111

In mode 1 the HFC-S is addressed by two successive port addresses on the ISA-PC bus. The port address is selected by the lines SA0 - SA9.
The address with SA0='1' is for register selection and the address with SA0='0' is used for data read/write (see also: 3.1).

1.2.2 Processor interface modes

The processor modes are selected by IIOSEL3-0 = '0000' (see also 3.2).

Mode 2: Motorola bus with control signals /CS, R/W, /DS is s elected by setting ALE to VDD.

Mode 3: Siemens/Intel bus with seperated address bus and databus and control signals /CS, /WR, /RD is selected by setting ALE to GND.

Mode 4: Intel bus with multiplexed address and databus with control signals /CS, /WR, /RD, ALE.
ALE latches the address. The address lines SA0-SA7 must be connected to the data lines BD0-BD7.

The lines SA0-SA7 are used for direct addressing the internal registers of the HFC-S.

2 Pin description

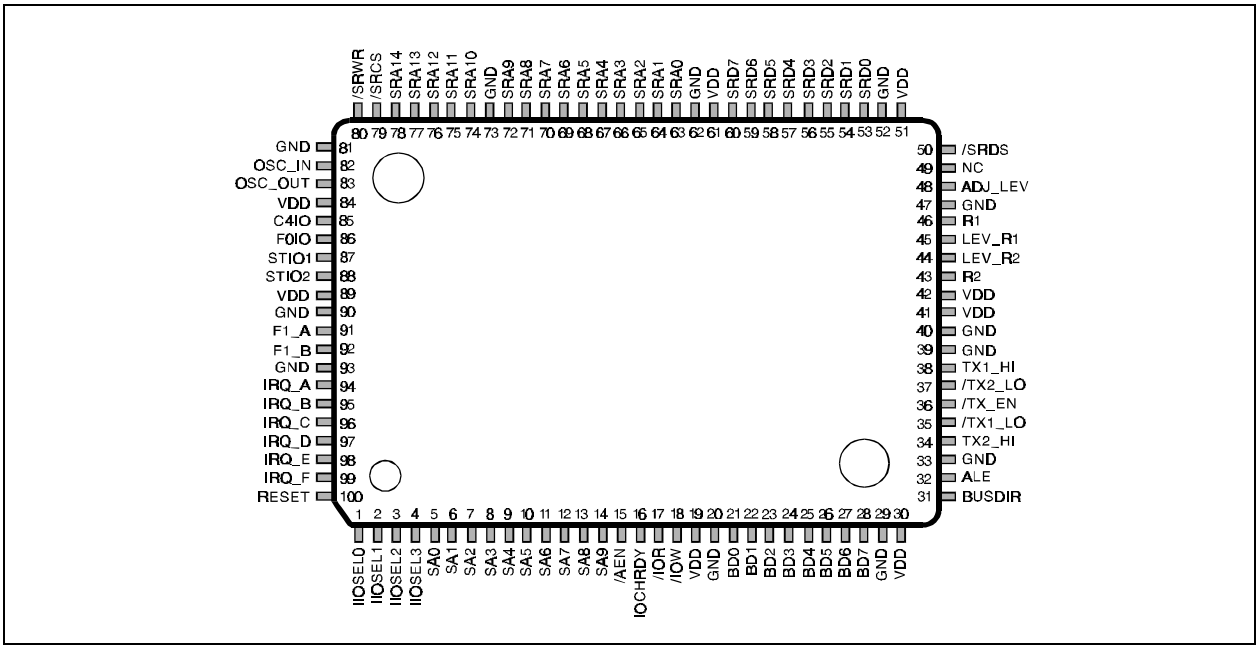


Figure 2: Pin Connection

2.1 ISA-PC bus and microprocessor interface

Pin No.	Pin Name	Input Output Tristate	Mode	Function
				Mode/initial I/O address select
1	IIOSEL0	I [u)]	all	bit 0
2	IIOSEL1	I [u)]	all	bit 1
3	IIOSEL2	I [u)]	all	bit 2
4	IIOSEL3	I [u)]	all	bit 3
				Register/ISA-PC address bus
5	SA0	I	all	Address bit 0
6	SA1	I	all	Address bit 1
7	SA2	I	all	Address bit 2
8	SA3	I	all	Address bit 3
9	SA4	I	all	Address bit 4
10	SA5	I	all	Address bit 5
11	SA6	I	all	Address bit 6
12	SA7	I	all	Address bit 7
13	SA8 /DMAAK0	I I	1 2,3,4	Address bit 8 DMA acknowledge channel 0 Direct access to PCM30 bus AUX1 channel data register (low active)

[u)] internal pull up

Pin No.	Pin Name	Input Output Tristate	Mode	Function
14	SA9 /DMAAK1	I I	1 2,3,4	address bit 9 DMA acknowledge channel 1 direct access on PCM30 bus AUX2 channel dataregister (low active)

☝ **important!**
If DMA acknowledge signals /DMAAK0 and /DMAAK1 are active, the fu nction of the read/write enables is inverted. This means a read command on the controller databus writes the AUX-Channel register and a write command reads the register. The address on the address bus (SA0-SA7) is ignored.

15	/AEN /CS	I I	1 2,3,4	PC bus address enable chipselect low active
16	IOCHRDY	OT [1)] OT [1)]	1 2,3,4	I/O channel ready low active wait signal for external processor
17	/IOR /DS	I I	1,3,4 2	I/O read enable I/O data strobe
18	/IOW R/W	I I	1,3,4 2	I/O write enable Read/Write select (WR='0')
21	BD0	I/O	all	Databus bit 0 (LSB)
22	BD1	I/O	all	Databus bit 1
23	BD2	I/O	all	Databus bit 2
24	BD3	I/O	all	Databus bit 3
25	BD4	I/O	all	Databus bit 4
26	BD5	I/O	all	Databus bit 5
27	BD6	I/O	all	Databus bit 6
28	BD7	I/O	all	Databus bit 7 (MSB)
31	BUSDIR	O	all	Databus direction signal for external busdriver '0' BD0-BD7 are outputs
32	ALE	I		Address latch enable ALE to GND and IIOSEL0-3 ≠0000: mode 1 ALE to VDD and IIOSEL0-3=0000: mode 2 ALE to GND and IIOSEL0-3=0000: mode 3 pulse on ALE and IIOSEL0-3=0000: mode 4

[1)] open drain, external pull up resistor required

2.2 S/T interface transmit signals

Pin No.	Pin Name	Input Output Tristate	Function
34	TX2_HI	O	Transmit output 2
35	/TX1_LO	OT	GND driver for transmitter 1
36	/TX_EN	O	Transmit enable
37	/TX2_LO	OT	GND driver for transmitter 2
38	TX1_HI	O	Transmit output 1

See also: 7.2 External transmitter circuitry .

2.3 S/T interface receive signals

43	R2	I	Receive data 2
44	LEV_R2	I	Level detect for R2
45	LEV_R1	I	Level detect for R1
46	R1	I	Receive data 1
48	ADJ_LEV	OT	Levelgenerator

See also: 7.1 External receiver circuitry .

2.4 SRAM Interface

			SRAM data bus
53	SRD0	I/O	SRAM data bit 0 (LSB)
54	SRD1	I/O	SRAM data bit 1
55	SRD2	I/O	SRAM data bit 2
56	SRD3	I/O	SRAM data bit 3
57	SRD4	I/O	SRAM data bit 4
58	SRD5	I/O	SRAM data bit 5
59	SRD6	I/O	SRAM data bit 6
60	SRD7	I/O	SRAM data bit 7 (MSB)
			SRAM address bus
63	SRA0	O	SRAM address bus bit 0 (LSB)
64	SRA1	O	SRAM address bus bit 1
65	SRA2	O	SRAM address bus bit 2
66	SRA3	O	SRAM address bus bit 3
67	SRA4	O	SRAM address bus bit 4
68	SRA5	O	SRAM address bus bit 5
69	SRA6	O	SRAM address bus bit 6
70	SRA7	O	SRAM address bus bit 7
71	SRA8	O	SRAM address bus bit 8
72	SRA9	O	SRAM address bus bit 9

Pin No.	Pin Name	Input Output Tristate	Function
74	SRA10	O	SRAM address bus bit 10
75	SRA11	O	SRAM address bus bit 11
76	SRA12	O	SRAM address bus bit 12
77	SRA13	O	SRAM address bus bit 13
78	SRA14	O	SRAM address bus bit 14 (MSB)
50	/SRDS	O	**SRAM control signals** Data strobe to external device
79	/SRCS	O	SRAM chip select
80	/SRWR	O	SRAM write enable

2.5 Oscillator

82	OSC_IN	I	Oscillator input or quarz connection 12.288 Mhz for HFC-S with PCM30 bus function
83	OSC_OUT	O	Oscillator output or quarz connection

2.6 PCM30 bus interface

Pin No.	Pin Name	Input Output Tristate	Mode	Function
85	C4IO	I/O [u)]	all	4.096 Mhz clock PCM30 bus clock master output PCM30 bus clock slave input (reset default)
86	F0IO	I/O [u)]	all	Frame synchronisation, 8kHz pulse for PCM30 bus frame synchronisation PCM30 bus master output PCM30 bus slave input (reset default)
87	STIO1	I/OT [u)]	all	PCM30 bus databus I Slotwise programmable as input or output
88	STIO2	I/OT [u)]	all	PCM30 bus databus II Slotwise programmable as input or output

[u)] internal pull up

2.7 PCM30 Timeslot enable signals

(e. g. for PCM codecs)

91	F1_A	O	all	enable signal for external CODEC A Programmable as positive (reset default) or negative pulse.
92	F1_B	O	all	enable signal for external CODEC B Programmable as positive (reset default) or negative pulse.

2.8 Interrupt outputs

Pin No.	Pin Name	Input Output Tristate	Mode	Function
94	IRQ_A /IRQ_P	OT OT [1]	1 2,3,4	PC bus interrupt request A processor interrupt request low active
95	IRQ_B IRQ_P	OT OT [2]	1 2,3,4	PC bus interrupt request B processor interrupt request high active
96	IRQ_C /WD_RES	OT OT [1]	1 2,3,4	PC bus interrupt request C Watchdog expired, external reset low active
97	IRQ_D WD_RES	OT OT [2]	1 2,3,4	PC bus interrupt request D Watchdog expired, external reset high active
98	IRQ_E DMARQ0	OT O	1 2,3,4	PC bus interrupt request E DMA request AUX1 channel register (high active)
99	IRQ_F DMARQ1	OT O	1 2,3,4	PC bus interrupt request F DMA request AUX2 channel register (high active)

[1] open drain, external pull up resistor required
[2] open source, external pull down resistor required

2.9 Miscellaneous pins

49	NC			No connection (leave pin open)
100	RESET	I	all	Reset for HFC-S (high active)

2.10 Power supply

Pin No.	Pin Name	Function
19, 30, 41, 89, 42, 51, 61, 84	VDD	VDD (+3V to +5V)
20, 29, 33, 39, 40, 47, 52, 62, 73, 81, 90, 93	GND	GND

☝ **important!**
All power supply pins VDD and GND must be directly connected to each other.

To keep VDD and GND bounce to a minimum a bypass capacitor (10 nF to 100 nF) should be placed between each pair of VDD/GND pins.

2.11 RESET characteristics

The reset signal (hardware reset and soft reset) must be active for at least 4 clock cycles.

The PCM30 bus lines STIO1 and STIO2 and the interrupt lines are in tristate mode after a reset.

The HFC-S is in slave mode after reset.

C4IO and F0IO are inputs.

The lines F1_A and F1_B are '0'.

In the processor modes DMARQ1 and DMARQ2 are inactive ('0').

The S/T state machine is stuck to '0' after reset. This means the HFC-S does not react to any signal on the S/T interface before the S/T state machine is initialised.

Registers which are cleared are explained in the register section of this data sheet.

3 Functional description

3.1 ISA-PC mode

3.1.1 Programming of I/O addresses

The HFC-S occupies two consecutive addresses in the I/O map of a PC if it is in ISA-PC mode. It decodes only the 10 lower address lines as most slot cards do on the ISA-PC bus. On the lower of both addresses SA0 = 0; on the higher SA0=1.

After every Master Reset (RESET = 1) the I/O address select circuit inside the HFC-S is in hardware mode. In this mode the HFC-S can not be accessed until it is initialised to an I/O address.

At first one of 15 different I/O addresses must be selected by the 4 inputs IIOSEL0 .. IIOSEL3 as Table 1 shows:

IIOSEL 3 2 1 0	Selected I/O address
0 0 0 0	processor mode
0 0 0 1	2E0h
0 0 1 0	2D0h
0 0 1 1	210h
0 1 0 0	2C0h
0 1 0 1	200h
0 1 1 0	2F8h
0 1 1 1	2E8h
1 0 0 0	2B0h
1 0 0 1	3E0h
1 0 1 0	320h
1 0 1 1	278h
1 1 0 0	310h
1 1 0 1	330h
1 1 1 0	300h
1 1 1 1	3E8h

Table 1: Selected I/O address after reset

The hardware selected I/O address might have an address collision with another I/O device in the PC.

After a hardware reset (RESET = 1) you must first write an I/O address into the HFC-S to set the I/O address for every further access to the device.

The procedure is as follows:
First you must write the lower 8 bits of the new I/O address you want into the lower address (SA0 = 0) of the hardware selected I/O address. The LSB of the new address is a don't care bit because the HFC-S always occupies two I/O addresses.

Then the additional 2 bits of the new I/O address have to be written into the higher address (SA0 = 1) of the hardware selected I/O address. The other 6 bits in the byte must have a special pattern to switch over to the software selected address mode. This pattern must be 0101 01 **aa**, whereby **aa** are the 2 higher address bits.

e.g.: wanted I/O address: **3A4h / 3A5h**

IIOSEL(3:0): 0001
then hardware selected I/O address is: **2E0h** = 10 1110 0000 b

write the value **A4h** or **A5h** into **2E0h** = 1010 010x b
write the value **57h** into **2E1h** = 0101 01 b pattern
11 b address
0101 0111 b

x = don't care

All further accesses to the HFC-S can only be done on the addresses **3A4h / 3A5h**. Only a master reset on the RESET pin will switch back the HFC-S into hardware selected address mode.

☝ **hint:**
It's useful to solve a possible address conflict by programming the I/O address as early as possible. It is recommendable to set the address with a simple .SYS driver in a DOS environment.

3.1.2 ISA-PC bus interface

The HFC-S only uses 2 I/O addresses with SA0 switches between data or control information in ISA-PC mode. As normal only 10 bits of the ISA-PC bus address are used for I/O address selection.

SA0	/IOR	/IOW	/AEN	Operation
X	X	X	1	no access
X	1	1	X	no access
0	0	1	0	read data
0	1	0	0	write data
1	0	1	0	read status
1	1	0	0	write control

X = don't care

☝ **important!**
ALE must be connected to GND and at least one of the IIOSEL0-3 must be '1' or open!

The HFC-S has no memory or DMA access to any component on the ISA-PC bus.

Because of its power drive characteristic it needs no external driver for the ISA-PC bus data lines.

If necessary you can add an external bus driver. In this case the output BUSDIR determines the driver direction.

BUSDIR = 1 means that data is driven into the HFC-S;
BUSDIR = 0 means that the HFC-S is read and data is driven to the external bus.

3.2 Processor mode

In the microprocessor mode the HFC-S uses 256 I/O addresses (SA0 - SA7).

/IOR /DS	/IOW R/W	/CS	ALE	Operation	Mode
X	X	1	X	no access	all
1	1	X	X	no access	all
0	1	0	1	read data	2
0	0	0	1	write data	2
0	1	0	0	read data	3
1	0	0	0	write data	3
0	1	0	0*)	read data	4
1	0	0	0*)	write data	4

X = don't care

*) 1-pulse latches I/O address.

All registers are directly accessable by their I/O address (see register description).

Except in mode 4 ALE is assumed to be stable after a RESET.

3.2.1 DMA access in processor mode

In processor mode a simple DMA access to the auxiliary channels of the PCM30 interface is possible. This is useful for tone synthetisation or for voice recording. DMAREQ is asserted every 125µs at a BUSY/NOBUSY transition. DMAREQ is reset when /DMAAK is active.

Mode	/DMAAK0	/DMAAK1	/CS	ALE	/IOR /DS	/IOW R/W	Function
2,3,4	1	1	X	X	X	X	no DMA
2	0	1	X	1	X	0	DMA read AUX1
2	0	1	X	1	X	1	DMA write AUX1
2	1	0	X	1	X	0	DMA read AUX2
2	1	0	X	1	X	1	DMA write AUX2
3	0	1	X	0	1	0	DMA read AUX1
3	0	1	X	0	0	1	DMA write AUX1
3	1	0	X	0	1	0	DMA read AUX2
3	1	0	X	0	0	1	DMA write AUX2
4	0	1	X	0*)	1	0	DMA read AUX1
4	0	1	X	0*)	0	1	DMA write AUX1
4	1	0	X	0*)	1	0	DMA read AUX2
4	1	0	X	0*)	0	1	DMA write AUX2

Table 2: DMA access in processor mode

*) 1-pulse latches I/O address.

3.3 Register description

In ISA-PC mode all registers are selected by first writing the address into the Control Internal Pointer (CIP) register. This is done by writing the HFC-S on the higher address SA0 = 1.
All consecutive read or write data accesses (SA0 = 0) are done with the selected register until the CIP register is changed.

In processor mode all registers can be directly accessed. The registers are selected by SA0 - SA7.

3.3.1 FIFO control registers

The FIFO control registers are used to select and control the FIFOs of the HFC-S. In processor mode the value is the address which directly selects the corresponding register.

CIP / I/O-address
10zzzzzd **z**: 5 bits for D-channel FIFO register control
10yyyyff **y**: 4 bits for B-channel FIFO register control

yyyy	**zzzzz**		
0000	01000	FIFO input counter (Z1) low byte	**r)**
0001	01010	FIFO input counter (Z1) high byte	**r)**
0010	01100	FIFO output counter (Z2) low byte	**r)**
0011	01110	FIFO output counter (Z2) high byte	**r)**
HDLC mode:			
1010	01001	dummy for increment of frame counter (F1)	**r)**
1011	01011	data write into FIFO and increment Z1	**w)**
1100	01101	FIFO input HDLC frame counter (F1)	**r)**
1101	01111	FIFO output HDLC frame counter (F2)	**r)**
1110	10001	dummy for increment of frame counter (F2)	**r)**
1111	10011	data read out of FIFO and increment Z2	**r)**
Transparent mode (only selectable for B-channels):			
1010		data write into FIFO upside down and increment Z1	**w)**
1011		data write into FIFO and increment Z1	**w)**
1100		FIFO input HDLC frame counter (F1)	**r)**
1101		FIFO output HDLC frame counter (F2)	**r)**
1110		data read out of FIFO upside down and incremement Z2	**r)**
1111		data read out of FIFO and increment Z2	**r)**

f: B-channel FIFO-No.:

00	channel B1 transmit	10	channel B2 transmit
01	channel B1 receive	11	channel B2 receive

d: D-channel FIFO-No.:
0 D-channel transmit direction
1 D-channel receive direction

r) corresponding data register is read only
w) corresponding data register is write only

☝ **important!**
FIFO change
Changing the FIFO must be the last FIFO operation in a non BUSY phase. The new FIFO is selected after one busy phase.
To select a new FIFO in processor mode a dummy value must be written to the Z1 register address of this FIFO. The Z1 register is not changed by this operation.

Incrementation of the frame counters (F1, F2)
If the frame counters (F1, F2) are changed it must be in a seperate non BUSY period. That means writing data to the FIFO or reading data from the FIFO is not allowed during this period. Also selecting a new FIFO is not allowed. Reading the counters Z1, Z2, F1 and F2 is allowed before incrementing the frame counter.

Accessability of registers
All operations on the FIFOs and on FIFO control registers and on B- and D-channel data registers of the S/T and PCM30 bus part are only allowed in the non BUSY period of the HFC-S.

Status, interrupt and control registers can be read and written at any time.

3.3.2 Registers of the S/T section

CIP / I/O-address		Name	r/w	Function
00110000	30h	STATES	r/w	State of the TE/NT state machine
00110001	31h	SCTRL	w	S/T control register
00110010	32h	TEST	w	Power-Up mode
00110100	34h	SQ_REC SQ_SEND	r w	receive register for S/Q bits send register for S/Q bits
00110111	37h	CLKDEL	w	setup of the delay time between receive and send direction (TE) receive data sample time (NT)
00111100	3Ch	B1_REC*) B1_SEND*)	r w	B1-channel receive register B1-channel transmit register
00111101	3Dh	B2_REC*) B2_SEND*)	r w	B2-channel receive register B2-channel transmit register
00111110	3Eh	D_REC*) D_SEND*)	r w	D-channel receive register D-channel transmit register

*) These registers are read/written automatically by the HDLC FIF O controller (HFC) or PCM30 bus controller and need not be accessed by the user.

3.3.3 Registers of the PCM30 bus section

PCM30 bus timeslot selection registers

CIP / I/O-address		Name	r/w	Function
00100000	20h	B1_SSL	w	B1-channel transmit slot (0..31)
00100001	21h	B2_SSL	w	B2-channel transmit slot (0..31)
00100010	22h	AUX1_SSL	w	AUX1-channel transmit slot (0..31)
00100011	23h	AUX2_SSL	w	AUX2-channel transmit slot (0..31)
00100100	24h	B1_RSL	w	B1-channel receive slot (0..31)
00100101	25h	B2_RSL	w	B2-channel receive slot (0..31)
00100110	26h	AUX1_RSL	w	AUX1-channel receive slot (0..31)
00100111	27h	AUX2_RSL	w	AUX2-channel receive slot (0..31)

PCM30 bus data registers

CIP / I/O-address		Name	r/w	Function
00101000	28h	B1_D*)	r/w	PCM30 bus B1-channel data register
00101001	29h	B2_D*)	r/w	PCM30 bus B2-channel data register
00101010	2Ah	AUX1_D**)	r/w	AUX1-channel data register
00101011	2Bh	AUX2_D**)	r/w	AUX2-channel data register

PCM30 bus configuration registers

CIP / I/O-address		Name	r/w	Function
00101110	2Eh	MST_MODE	w	mode register for PCM30 bus
00101111	2Fh	CONNECT	w	connect functions for S/T, HFC, PCM30

*) These registers are read/written automatically by the HDLC FIFO controller (HFC) or by he S/T controller and need not be accessed by the user.

**) These registers can also be accessed by DMA

3.3.4 Interrupt and status register

CIP / I/O address		Name	r/w	Function
00011000	18h	CIRM	w	interrupt selection and softreset register
00011001	19h	CTMT	w	transparent mode and time control register
00011010	1Ah	INT_M1	w	interrupt mask register 1
00011011	1Bh	INT_M2	w	interrupt mask register 2 and B-channel mode register (64 kbit/s or 56 kbit/s)
00011110	1Eh	INT_S1	r	interrupt status register
00011100	1Ch	STATUS	r	common status register
00011101	1Dh	STATUS_DISBUSY		same as STATUS register but also locks busy-nobusy transition (see also 3.7.1)

3.4 Watchdog / timer

The watchdog function of the HFC-S has two different modes which can be selected by bit 5 of the CTMT register.
In the first mode the watchdog timer expires after the selected time if the timer has been reset and the INT_S1 register is not read during the watchdog timer period.
In the second mode the watchdog timer expires after the selected time if no HFC-S register is accessed during the watchdog timer period. In this mode every access to the HFC-S resets the watchdog **and** the timer.

3.5 FIFOs

There are 6 FIFOs with 6 HDLC-Controllers in the HFC-S. The HDLC circuits are located on the S/T device side of the HFC-S. So always plain data is stored in the FIFO. Zero insertion and deletion is done:

– if the data goes to the S/T device in send FIFOs and
– when the HDLC data comes from the S/T device or PCM30 bus in receive operation.

There are a send and a receive FIFO for each of the two B-channels and for the D-channel.

The FIFOs are realized as ring buffers in the external SRAM. To control them there are some counters.

	B-channel	D-channel
Z1: FIFO input counter	13 Bit	9 Bit
Z2: FIFO output counter	13 Bit	9 Bit

Each counter points to a byte position in the SRAM. On a FIFO input operation Z1 is incremented. On an output operation Z2 is incremented.

After every pulse on the F0IO signal the HFC-S goes into busy cycle and two HDLC-bytes are written into the S/T interface (FIFOs No. 0 and 2) and two HDLC-bytes are read from the S/T interface (FIFOs No. 1 and 3).
D-channel data is handled in a similar way.

> ☝ **important!**
> Instead of the S/T interface also PCM30 bus is selectable for each B-channel (see CONNECT register).

If Z1 = Z2 the FIFO is empty.

Additionally there are two counters F1 and F2 for every FIFO channel (5Bit for B-channel, 4Bit for D-channel). They count the HDLC-frames in the FIFOs and form a ring buffer as Z1 and Z2 do, too.

Again F1 is incremented when a complete frame has been received and stored in the FIFO. F2 is incremented when a complete frame has been read from the FIFO.

If F1 = F2 there is no complete frame in the FIFO.

When the RESET line is active or software reset is active Z1, Z2, F1 and F2 are all initialized to all 1s.

> ☝ **important!**
> The counter state 0200h of the Z-counters follows counter state 1FFFh in the B-channel FIFOs.
> If 8k RAM mode is selected counter state 1A00h of the Z-counters follows counter state 1FFFh in the B-channel FIFOs.
> The counter state 000h of the Z-counters follows counter state 1FFh in the D-channel FIFOs.
>
> The counter state 00h of the F-counters follows counter state 1Fh in the B-channel FIFOs.
> The counter state 10h of the F-counters follows counter state 1Fh in the D-channel FIFOs.

3.5.1 FIFO channel operation

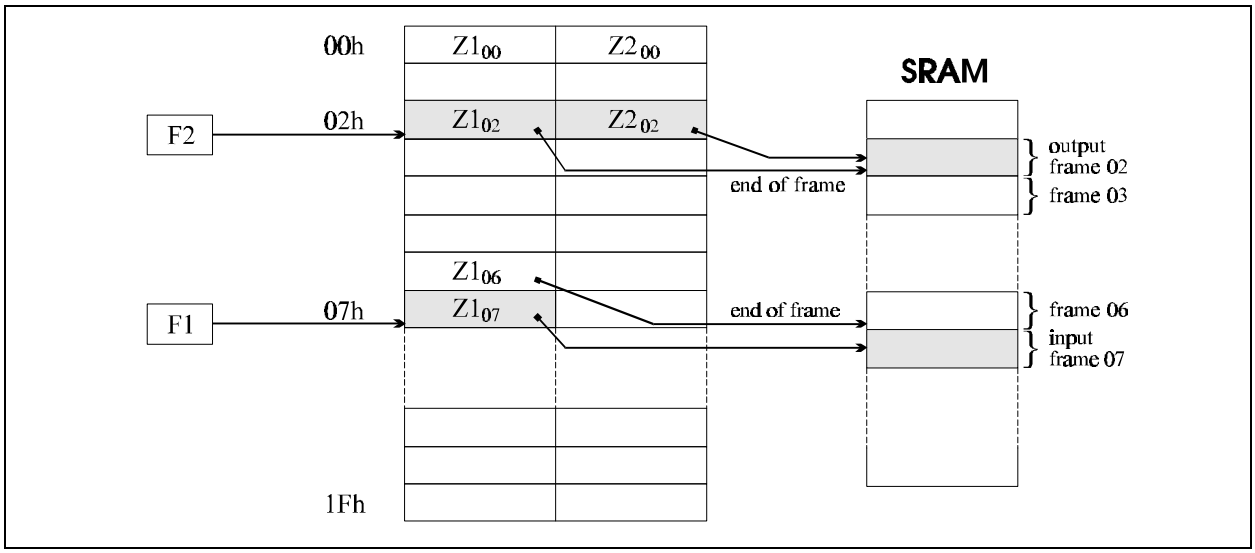


Figure 3: FIFO Organisation (shown for B-channel, similar for D-channel)

3.5.1.1 Send channels (B1, B2 and D transmit)

The send channels send data from the ISA-PC/processor bus interface to the FIFO and the HFC-S converts the data into HDLC code and tranfers it from the FIFO into the S/T or/and the PCM30 bus interface write registers.

The HFC-S checks Z1 and Z2. If Z1=Z2 (FIFO empty) the HFC-S generates a HDLC-Flag (0111 1110) and sends it to the S/T device. In this case Z2 is not incremented. If also F1=F2 only HDLC flags are sent to the S/T interface and all counters remain unchanged. If the frame counters are unequal F2 is incremented and the HFC-S tries to send the next frame to the output device. After the end of a frame (Z2 reaches Z1) it automatically generates the 16 bit CRC checksum and adds the ending flag. If there is another frame in the FIFO (F1 ≠F2) the F2 counter is incremented.

With every byte you send to the FIFO via the ISA-PC bus interface Z1 is incremented automatically. If a complete frame has been send F1 must be incremented to send the next frame. If the frame counter F1 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 3).
Z1(F1) is used for the frame which is just written from the PC-bus side. Z2(F2) is used for the frame which is just beeing transmitted to the S/T device side of the HFC-S. Z1(F2) is the end of frame pointer of the current output frame.

In the send channels F1 is only changed from the PC interface side if the software driver wants to say „end of send frame“. Then the current value of Z1 is stored, F1 is incremented and Z1 is used as start address of the next frame. Z1(F2) and Z2(F2) can not be accessed.

> ☝ **important!**
> At the start of the first frame when the FIFO is totally empty at least two bytes must be put into the FIFO before a BUSY condition is initialized by the HFC-S. This is necessary to avoid the initialisation of a CRC sequence after a one-byte frame. To satisfy this condition you should wait for a BUSY / NOBUSY status transition. In this case there is enough time to write more than one byte into the FIFO.

3.5.1.2 FIFO full condition in send channels

Due to the limited number of registers in the HFC-S the driver software must maintain a list of frame start and end addresses to calculate actual FIFO depth and check FIFO full condition. Because there are a maximum of 32 frame counter values and the start address of a frame is the incremented value of the last frame end address the memory table must have only 32 values of 16 bits (13 bits) instead of 64.

Remember that an increment of Z-value 1FFFh is 0200h in the B-channels!

There are two different FIFO full conditions. The first one is met when the FIFO contents comes up to 31 frames (B-channel) or 15 frames (D-channel). There is no possibility for the HFC-S to manage more frames even if the frames are very small.

The second limitation is the depth of the FIFO which is 512 byte for the D-channel and 7.5 KByte for the B-channel (32KByte external RAM).

3.5.1.3 Receive Channels (B1, B2 and D reiceive)

The receive channels receive data from the S/T or PCM30 bus interface read registers. The data is converted from HDLC into plain data and send to the FIFO. The data can then be read via the processor interface.

The HFC-S checks the HDLC data coming in. If it finds a flag or more than 5 consecutive 1s it does not generate any output data. In this case Z1 is not incremented. Proper HDLC data being received is converted by the HFC-S into plain data. After the ending flag of a frame the HFC-S checks the HDLC CRC checksum. If it is correct one byte with all 0s is inserted behind the CRC data in the FIFO named STAT. This last byte of a frame in the FIFO is different from all 0s if there is no correct CRC field at the end of the frame.

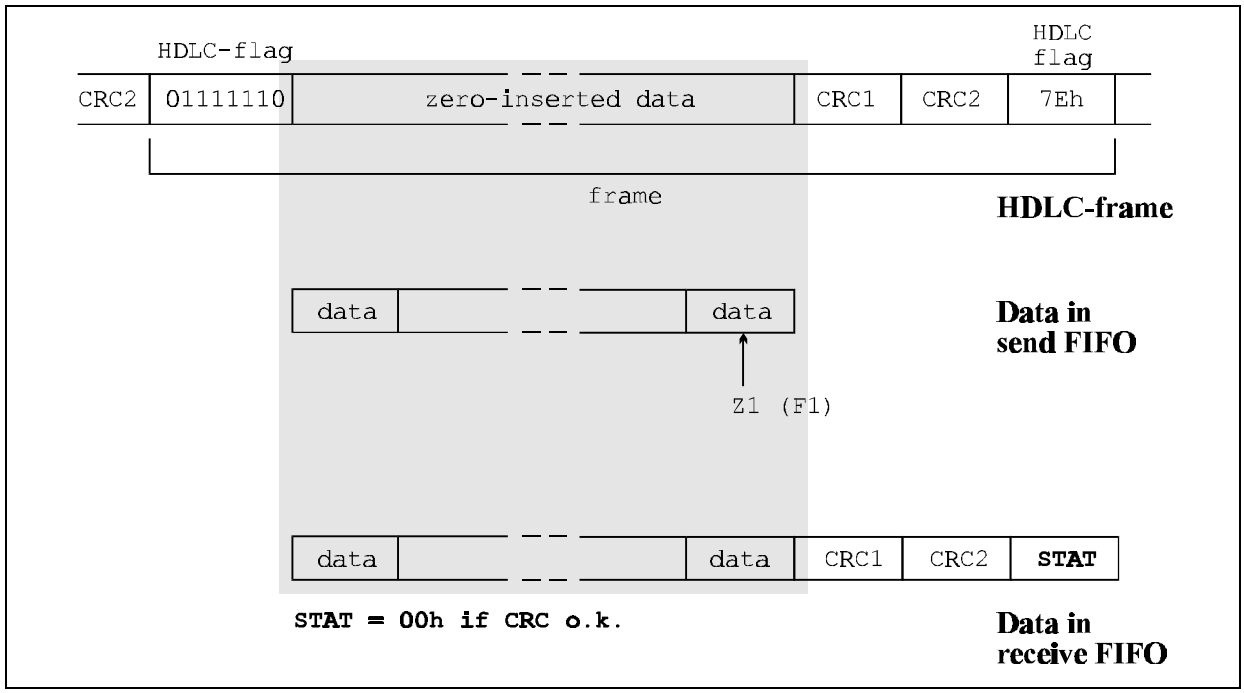


Figure 4: FIFO Data Organisation

The ending flag of a HDLC-frame can also be the starting flag of the next frame.

After a frame is received completely F1 is incremented by the HFC-S automatically and the next frame can be received.

After reading a frame via the processor bus interface F2 must be incremented. If the frame counter F2 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 3).
Z1(F1) is used for the frame which is just received from the S/T device side of the HFC. Z2(F2) is used for the frame which is just beeing transmitted to the ISA-PC bus interface. Z1(F2) is the end of frame pointer of the current output frame.

To calculate the length of the current receive frame the software has to evaluate Z1-Z2+1. When Z2 reaches Z1 the complete frame has been read.

In the receive channels F2 must be incremented from the PC interface side after the software detects an end of receive frame (Z1=Z2) and F1 ≠F2. Then the current value of Z2 is stored, F2 is incremented and Z2 is copied as start address of the next frame. If Z1 = Z2 and F1 = F2 the FIFO is totally empty. Z1(F1) can not be accessed.

3.5.1.4 FIFO full condition in receive channels

Because the ISDN-B-channels and the ISDN-D-channels have no hardware based flow control there is no possibility to stop input data if a receive FIFO is full.

So there is no FIFO full condition implemented in the HFC-S. The HFC-S assumes that the FIFOs are so deep that the host processor hardware is able to avoid any overflow of the receive FIFOs. Overflow conditions are again more than 31 input frames (15 frames for D-channel) or a real overflow of the FIFO because of excessive data.

Because HDLC procedures only know a window size of 7 frames no more than 7 frames are send without software intervention. Due to the great depth of the FIFOs of the HFC-S it is easy to poll the HFC-S even in large time intervalls without having to fear a FIFO overflow condition.

However to avoid any undetected FIFO overflows the software driver should check the number of frames in the FIFO which is F1-F2. An overflow exists if the number (F1-F2) is less than the number in the last reading even if there was no reading of a frame in between.

After a detected FIFO overflow condition the HFC-S must be reset via the software or hardware RESET!

3.5.1.5 FIFO initialisation

All counters Z1, Z2, F1 and F2 of all FIFOs are initialized to all 1s after a RESET. The RESET signal must have a length of at least 4 clock cycles.

Then the result is Z1 = Z2 = 1FFF $_h$ and F1 = F2 = 1F $_h$ for the B-channels
and Z1 = Z2 = 1FFh and F1 = F2 = 1Fh for the D-channel.

Please mask bit 4 of D-channel from counter F1, F2.

The same initialisation is done if the bit 3 in the CIRM register is set (soft reset).

3.5.2 Transparent mode of HFC-S

You can switch off HDLC operation for each B-channel independently. There is one bit for each B-channel in the CTMT control register. If this bit is set data in the FIFO is send directly to the S/T or PCM30 bus interface and data from the S/T or PCM30 bus interface is send directly to the FIFO.

Be sure to switch into transparent mode only if F1=F2. Being in transparent mode the Fx counters remain unchanged. Z1 and Z2 are the input and output pointers respectively. Because F1=F2 both Z-counters are always accessable and have valid data.

If a send FIFO channel changes to FIFO empty condition no CRC is generated and the last data byte written into the FIFO is repeated until there is new data.

In receive channels there is no check on flags or correct CRCs and no status byte is added.

The byte bounderies are not arbitrary like in HDLC mode where byte synchronisation is achieved with HDLC-flags. The data is just the same as it comes from the S/T or PCM30 bus interface or is send to this.

Because Fx incrementation dummy registers are not used you can send and receive transparent data in two shapes. The normal and first shape is tranporting B-channel data with the LSB first as it is usual in HDLC mode. The second shape is sending the bytes upside down as it is normal for PWM data. So the first bit is the MSB.

3.6 External SRAM

For the FIFO data an 32K x 8 external SRAM is used. A 8K x 8 external RAM is also possible but not recommended.

The required access time is 80 ns or below.

1024 Byte of the external SRAM are reserved for internal HFC-S use.

external SRAM	B-channel FIFO depth per channel and direction	D-channel FIFO depth per direction
8K x 8	1536 Byte	512 Byte
32K x 8	7680 Byte	512 Byte

Table 3: SRAM size and FIFO depth

To initialise the HFC-S for 8K x 8 SRAM use:
- write 18h to the CIRM register
- wait at least 4 clock cycles
- write 10h to the CIRM register

For all further accesses to the CIRM register bit 4 must be set.

☝ **hint!**
If you connect the HFC-S with the SRAM you can simplify PCB layout if you permutate address lines and data lines. If you connect data lines of the SRAM with data lines of the HFC-S and SR-address lines of the HFC-S with address lines of the SRAM you can do this in any order.

3.7 Busy synchronisation

For internal processing of the data channels and HDLC the HFC-S enters a busy phase every 125µs on a falling F0IO edge. During this BUSY phase most of the registers must not be accessed (all FIFO registers, B1_REC, B2_REC, B1_SEND, B2_SEND, D_REC, D_SEND, B1_D and B2_D).

The minimum BUSY phase time is 280 clock cycles (22.8µs at 12.288MHz) and the maximum BUSY phase time is 630 clock cycles (51.3µs at 12.288MHz).

3.7.1 Busy synchronisation with status read

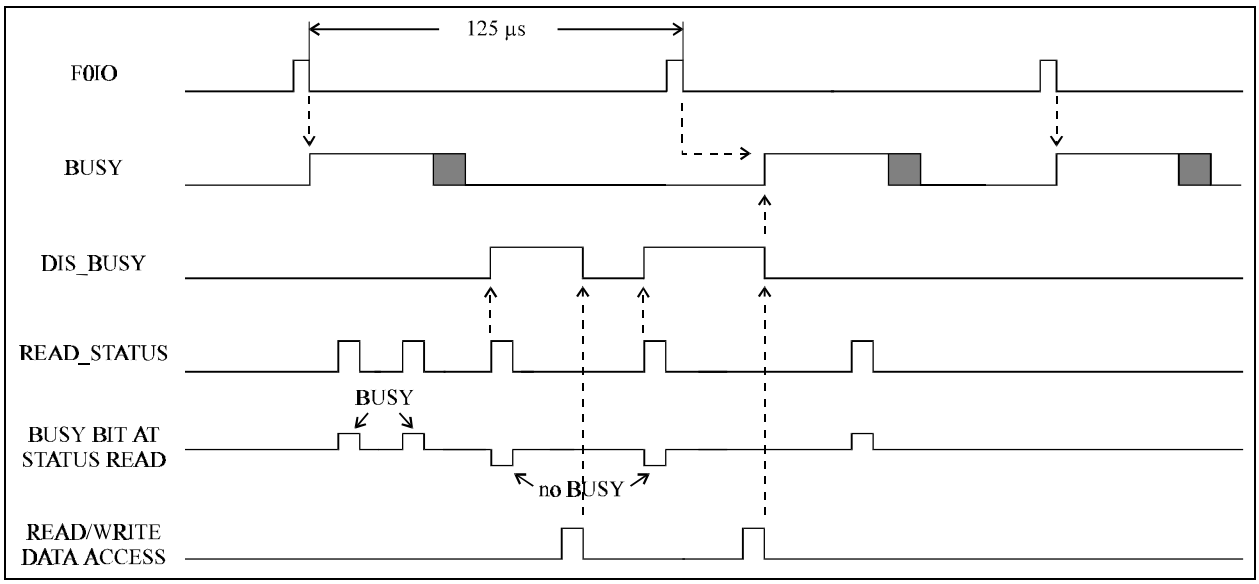


Figure 5: Timing relations and delayed BUSY

The lines BUSY and DIS_BUSY are internal signals of the HFC-S. If BUSY is high the HFC-S is in a phase when busy critical registers must not be accessed. The signal DIS_BUSY disables the start of the internal BUSY phase until the next read/write data operation is finished. To avoid loss of data the DIS_BUSY signal must not disable the BUSY so that the end of BUSY comes after the next F0IO signal (see also: STATUS register bit description).
READ_STATUS symbolizes a status read operation. The high signal means the status is read. BUSY BIT AT STATUS READ is the value returned from a read status operation (bit 0 in STATUS register). READ/WRITE DATA ACCESS symbolizes a data read/write operation.

3.7.2 Busy synchronisation with IOCHRDY

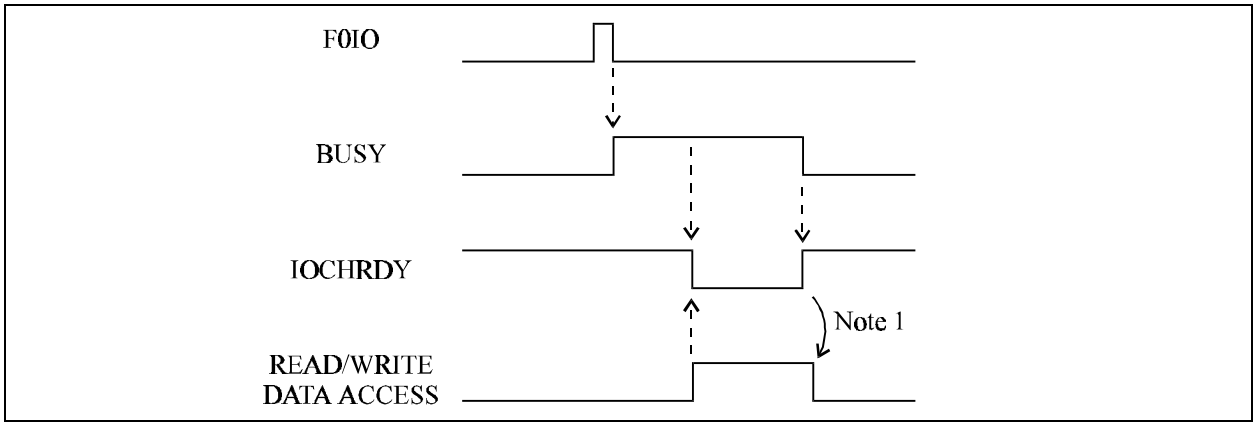


Figure 6: Function of IOCHRDY

Note 1: The read/write data access is finished by an external processor after release of IOCHRDY.

Repeated status read can be avoided if the IOCHRDY output of the HFC-S is connected to the /WAIT line of the external processor. If the HFC-S is accessed during a BUSY phase the processor waits until the end of the BUSY phase.

4 Register bit description

4.1 Register bit description of S/T section

Name	Addr.	Bits	r/w	Function
STATES	(30h)	3..0	r	binary value of actual state (NT: Gx, TE: Fx)
			w	prepare for new state xxxx
		4	w	'1' loads the prepared state (bit 3..0) and stops the state machine. This bit needs to be set for a minimum period of 5.21 µs and must be cleared by software. (reset default) '0' restarts the state machine. After writing an invalid state the state machine goes to deactivated state (G1, F2)
			r	not defined
		5	w	'0' prepare deactivation '1' prepare activation
			r	not defined
		6	w	'1' start activation/deactivation as selected by bit 5 This bit is automatically cleared after activation/ deactivation.
			r	not defined
		7	w	'0' no operation '1' in NT mode allows transition from G2 to G3. The bit is automatically cleared after the transition.
			r	not defined

☝ **important!**
The state machine is stuck to '0' after a reset. Writing a '0' to bit 4 of the STATES register restarts the state machine.
In this state the HFC-S sends no signal on the S/T-line and it is not possible to activate it by incoming INFOx.
NT mode: The NT state machine does not change automatically from G2 to G3 if the TE side sends INFO3 frames. This transition must be activated each time by bit 7 of the STATES register.

Name		Bits	r/w	Function
SCTRL	(31h)			B-channel enable
		0	w	'0' B1 send data disabled (permanent 1 sent in activated states, reset default) '1' B1 data enabled
		1	w	'0' B2 send data disabled (permanent 1 sent in activated states, reset default) '1' B2 data enabled
		2	w	S/T-interface mode '0' TE mode (reset default) '1' NT mode
		3	w	D-channel priority '0' high priority 8/9 (reset default) '1' low priority 10/11
		4	w	S/Q bit transmission '0' S/Q bit disable (reset default) '1' S/Q bit enable
		5	w	'0' normal operation (reset default) '1' send 96kHz transmit test signal (alternating zeros) only in states 4, 6, 7 (TE) and 2, 3 (NT)
		6	w	TX_LO line setup '0' capacitive line mode for normal S/T-interface (reset default) '1' non capacitive line mode
		7	w	Power down '0' power up, oscillator active (reset default) '1' power down, oscillator stopped
TEST	(32h)	0	w	Power down mode bit '0' S/T awake disable (reset default) Power up can only be programmed by register access (SCTRL bit 7). '1' S/T awake enable. Oscillator starts on every non INFO0 S/T signal.
		7..1	w	must be set to '0'

Name		Bits	r/w	Function
SQ_REC	(34h)	3..0	r	TE mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4) NT mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)
		4	r	'1' a complete S or Q dataword has been received Reading SQ_REC clears the bit.
		6,5	r	not defined
		7	r	'1' ready to send a new S or Q dataword Writing to SQ_SEND clears the bit.
SQ_SEND	(34h)	3..0	w	TE mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4) NT mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)
		7..4	w	not defined
CLKDEL	(37h)	3..0	w	TE: 4 bit delay value to configure the delay time between receive and transmit direction. The delay of the external S/T-interface circuit can be compensated. The lower the value the smaller the delay between receive and transmit direction (see Figure 12) NT: Data sample point. The lower the value the earlier the input data is sampled. The steps are 130ns at 7.68MHz clock frequency and 163ns at 12.288MHz clock frequency.
		6..4	w	NT mode only early edge input data shaping Low pass characteristic of extended bus configurations can be compensated. The lower the value the earlier input data pulse is sampled. No compensation means a value of 6 (110b). Step size is the same as for bits 3-0.
		7	w	master clock frequency selection register '0' 12.288MHz (reset default) '1' 7.68 MHz This frequency can only be used in slave mode with external master clock at PCM30 bus (C4O, F0O).

☝ **note!**
The register is initialized with a '0' after reset. The register should be initialized as follows before
activating the TE/NT state machine in 12.288 MHz mode:
TE mode: 0Dh .. 0Fh NT mode: 6Ch

4.2 Register bit description of PCM30 bus section

Timeslots for transmit direction

Name	Addr.	Bits	r/w	Function
B1_SSL	(20h)			
B2_SSL	(21h)			
AUX1_SSL		(22h)		
AUX2_SSL		(23h)		
		4..0	w	select PCM30 bus transmission slot (0..31)
		5	w	ignored
		6	w	select PCM30 bus data lines '0' STIO1 output '1' STIO2 output
		7	w	transmit channel enable for PCM30 bus '0' disable (reset default) '1' enable

☝ **important!**
Enabling more than one channel on the same slot causes undefined output data.

Timeslots for receive direction

Name		Bits	r/w	Function
B1_RSL	(24h)			
B2_RSL	(25h)			
AUX1_RSL		(26h)		
AUX2_RSL		(27h)		
		4..0	w	select PCM30 bus receive slot (0..31)
		5	w	unused
		6	w	select PCM30 bus data lines '0' STIO2 is input '1' STIO1 is input
		7	w	receive channel enable for PCM30 bus '0' disable (reset default) '1' enable

Name		Bits	r/w	Function
B1_D	(28h)			
B2_D	(29h)			
AUX1_D	(2Ah)			
AUX2_D	(2Bh)			
		0..7	r/w	read/write data registers for selected timeslot data

☝ **note!**
If the data registers AUX1_D and AUX2_D are not overwritten, the transmisson slots AUX1_SSL and AUX2_SSL mirror the data received in AUX1_RSL and AUX2_RSL slots. This is useful for an internal connection between two CODECs.

Name	Bits	r/w	Function
MST_MODE (2Eh)	0	w	PCM30 bus mode '0' slave (reset default) (C4IO and F0IO are inputs) '1' master (C4IO and F0IO are outputs)
	1	w	polarity of C4- and C2O-clock '0' F0IO is sampled on negative clock transition '1' F0IO is sampled on positive clock transition
	2	w	polarity of F0-signal '0' F0 positive pulse (reset default) '1' F0 negative pulse
	3	w	duration of F0-signal '0' F0 active for one C4-clock (244ns) (reset default) '1' F0 active for two C4-clocks (488ns)
	5, 4	w	time slot for codec-A signal F1_A '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' signal C2O -> pin F1_A (C2O is 2048kHz clock)
	7, 6	w	time slot for codec-B signal F1_B '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' AUX2 receive slot

The pulse shape and polarity of the codec signals F1_A and F1_B is the same as the pulseshape of the F0IO signals. The polatity of C2O can be changed by bit 1.

RESET sets register MST_MODE to all '0's.

4.3 Register bit description of CONNECT register

Name	Bits	r/w	Function
CONNECT (2Fh)	5..0	w	select B1-channel data flow
			destination source
			bit 0: '0' B1-HFC ← B1-S/T
			'1' B1-HFC ← B1-PCM30
			bit 1: '0' B1-S/T ← B1-HFC
			'1' B1-S/T ← B1-PCM30
			bit 2: '0' B1-PCM30 ← B1-HFC
			'1' B1-PCM30 ← B1-S/T
			select B2-channel data flow
			destination source
			bit 3: '0' B2-HFC ← B2-S/T
			'1' B2-HFC ← B2-PCM30
			bit 4: '0' B2-S/T ← B2-HFC
			'1' B2-S/T ← B2-PCM30
			bit 5: '0' B2-PCM30 ← B2-HFC
			'1' B2-PCM30 ← B2-S/T
	7, 6	w	unused

RESET sets CONNECT register to all '0's.

The following figure shows the different options for switching the B1-channel with the CONNECT register. The options for the B2-channel are the same.

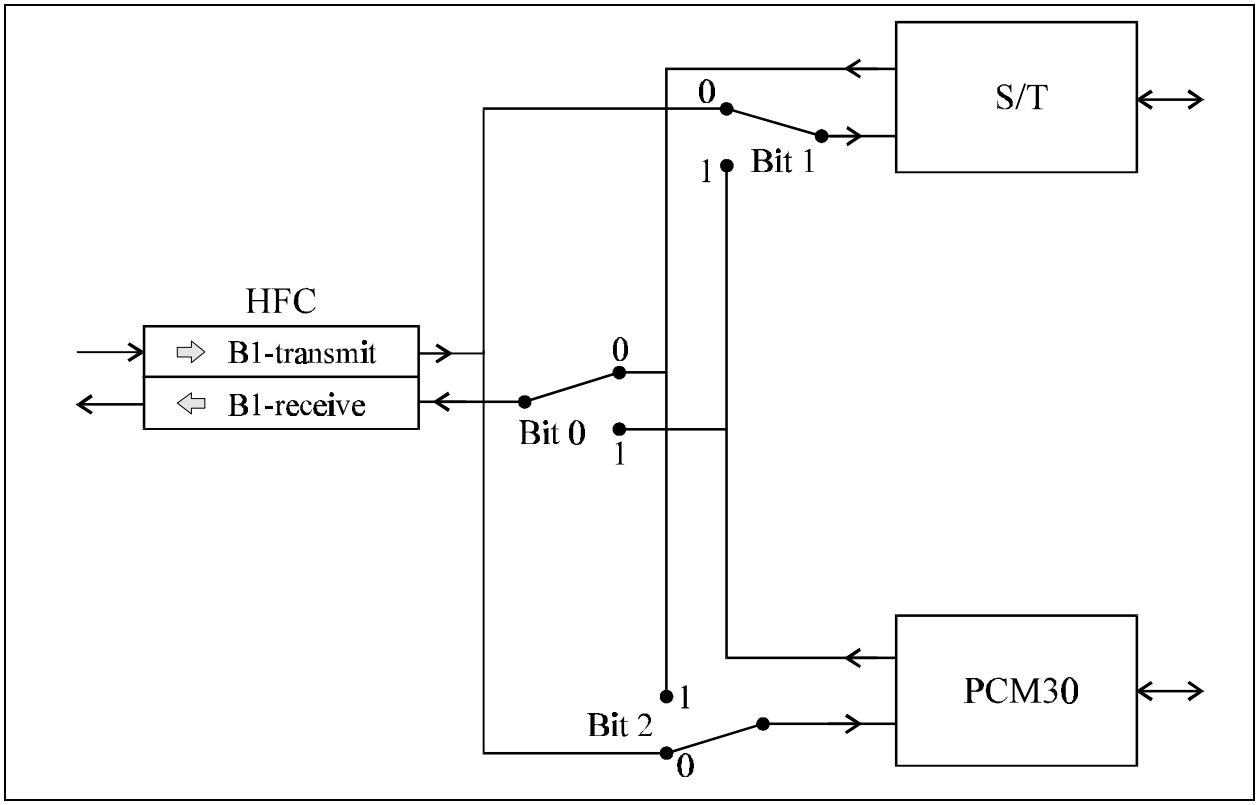


Figure 7: Function of the CONNECT register bits 0..2

4.4 Register bit description of interrupt, status and control registers

Name		Bits	r/w	Function
CIRM	(18h)	2..0	w	select IRQ channel in PC mode '000' IRQ disable (reset default) '001' IRQ_A '010' IRQ_B '011' IRQ_C '100' IRQ_D '101' IRQ_E '110' IRQ_F '111' IRQ disable
		3	w	soft reset, similar as hardware reset; the registers CIP, CIRM and CTMT are not changed so selected I/O address is kept in ISA-PC mode. The reset is active until the bit is cleared. '1' activate reset '0' deactivate reset (reset default)
		4	w	select memory '0' 32k x 8 external RAM (reset default) '1' 8k x 8 external RAM
		7..5		ignored
CTMT	(19h)	0	w	HDLC/transparent mode for channel B1 '0' HDLC mode (reset default) '1' transparent mode
		1	w	HDLC/transparent mode for channel B2 '0' HDLC mode (reset default) '1' transparent mode
		2		ignored
		4, 3	w	select timer and watchdog timer watchdog '00' 25ms 50ms '01' 50ms 100ms '10' 400ms 800ms '11' 800ms 1600ms
		5	w	timer/watchdog reset mode '0' reset timer/WD by CTMT bit 7 (reset default) '1' automatically reset timer/WD at each access to HFC-S

Name		Bits	r/w	Function
CTMT	(19h)	6		ignored
		7	w	reset timer/WD '1' reset timer/WD The bit is automatically cleared.
INT_M1	(1Ah)	0	w	interrupt mask for channel B1 in transmit direction
		1	w	interrupt mask for channel B2 in transmit direction
		2	w	interrupt mask for channel D in transmit direction
		3	w	interrupt mask for channel B1 in receive direction
		4	w	interrupt mask for channel B2 in receive direction
		5	w	interrupt mask for channel D in receive direction
		6	w	interrupt mask for state change of TE/NT state machine
		7	w	interrupt mask for timer

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits t o '0'.

INT_M2	(1Bh)	0	w	interrupt mask for BUSY/NOBUSY transition
		1		must be '0'
		2	w	in 64 kbit/s mode: must be '0' in 56 kbit/s mode: value of the LSB in 7-bit mode
		3	w	enable for interrupt output ('1' = enable)
		4	w	56 kbit/s mode selection bit for B1-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		5	w	56 kbit/s mode selection bit for B2-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		6	w	'1' Data inverted for B1-channel '0' Data not inverted for B1-channel (reset default)
		7	w	'1' Data inverted for B2-channel '0' Data not inverted for B2-channel (reset default)

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits to '0'.

Name		Bits	r/w	Function
INT_S1	(1Eh)	0	r	B1-channel interrupt status in transmit direction
		1	r	B2-channel interrupt status in transmit direction in HDLC mode: '1' a complete frame was transmitted, the frame counter F2 was incremented in transparent mode, external RAM 32K x 8: '1' bit12 in Z2 counter changed from '0' to '1' in transparent mode, external RAM 8K x 8: '1' bit10 in Z2 counter changed from '0' to '1'
		2	r	D-channel interrupt status in transmit direction '1' a complete frame was transmitted, the framecounter F2 was incremented
		3	r	B1-channel interrupt status in receive direction
		4	r	B2-channel interrupt status in receive direction in HDLC mode: '1' a complete frame was transmitt ed, the frame counter F1 was incremented in transparent mode, external RAM 32K x 8: '1' bit12 in Z1 counter changed from '0' to '1' in transparent mode, external RAM 8K x 8: '1' bit10 in Z1 counter changed from '0' to '1'
		5	r	D-channel interrupt status in receive direction '1' a complete frame was received, the frame counter F1 was incremented
		6	r	TE/NT state machine interrupt status '1' state of state machine has changed
		7	r	timer interrupt status '1' timer is elapsed

☝ **important!**
Reading the INT_S1 register resets all active read interrupts. New interrupts may occur during read. These interrupts are reported at the next read of INT_S1.
The interrupt output goes inactive during the read of INT_S1. If interrupts occur during this read the interrupt line goes active immediately after the read is finished. So processors with level or transition triggered interrupt inputs can be connected.

Name		Bits	r/w	Function
STATUS	(1Ch)	0	r	BUSY/NOBUSY status '1' the HFC-S is in BUSY state '0' the HFC-S is in NOBUSY state, access on all FIFO functions is now possible
		1	r	unused, '0'
		2	r	BUSY/NOBUSY transition interrupt status '1' the HFC-S has changed from BUSY to NOBUSY state, access on all FIFO functions is now possible This bit is reset by a read of INT_S1.
		3	r	unused, '0'
		4	r	timer status '0' timer not elapsed '1' timer elapsed
		5	r	TE/NT state machine interrupt state '1' state of state machine has changed
		6	r	FRAME interrupt has occured (any data channel interrupt) all masked D-channel and B-channel interrupts are "ored"
		7	r	ANY interrupt all masked interrupts are "ored"

Reading the STATUS register clears no bit.

STATUS_DISBUSY	(1Dh)	r	see STATUS register All bits are the same as in the STATUS register.

All processor modes:
Reading STATUS_DISBUSY register delays the transition from nobusy to busy until any other register of the HFC-S is accessed (see Figure 5 on page 26).
This register should be checked for nobusy before accessing any busy-critical register to avoid a transition from nobusy to busy during a FIFO register access, which may destroy register values.
Busy-critical register are all FIFO registers, the data register of the S/T-part B1_REC/B1_SEND and B2_REC/B2_SEND, D_REC/D_SEND and the B-channel data register B1_D and B2_D of the PCM30 bus part.

ISA-PC mode:
It is possible to read the STATUS_DISBUSY register in ISA-PC mode directly by a READ operation to the port address with SA0='1', but it is necessary to enable the HFC-S going into busy cycle again after a data port access with SA0='0'.

5 Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Rating
Supply voltage	V_{CC}	-0.3V to +7.0V
Input voltage	V_I	-0.3V to V_{CC} + 0.3V
Output voltage	V_O	-0.3V to V_{CC} + 0.3V
Operating temperature	T_{opr}	-40°C to +85°C
Storage temperature	T_{stg}	-55°C to +150°C

Recommended operating conditions for TTL and CMOS interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.
Supply voltage	V_{CC}		3.0V	5.0V	5.25V
Supply current normal power down	I_{CC}	f_{CLK}=12.288MHz running oscillator: oscillator stopped:		 20 mA 6 mA	
Operating temperature	T_{opr}		0°C		+70°C

Electrical characteristics

V_{CC} = 4.75V to 5.25V (TTL), V_{CC} = 4.5V to 5.5V (CMOS), T_{opr} = -10°C to +70°C

Parameter	Symbol	Condition	TTL level			CMOS level		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Input LOW voltage	V_{IL}				0.8V			1.5V
Input HIGH voltage	V_{IH}	Schmitt input buffer	2.0V			3.5V		
Input HIGH threshold voltage	V_{T+}				2.2V			3.7V
Input LOW threshold voltage	V_{T-}		0.5V			1.0V		
Hysteresis voltage	V_H		0.2V			0.4V		
Output LOW voltage	V_{OL}				0.4V			0.4V
Output HIGH voltage	V_{OH}		4.0V			4.0V		
Output leakage current	$\lvert I_{OZ} \rvert$	High Z			10µA			10µA
Pull-up resistor input current	$\lvert I_{IL} \rvert$	V_I = 0V	8.0µA		60µA	8.0µA		60µA

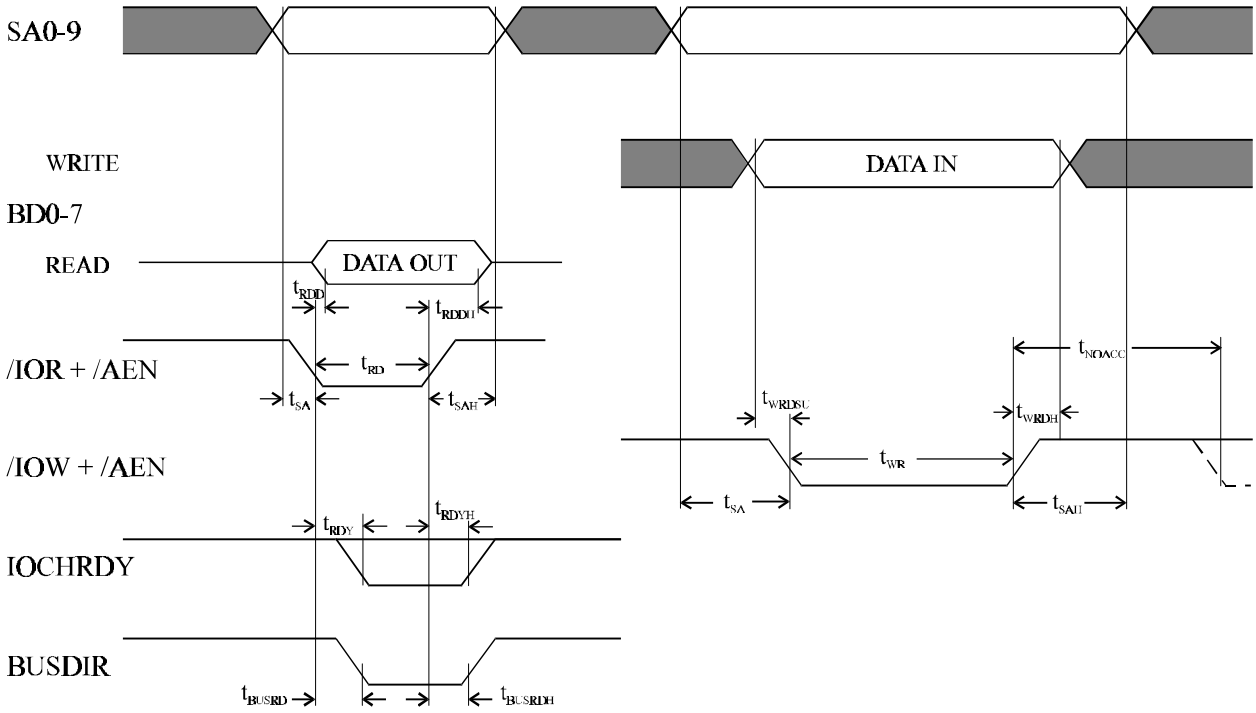
I/O Characteristics

Input	Interface Level
IIOSEL0-3	TTL, internal pull-up resistor
SA0-9	TTL
/AEN	TTL
/IOR	TTL
/IOW	TTL
BD0-7	TTL
ALE	TTL
SRD0-7	TTL
C4IO	TTL, internal pull-up resistor
F0IO	TTL, internal pull-up resistor
STIO1-2	TTL, internal pull-up resistor
/IRQ_P	open drain, external pull up resistor required
IRQ_P	open source, external pull down resistor required
/WD_RES	open drain, external pull up resistor required
WD_RES	open source, external pull down resistor required
RESET	CMOS Schmitt Trigger

	Driver Capability		
	Low		High
Output	0.4V	0.6V	V_{CC} - 0.4V
IOCHRDY	12mA		
BD0-7	18mA	24mA	8mA
BUSDIR	4mA		2mA
TX2_HI	4mA		2mA
/TX1_LO	12mA		
/TX_EN	4mA		2mA
/TX2_LO	12mA		
TX1_HI	4mA		2mA
SRD0-7	4mA		2mA
SRA0-14	4mA		2mA
/SRCS	4mA		2mA
/SRWE	4mA		2mA
C4IO	6mA		3mA
F0IO	6mA		3mA
STIO1-2	6mA		3mA
F1_A-B	6mA		3mA
IRQA-F	6mA		3mA

6 Timing characteristics

6.1 ISA-PC bus or processor access

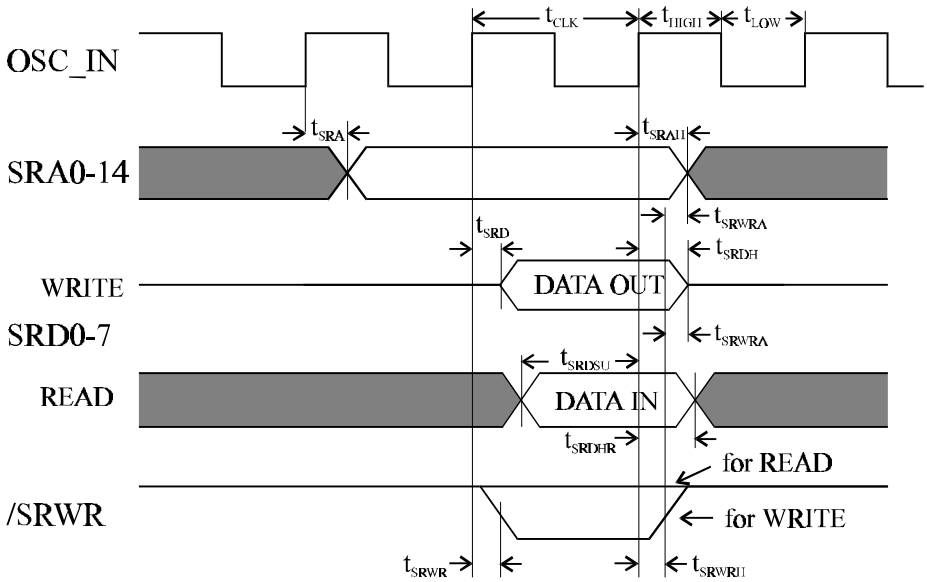


Timing Diagram 1: ISA-PC bus or processor access

SYMBOL	CHARACTERISTICS	MIN.	MAX.
t_{RDD}	/IOR Low to Read Data Out Time	3ns	25ns
t_{RDDH}	/IOR High to Data Buffer Turn Off Time	2ns	15ns
t_{SA}	Address to /IOR or /IOW Low Setup Time	20ns	–
t_{SAH}	Address Hold Time after /IOR or /IOW High	20ns	–
t_{RD}	Read Time	2 x t_{CLK}	∞
t_{WR}	Write Time	2 x t_{CLK}	∞
t_{WRDSU}	Write Data Setup Time to /IOW Low	5ns	∞
t_{WRDH}	Write Data Hold Time from /IOW High	10ns	–
t_{RDY}	Delay Time from /IOR or /IOW Low to IOCHRDY Low	3ns	30ns
t_{RDYH}	Delay Time from /IOR Low or /IOW High to IOCHRDY High	3ns	30ns
t_{BUSRD}	Delay Time from /IOR Low to BUSDIR Low	3ns	25ns
t_{BUSRDH}	Delay Time from /IOR High to BUSDIR High	2ns	15ns
t_{NOACC} *)	Time no access is possible	4 x t_{CLK}	–

*) only in processor mode

6.2 SRAM access



Timing Diagram 2: SRAM access

SYMBOL	CHARACTERISTICS	MIN.	MAX.
f_{CLK}	Clock frequency	7.68MHz	12.288MHz
$\Delta f_{CLK} / f_{CLK}$	Relative Clock frequency deviation	0	$\pm 10^{-4}$
t_{LOW} *)	Clock Low Level Width	30ns	–
t_{HIGH} *)	Clock High Level Width	30ns	–
t_{CLK}	Clock Cycle Time	1/ f_{CLK}	–
t_{SRA}	Address Stable after Clock ↑	5ns	70ns
t_{SRAH}	Address Stable Hold Time after Clock ↑	5ns	–
t_{SRD}	Data Out Stable after Clock ↑	15ns	50ns
t_{SRDH}	Data Out Stable Hold Time after Clock ↑	5ns	–
t_{SRDSU}	Data In Setup Time to Clock ↑	20ns	–
t_{SRDHR}	Data In Hold Time after Clock ↑	0ns	–
t_{SRWR}	Delay Time Clock ↑ to /SRWR Low	2ns	40ns
t_{SRWRH}	Delay Time Clock ↑ to /SRWR High	5ns	40ns
t_{SRWRA}	Data and Address Hold Time after /SRWR ↑	1ns	–

*) Clock should be symmetrical so $t_{LOW} = t_{HIGH}$

6.3 PCM30 bus clock and data alignment for Mitel ST™ bus

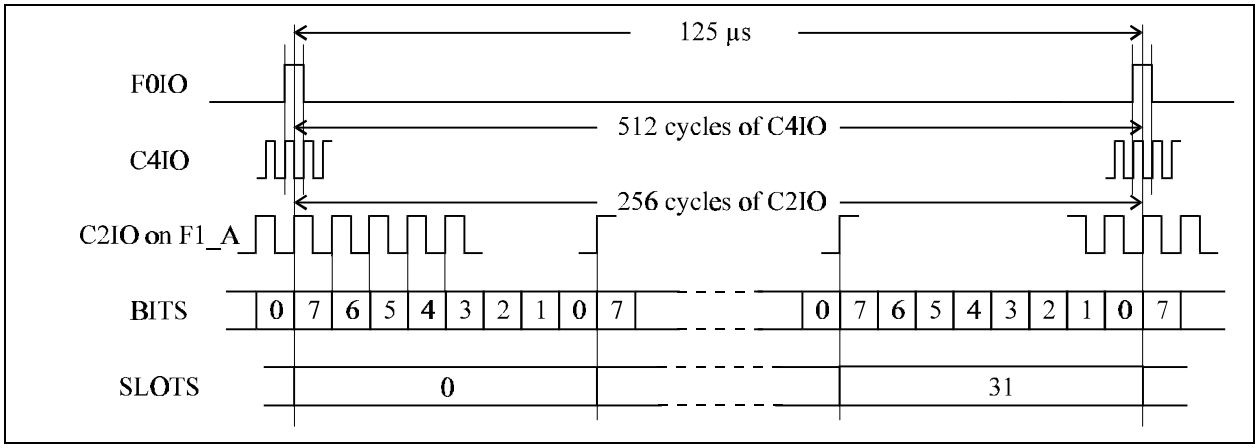
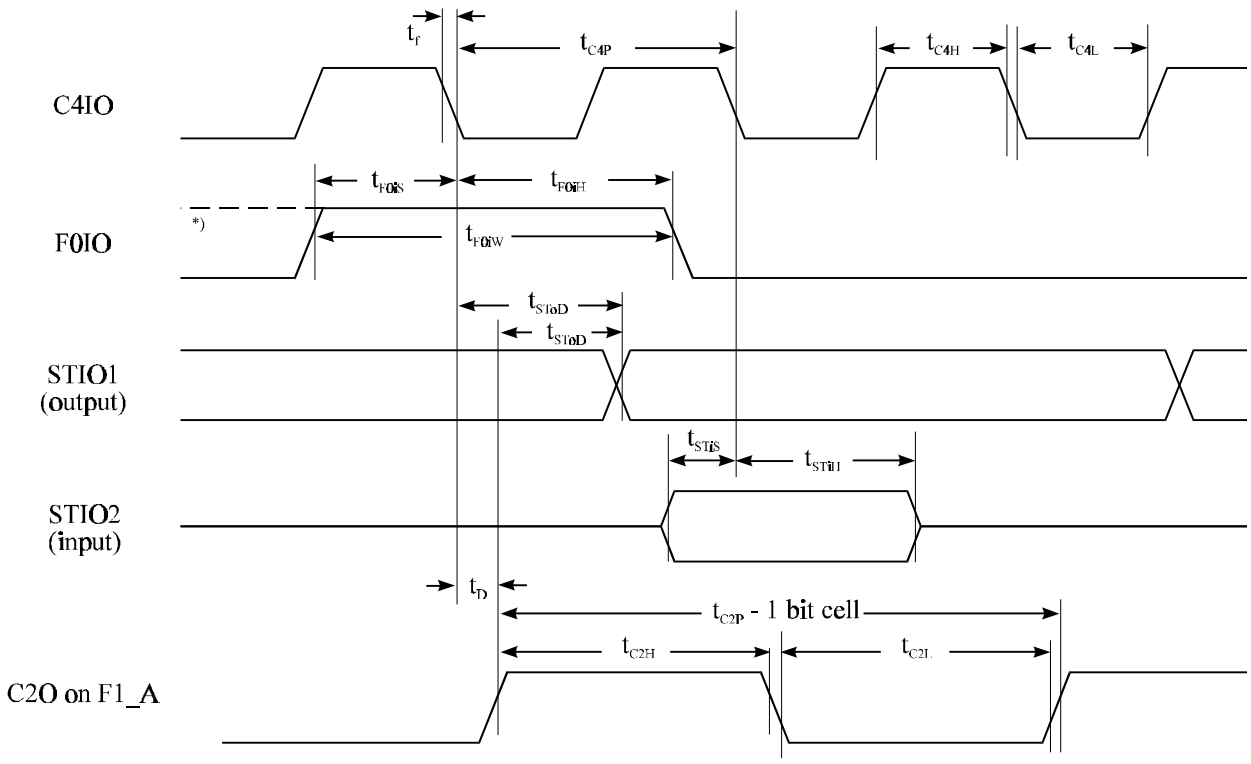


Figure 8: PCM30 bus clock and data alignment

6.4 PCM30 timing



Timing Diagram 3: PCM30 timing

*) F0IO starts one C4IO clock earlier if bit 3 in MST_MODE register is set. If this bit is set F0IO is also awaited one C4IO clock cycle earlier.

SYMBOL	CHARACTERISTICS	MIN.	MAX
t_{C4P}	Clock C4IO period (4.096 MHz)	243.9 ns	244.4 ns
t_{C4H}	Clock C4IO High Width	110 ns	134 ns
t_{C4L}	Clock C4IO Low Width	110 ns	134 ns
t_{C2P}	Clock C2O Period	487.8 ns	488.8 ns
t_{C2H}	Clock C2O High Width	220 ns	268 ns
t_{F0iS}	F0IO Setup Time	50 ns	150 ns
t_{F0iH}	F0IO Hold Time	50 ns	150 ns
t_{F0iW}	F0IO Width	200 ns	300 ns
t_{SToD}	STIO1 Delay Level 1 Output	20 ns	125 ns
t_{SToD}	STIO1 Delay Level 2 Output	20 ns	125 ns
t_{STiS}	STIO2 Set Up Time	30 ns	
t_{STiH}	STIO2 Hold Time	2 ns	30ns

All specifications are for 2.048 Mb/s Streams and f_{CLK} = 12.288 Mhz.

7 S/T interface circuitry

In order to comply to the physical requirements of ITU-T recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the HFC-S needs some additional circuitry, which are shown in the following figures.

7.1 External receiver circuitry

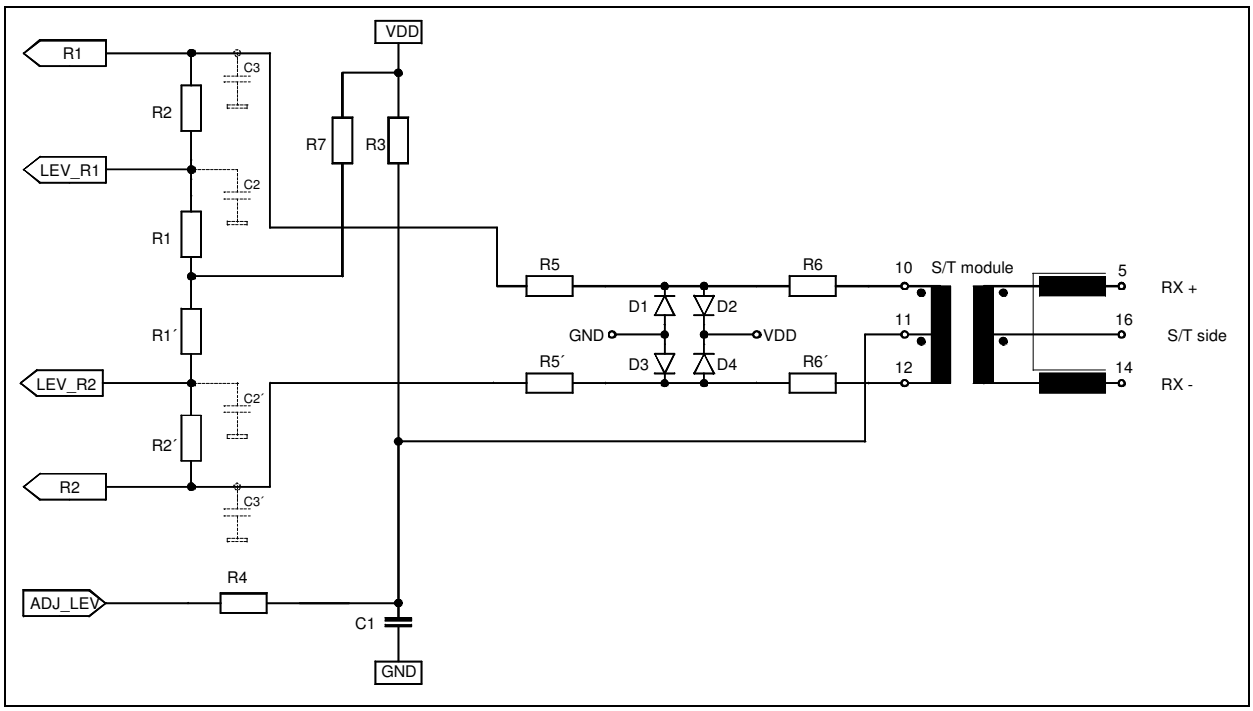


Figure 9: External receiver circuitry

Part list

R1, R1'	33 kΩ	R4	3.9 kΩ
R2, R2'	100 kΩ	R5, R5'	4.7 kΩ
R3	1 MΩ	R6, R6'	4.7 kΩ
R7	1.8 MΩ		

C1	47 nF
C2, C2' optional	22 - 47 pF
C3, C3' optional	10 pF

C2 - C3' are for reduction of high frequency input noise and should be located as close as possible to the HFC-S.

D1, D2	1N4148 or LL4148
D3, D4	1N4148 or LL4148

S/T module	see Table 4 on page 46

VDD	+5 V (if VDD ≠ +5V R7 and R3 must be changed)

7.2 External transmitter circuitry

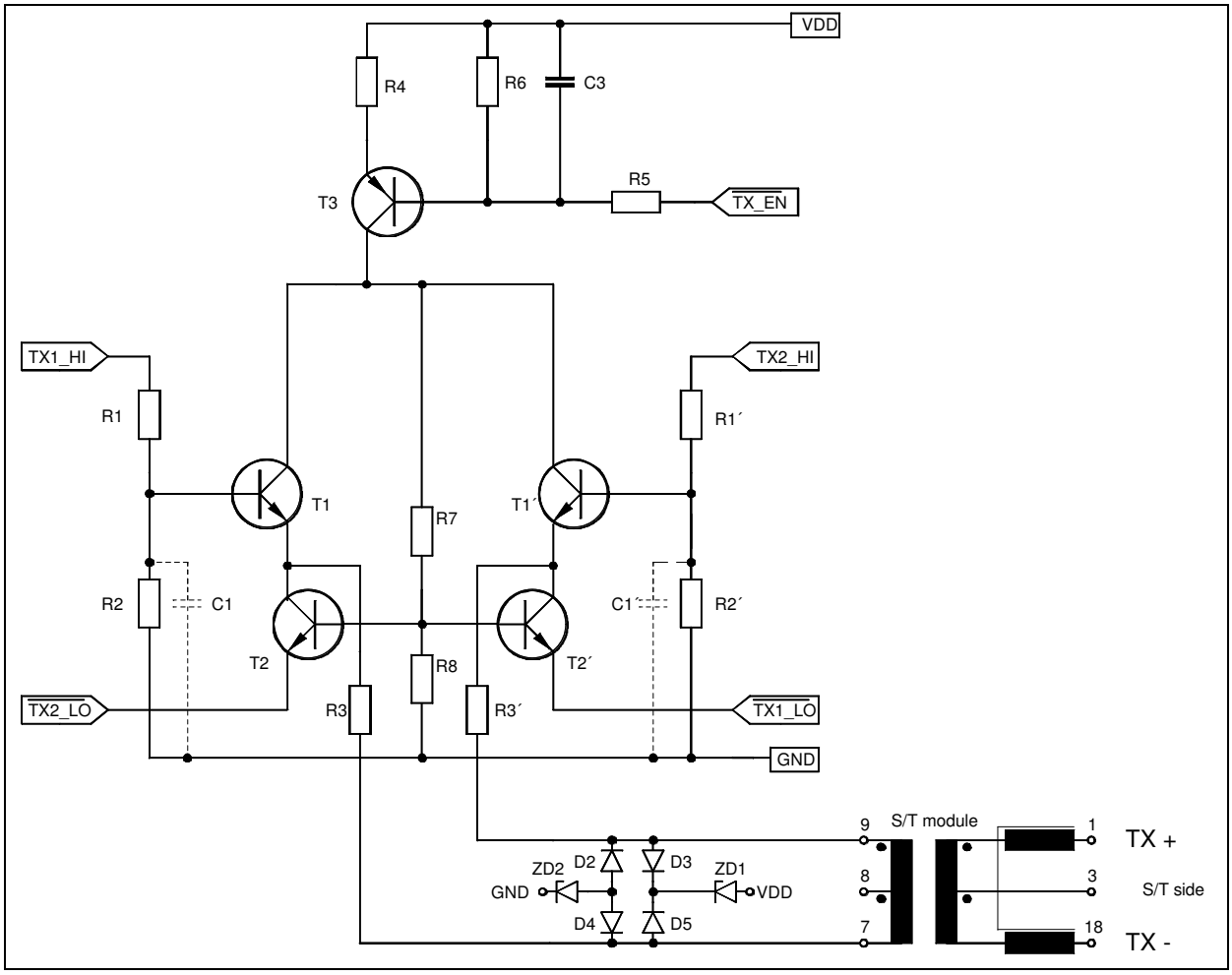


Figure 10: External transmitter circuitry

Part List

R1	2.2 kΩ ± 1%		
R2	3.0 kΩ ± 1%	D2, D3,	
R3, R3' *)	18 Ω	D4, D5	1N4148 or LL4148
R4	100 Ω	ZD1, ZD2	Z-Diode 2.7 V (e. g. BZV 55C 2V7)
R5	5.6 kΩ		
R6	3.3 kΩ	T1, T1',	
R7	3.3 kΩ	T2, T2'	BC550C, BC850C or similar
R8	3.3 kΩ	T3	BC560C, BC860C or similar
C1, C1'	10 - 33 pF (optional)		
C3	470 pF		

S/T module see Table 4 on page 46
VDD +5 V (if VDD ≠ +5V R1/R1' and R2/R2' must be changed)

*) value is depending on the used S/T module

S/T module part number	manufacturer
APC 56624 APC 42624	Advanced Power Components 47 Riverside Medway City Estate Rochester Kent ME2 4DP United Kingdom Phone: +44 1634-290588 Fax: +44 1634-290591
543 76 009 00	Vogt electronic AG Erlautal 7 D-94130 Obernzell Germany Phone: +49 8591/ 17-0 Fax: +49 8591/ 17-240
FE 8131-55Z	FEE GmbH **Singapore** Phone: +65 741-5277 Fax: +65 741-3013 **Bangkok** Phone: +662 718-0726-30 Fax: +662 718-0712 **Germany** Phone: +49 6106-82980 Fax: +49 6106-829898
VAC L5051-X014-80	VAC GmbH Postfach/P.O.B. 2253 D-63412 Hanau Germany Phone: +49 6181/ 38-0 Fax: +49 6181/ 38-2645
PT5121	Valor Electronics, Inc. **Asia** Phone: +852 2333-0127 Fax: +852 2363-6206 **North America** Phone: +1 619 537-2500 Fax: +1 619 537-2525 **Europe** Phone: +49 89-4802823 Fax: +49 89-484743
UT 21624	UMEC GmbH Kreuzenstrasse 80 74076 Heilbronn Germany Phone: +49 7131-7617-0 Fax: +49 7131-7617-20

Table 4: S/T module part numbers and manufacturer

7.3 Oscillator circuitry

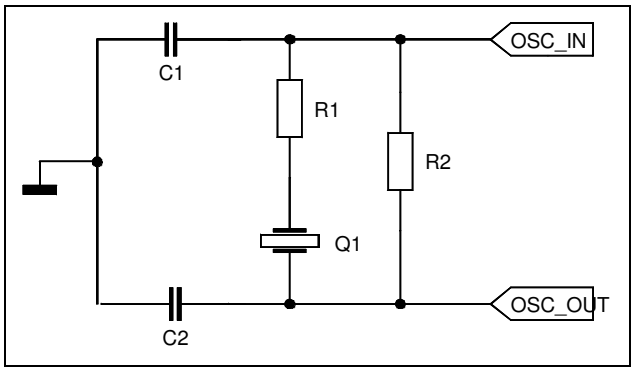


Figure 11: Oscillator Circuitry

Part list:

Q1	12.288 MHz quartz
R1	330 Ω
R2	1 MΩ
C1, C2	47 pF

The values of C1, C2 and R1 depend on the used quartz.

For a load-free check of the oscillator frequency the C4O clock of the PCM30 bus should be measured (HFC-S as master, S/T interface deactivated, 4.096 MHz frequency intented on the C4IO).

8 State matrices for NT and TE

8.1 S/T interface activation/deactivation layer 1 for finite state matrix for NT

State name / State number / INFO sent / Event	Reset	Deactive	Pending activation	Active	Pending deactivation
State number	G0	G1	G2	G3	G4
INFO sent	INFO 0	INFO 0	INFO 2	INFO 4	INFO 0
Activate request	G2 (Note 1)	G2 (Note 1)	|	|	G2 (Note 1)
Deactivate request	—	|	Start timer T2 G4	Start timer T2 G4	|
Expiry T2 (Note 2)	—	—	—	—	G1
Receiving INFO 0	—	—	—	G2	G1
Receiving INFO 1	—	G2 (Note 1)	—	/	—
Receiving INFO 3	—	/	G3 (Note 1)	—	—
Lost framing	—	/	/	G2	—

Table 5: Activation/deactivation layer 1 for finite state matrix for NT

— No state change
/ Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
| Impossible by the definition of the physical layer service

Notes

Note 1: Timer 1 (T1) is not implemented in the HFC-S and must be implemented in software.

Note 2: Timer 2 (T2) prevents unintentional reactivation. Its value is 32ms (256 x 125µs). This implies that a TE has to recognize INFO 0 and to react on it within this time.

8.2 Activation/deactivation layer 1 for finite state matrix for TE

Event \ State name		Reset	Sensing	Deactivated	Awaiting signal	Identifying input	Synchronized	Activated	Lost framing
State number		F0	F2	F3	F4	F5	F6	F7	F8
Info sent		INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
State machine release (Note 1)		F2	/	/	/	/	/	/	/
Activate Request	Receiving any signal	—	|	F5	|	|	—	|	—
	Receiving INFO 0	—	|	F4	|	|	—	|	—
Expiry T3 (Note 5)		—	/	—	F3	F3	F3	—	—
Receiving INFO 0		—	F3	—	—	—	F3	F3	F3
Receiving any signal (Note 2)		—	—	—	F5	—	/	/	—
Receiving INFO 2 (Note 3)		—	F6	F6	F6	F6	—	F6	F6
Receiving INFO 4 (Note 3)		—	F7	F7	F7	F7	F7	—	F7
Lost framing (Note 4)		—	/	/	/	/	F8	F8	—

Table 6: Activation/deactivation layer 1 for finite state matrix for TE

— No change, no action
| Impossible by the definition of the layer 1 service
/ Impossible situation

Notes

Note 1: After reset the state machine is fixed to F0.

Note 2: This event reflects the case where a signal is received and the TE has not (yet) determined wether it is INFO 2 or INFO 4.

Note 3: Bit- and frame-synchronisation achieved.

Note 4: Loss of Bit- or frame-synchronisation.

Note 5: Timer 3 (T3) is not implemented in the HFC-S and must be implemented in software.

9 Binary organisation of the frame

The frame structures are different for each direction of transmission. Both structures are illustrated in Figure 12.

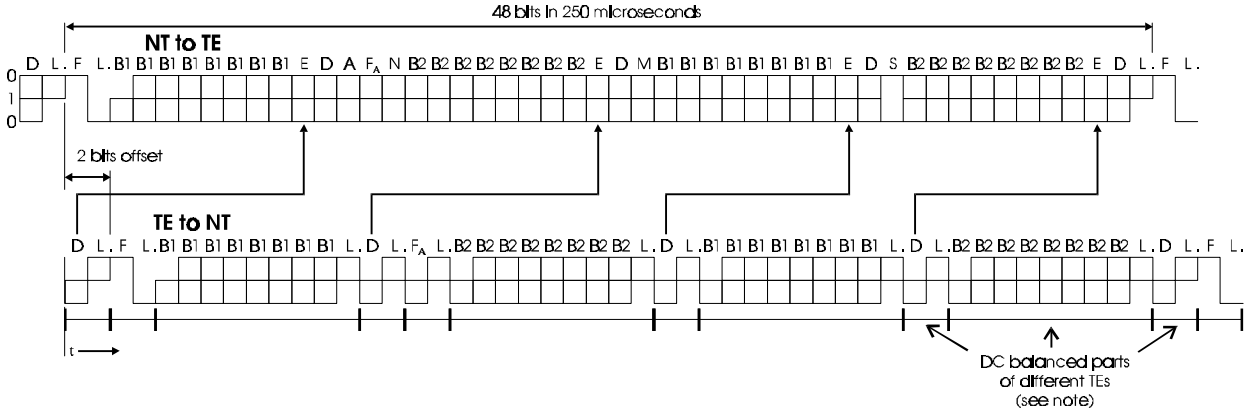


Figure 12: Frame structure at reference point S and T

F	Framing bit	N	Bit set to a binary value N = $\overline{F}_A$ (NT to TE)
L	D.C. balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit	S	S-channel bit
M	Multiframing bit		

☝ **note!**
Lines demarcate those parts of the frame that are independently d.c.-balanced.
The F_A bit in the direction TE to NT is used as Q bit in every fifth frame if S/Q bit transmission is enabled (see SCTRL register).
The nominal 2-bit offset is as seen from the TE. The offset can be adjusted with the CLKDEL register in TE mode. The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.
HDLC-B-channel data start with the LSB, PCM-B-channel data start with the MSB.

10 Clock synchronisation

10.1 Clock synchronisation in NT-mode

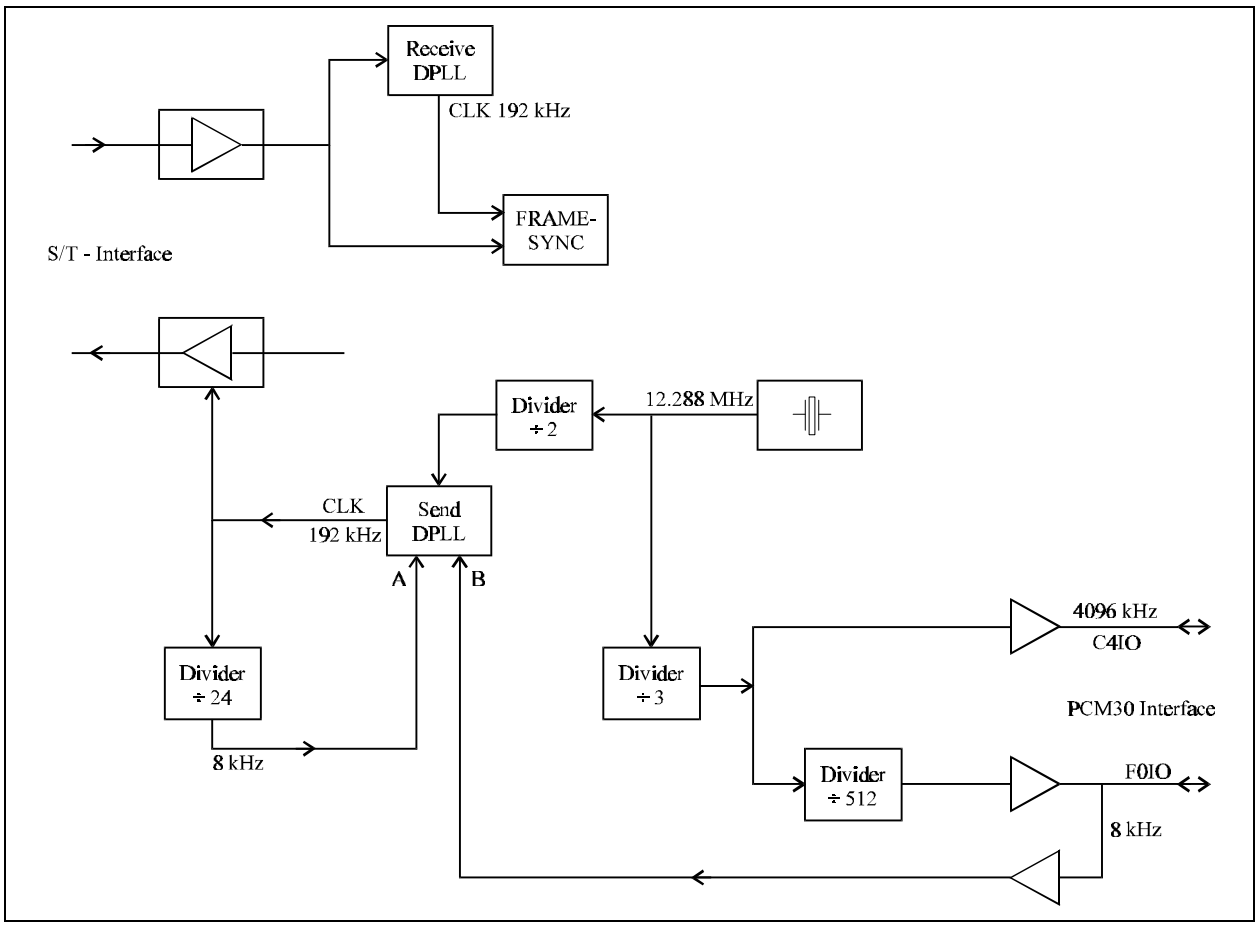


Figure 13: Clock synchronisation in NT-mode

10.2 Clock synchronisation in TE-mode

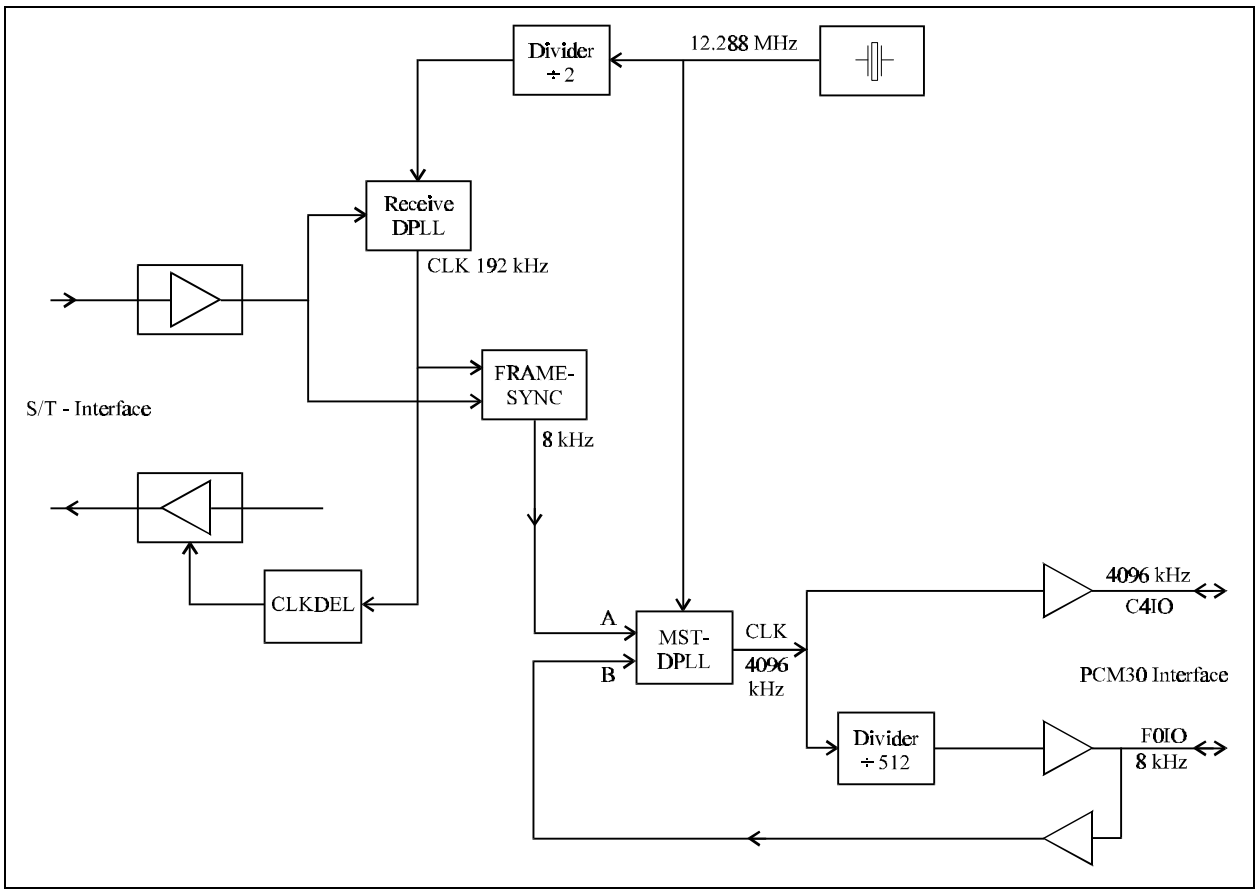


Figure 14: Clock synchronisation in TE-mode

The C4IO clock is adjusted in the 31th time slot twice for one half clock cycle.

11 HFC-S package dimensions

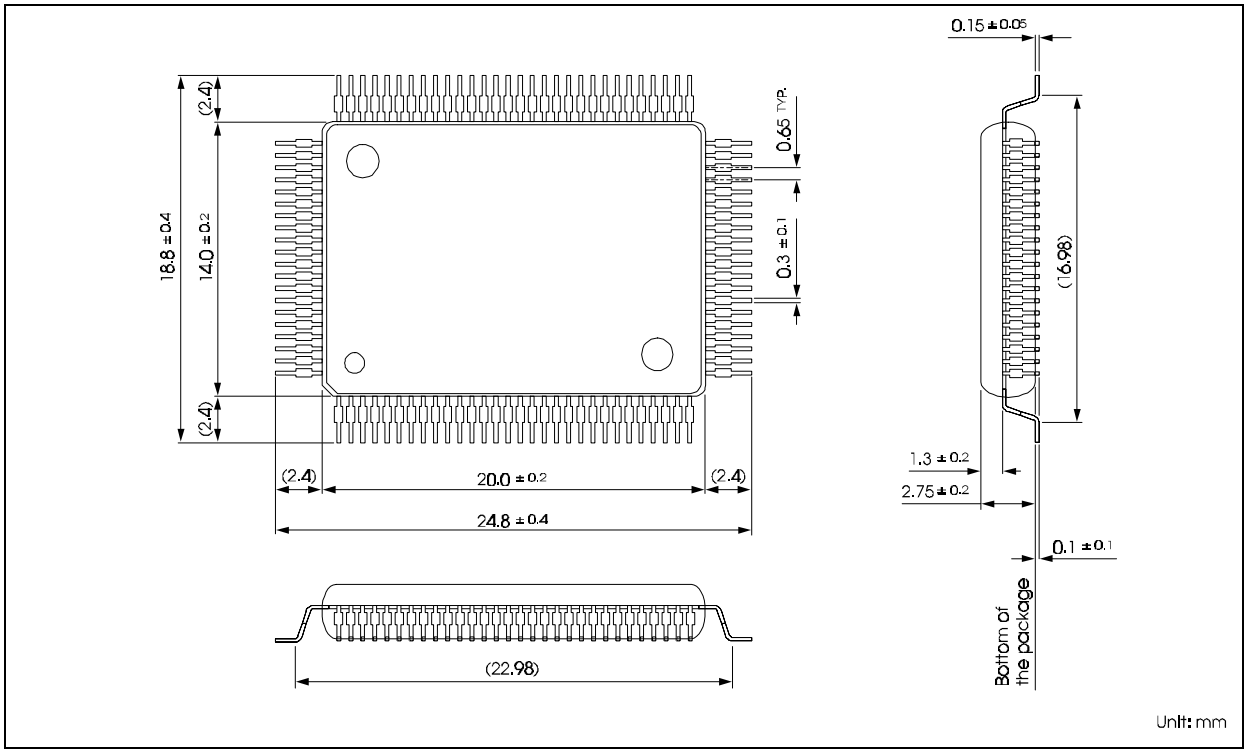
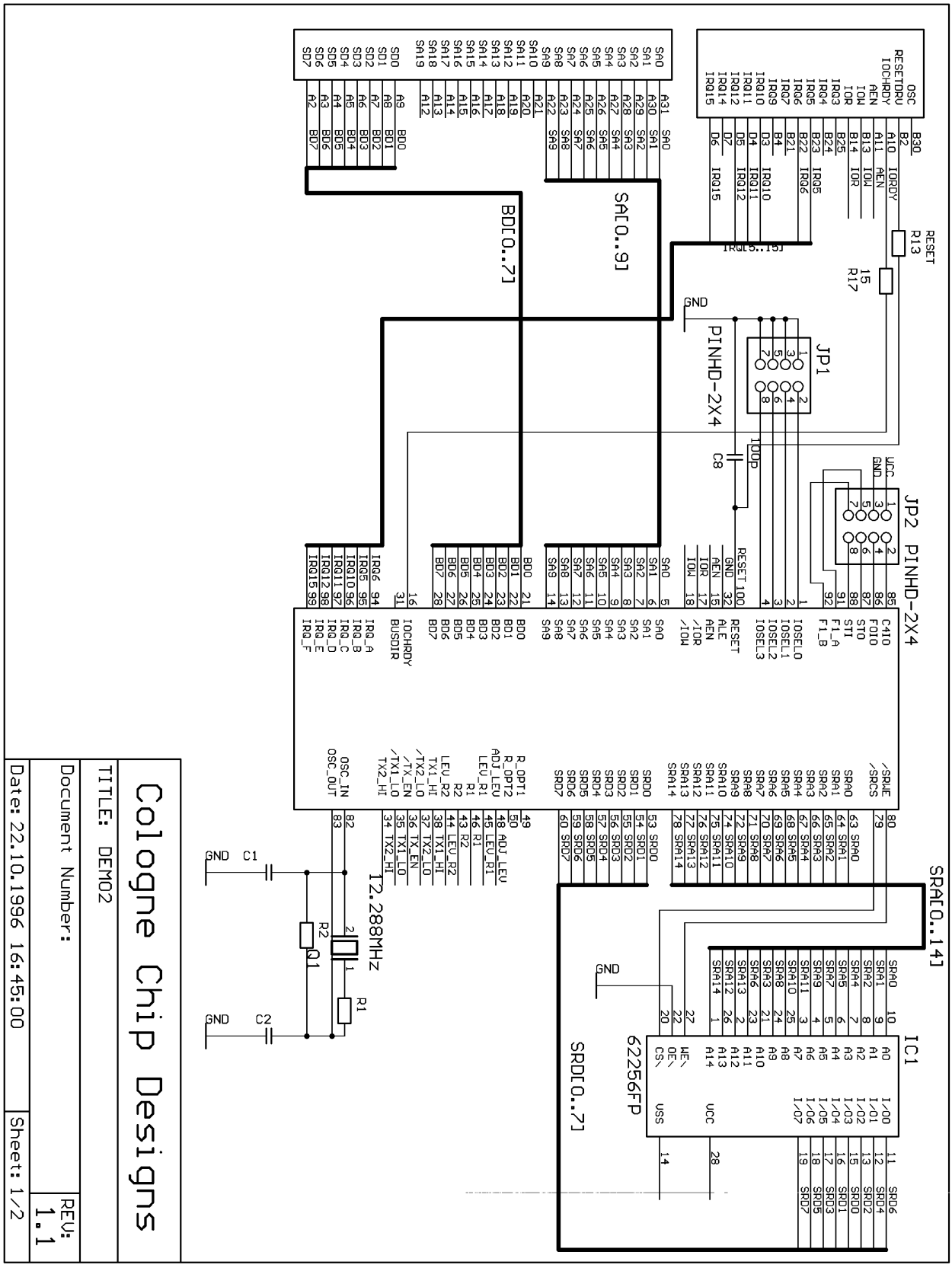
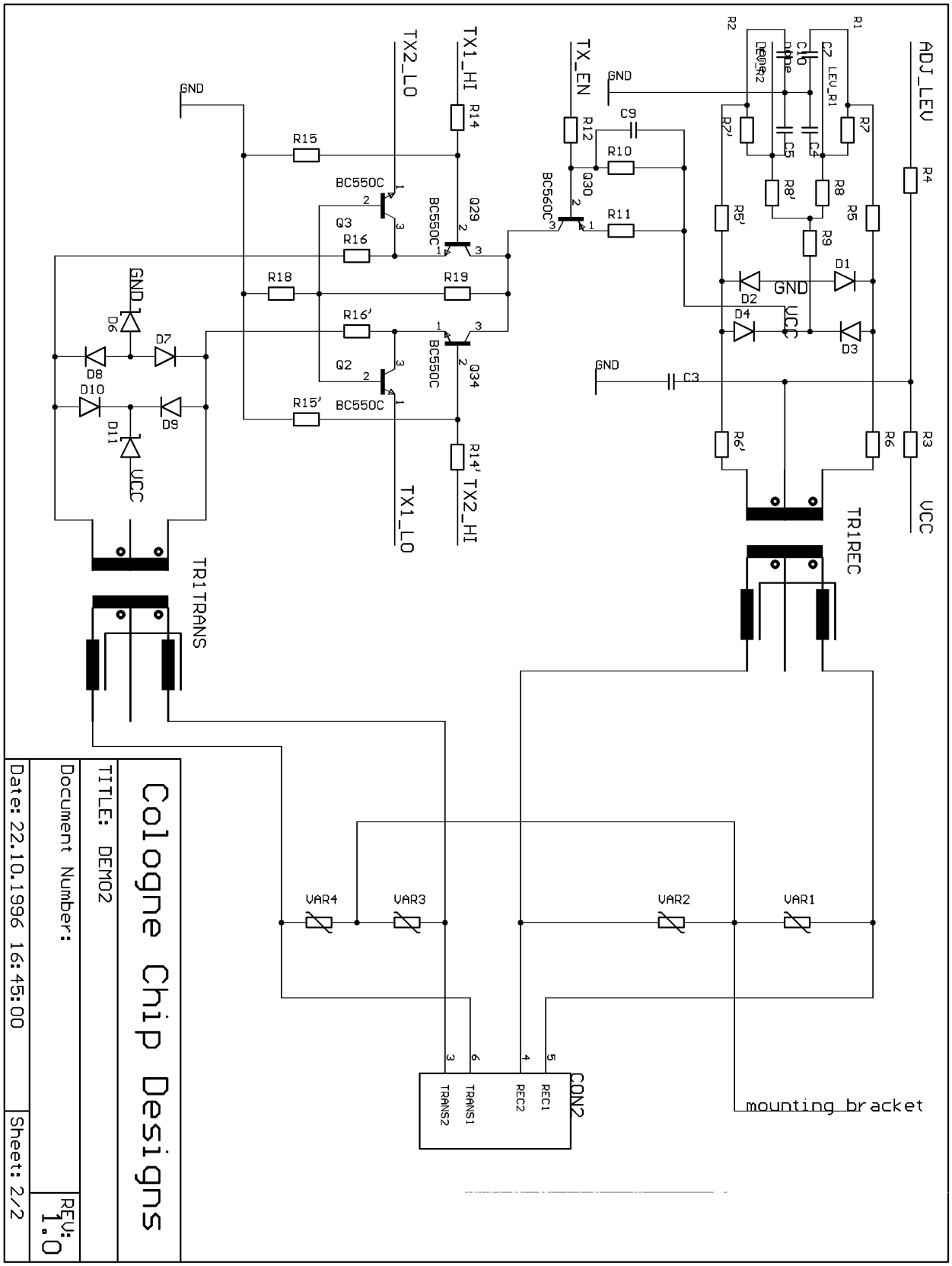


Figure 15: HFC-S package dimensions

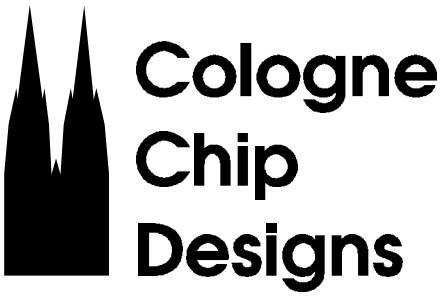
12 ISDN PC card sample circuitry with HFC-S




TX2_LO
TX1_HI
TX_EN
ADJ_LEV
GND
R15
R14
R12
R10
R11
R7
R4
C9
C10
C7
C5
C2
LEV_R1
R2
R1
R2'
R8'
R8
R5'
R5
R9
D1
D2
D4
D3
VCC
BC550C
Q3
Q29
Q30
R16
R18
R19
R16'
Q2
Q34
R15'
R14'
TX1_LO
TX2_HI
D6
D7
D8
D10
D11
D9
C3
R6'
R6
R3
TR1TRANS
TR1REC
VAR4
VAR3
VAR2
VAR1
CON2
TRANS2
TRANS1
REC2
REC1
mounting bracket
Cologne Chip Designs
TITLE: DEMO2
Document Number:
Date: 22.10.1996 16:45:00
Sheet: 2/2
REV: 1.0

Part List

Part	Value
C1	47pF
C2	47pF
C3	47nF
C4	none
C5	none
C7	none
C8	1nF
C9	470pF
C10	none
CB1	47nF
CB2	47nF
CB3	47nF
CB4	47nF
CB5	47nF
CB6	47nF
CB7	47nF
CB8	33µF
CB9	33µF
CON2	WESTERN
CON3	ISA
D1	LL4148
D2	LL4148
D3	LL4148
D4	LL4148
D6	2V7
D7	LL4148
D8	LL4148
D9	LL4148
D10	LL4148
D11	2V7
IC1	62256FP
IC1	HFC-S
JP1	PINHD-2X4
JP2	PINHD-2X4
Q1	12.288MHz
Q2	BC850C
Q3	BC850C
Q29	BC850C
Q30	BC860C
Q34	BC860C
R1	330Ω
R2	1MΩ
R3	1MΩ
R4	3.9kΩ
R5	4.7kΩ
R5'	4.7kΩ
R6	4.7kΩ
R6'	4.7kΩ
R7	100kΩ
R7'	100kΩ
R8	33kΩ
R8'	33kΩ
R9	1.8MΩ
R10	3.3kΩ
R11	100Ω
R12	5.6kΩ
R13	100kΩ
R14	2.2kΩ ±1%
R14'	2.2kΩ ±1%
R15	3.0kΩ ±1%
R15'	3.0kΩ ±1%
R16	18Ω
R16'	18Ω
R17	15Ω
R18	3.3kΩ
R19	3.3kΩ
TR1	SOTR



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