Cologne Chip

HFC - S PCI A
ISDN 2BDS0

ISDN HDLC FIFO controller
with
S/T and PCI interface
and
U-chip support

January 2001

Revision History

Date	Remarks
Jan. 2001	Information added to section: TRM register bit description, GCI/IOM2 timing. Changes made on: ISDN PCI card for 3.3V power supply (no $D3_{cold}$ support) part list and ISDN PCI card for 3.3V power supply with $D3_{cold}$ support part list: RG3, RG4 renamed to RG1, RG2 to match with the schematics.
Oct. 2000	Changes made in section: Sample circuitries: ISDN PCI card for 3.3 and 5V power supply (auto detect) with $D3_{cold}$ support: connectors for alternative footprint removed.
May 2000	Information added to section: S/T module part numbers, Sample circuitries.
Jan. 2000	Section added: Register list. Information added to section: GCI frame structure, sample circuitries. Errors corrected in section: configuring test loops (register addresses corrected), register bit description (STATES register address corrected), Auxiliary port write access (data out is valid until the next write access is initiated).
Aug. 1999	Sections added: Power management support of HFC-S PCI A, configuring test loops. Information added in section: STATES register bit description, S/T interface activation / deactivation layer 1 for finite state matrix for NT.
Apr. 1999	Auxiliary port access timing diagrams added.
Mar. 1999	Changes made on: S/T module part numbers and manufacturers.

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- Single chip ISDN-S-controller with B- and D-channel HDLC support
- Independent Read and Write HDLC-Channels for 2 ISDN B-channels and one ISDN D-channel
- B1- and B2-channel transparent mode independently selectable
- FIFO-Memory-Window: 4x 7.5 KByte (B-channel) and 2x 512 Byte (D-channel)
- max. 31 HDLC frames (B-channel) and 15 HDLC frames (D-channel) per channel and direction in FIFO
- 56 kbit/s restricted mode for U.S. ISDN lines selectable
- full I.430 ITU S/T ISDN support in TE and NT mode
- B1+B2 HDLC mode
- PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for interface to U-chip or external codecs
- integrated PCI Spec. 2.2 bus interface (power management included, ACPI ready) for 3.3V and 5V bus signal environment
- direct access to PCM30 interface for tone synthetisation
- 3.3V and 5V supply voltage
- rectangular QFP 100 case

1 General description

The HFC-S PCI A is an ISDN S/T HDLC basic rate controller for so called „passive“ ISDN PC cards with integrated S/T interface and PCM30 highway interface. It is the first all in one solution for a PCI ISDN PC-card world wide with power management and Windows 98 support.

A 32Kbyte memory window of the PC is used for the deep FIFOs. Also an industrial standard serial interface for telecom peripheral ICs is implemented. Codecs are normally connected to this interface.

1.1 Applications

- ISDN PCI PC card

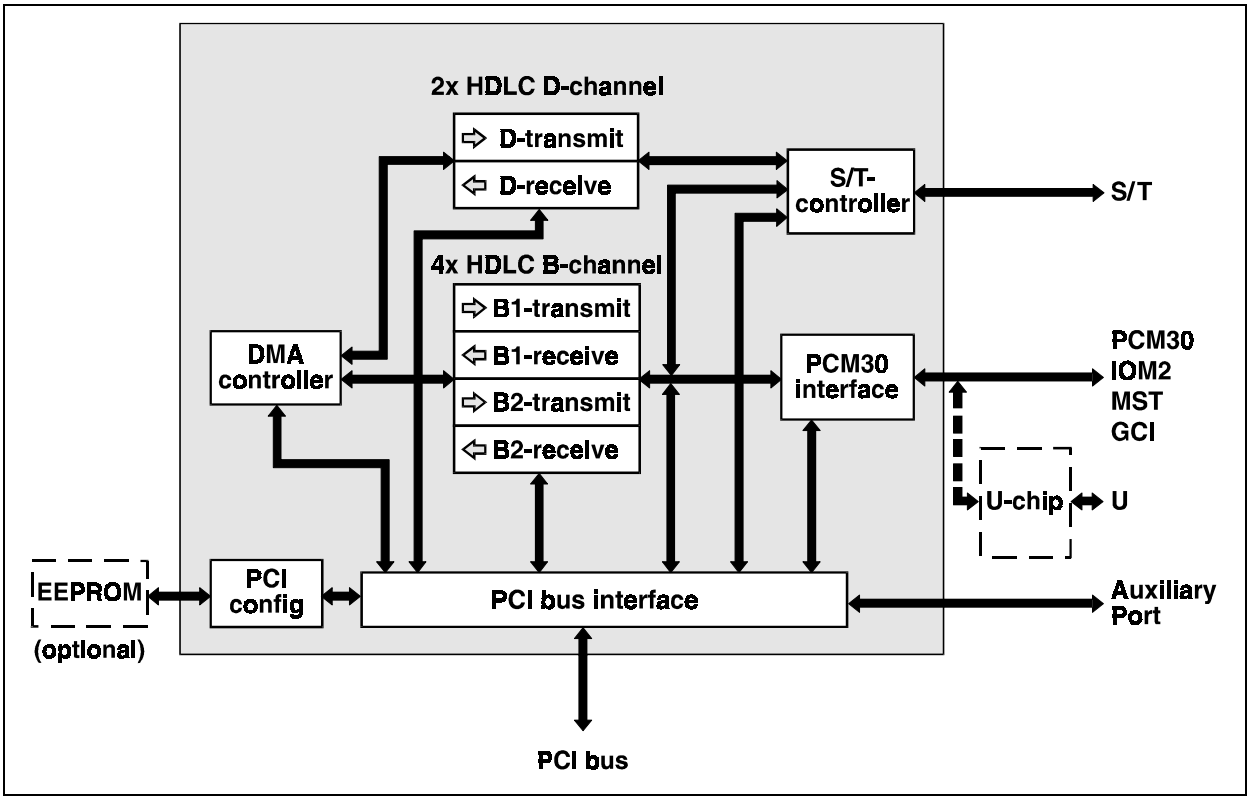


Figure 1: HFC-S PCI A block diagram

2 Pin description

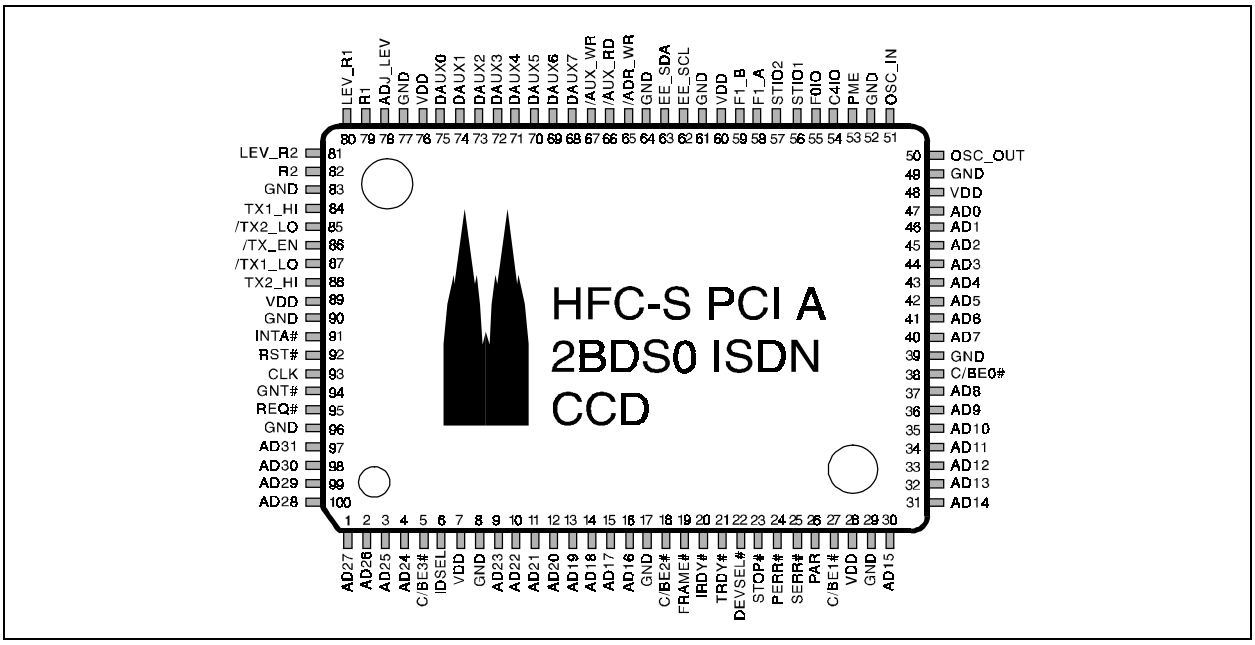


Figure 2: Pin Connection

2.1 PCI bus interface

For further information please refer to the PCI Local Bus Specification.

Pin No.	Pin Name	Input Output	Function
			PCI address bus
47	AD0	I/O	Address bit 0
46	AD1	I/O	Address bit 1
45	AD2	I/O	Address bit 2
44	AD3	I/O	Address bit 3
43	AD4	I/O	Address bit 4
42	AD5	I/O	Address bit 5
41	AD6	I/O	Address bit 6
40	AD7	I/O	Address bit 7
37	AD8	I/O	Address bit 8
36	AD9	I/O	Address bit 9
35	AD10	I/O	Address bit 10
34	AD11	I/O	Address bit 11
33	AD12	I/O	Address bit 12
32	AD13	I/O	Address bit 13
31	AD14	I/O	Address bit 14
30	AD15	I/O	Address bit 15

Pin No.	Pin Name	Input Output	Function
16	AD16	I/O	Address bit 16
15	AD17	I/O	Address bit 17
14	AD18	I/O	Address bit 18
13	AD19	I/O	Address bit 19
12	AD20	I/O	Address bit 20
11	AD21	I/O	Address bit 21
10	AD22	I/O	Address bit 22
9	AD23	I/O	Address bit 23
4	AD24	I/O	Address bit 24
3	AD25	I/O	Address bit 25
2	AD26	I/O	Address bit 26
1	AD27	I/O	Address bit 27
100	AD28	I/O	Address bit 28
99	AD29	I/O	Address bit 29
98	AD30	I/O	Address bit 30
97	AD31	I/O	Address bit 31
26	PAR	I/O	Parity bit
38	C/BE0#	I/O	Bus command and byte enable 0
27	C/BE1#	I/O	Bus command and byte enable 1
18	C/BE2#	I/O	Bus command and byte enable 2
5	C/BE3#	I/O	Bus command and byte enable 3
93	CLK	I	PCI clock
92	RST#	I	Reset
19	FRAME#	I/O	Cycle frame
20	IRDY#	I/O	Initiator ready
21	TRDY#	I/O	Target ready
23	STOP#	I/O	Stop
6	IDSEL	I	Initialisation device select
22	DEVSEL#	I/O	Device select
95	REQ#	O	Request
94	GNT#	I	Grant
24	PERR#	I/O	Parity error
25	SERR#	O	System error
53	PME	O	Power management event (high active) see also: Figure 14 on page 61
91	INTA#	O	Interrupt A

2.2 Auxiliary port

Pin No.	Pin Name	Input Output	Function
75	DAUX0	I/O	AUX data bit 0
74	DAUX1	I/O	AUX data bit 1
73	DAUX2	I/O	AUX data bit 2
72	DAUX3	I/O	AUX data bit 3
71	DAUX4	I/O	AUX data bit 4
70	DAUX5	I/O	AUX data bit 5
69	DAUX6	I/O	AUX data bit 6
68	DAUX7	I/O	AUX data bit 7
67	/AUX_WR	O	AUX write
66	/AUX_RD	O	AUX read
65	/ADR_WR	I/O [d)]	AUX address write

d) internal pull down

2.3 S/T interface transmit signals

88	TX2_HI	O	Transmit output 2
87	/TX1_LO	O	GND driver for transmitter 1
86	/TX_EN	O	Transmit enable
85	/TX2_LO	O	GND driver for transmitter 2
84	TX1_HI	O	Transmit output 1

See also: 7.2 External transmitter circuitry.

2.4 S/T interface receive signals

82	R2	I	Receive data 2
81	LEV_R2	I	Level detect for R2
80	LEV_R1	I	Level detect for R1
79	R1	I	Receive data 1
78	ADJ_LEV	O	Levelgenerator

See also: 7.1 External receiver circuitry.

2.5 Oscillator

Pin No.	Pin Name	Input Output	Function
51	OSC_IN	I	Oscillator input or quarz connection 12.288 MHz
50	OSC_OUT	O	Oscillator output or quarz connection

2.6 GCI/IOM2 bus interface

54	C4IO	I/O u)	4.096 MHz clock GCI/IOM2 bus clock master: output GCI/IOM2 bus clock slave: input (reset default)
55	F0IO	I/O u)	Frame synchronisation, 8kHz pulse for GCI/IOM2 bus frame synchronisation GCI/IOM2 bus master: output GCI/IOM2 bus slave: input (reset default)
56	STIO1	I/O u)	GCI/IOM2 bus databus I Slotwise programmable as input or output
57	STIO2	I/O u)	GCI/IOM2 bus databus II Slotwise programmable as input or output

u) internal pull up

2.7 GCI/IOM2 Timeslot enable signals

(e. g. for PCM codecs)

58	F1_A	O	enable signal for external CODEC A Programmable as positive (reset default) or negative pulse.
59	F1_B	O	enable signal for external CODEC B Programmable as positive (reset default) or negative pulse.

2.8 EEPROM interface

The external EEPROM is optional. EE_SCL/EN must be connected to GND if no external EEPROM is available.

63	EE_SDA	I/O u)	Serial data of external EEPROM
62	EE_SCL/EN	I/O u)	Clock of external EEPROM / EEPROM enable

u) internal pull up

2.9 Power supply

Pin No.	Pin Name	Function
7, 28, 48, 60, 76, 89	VDD	VDD (+3.3V or +5V)
8, 17, 29, 39, 49, 52, 61, 64, 77, 83, 90, 96	GND	GND

☝ **important!**
All power supply pins VDD must be directly connected to each other. Also all pins GND must be directly connected to each other.

To keep VDD and GND bounce to a minimum a bypass capacitor (10 nF to 100 nF) should be placed between each pair of VDD/GND pins.

2.10 RESET characteristics

The reset signal (hardware reset or software reset) must be active for at least 4 clock cycles.

The GCI/IOM2 bus lines STIO1, STIO2 and the interrupt lines are in tristate mode after a reset.

The HFC-S PCI A is in slave mode after reset. C4IO and F0IO are inputs.

The S/T state machine is stuck to '0' after reset. This means the HFC-S PCI A does not react to any signal on the S/T interface before the S/T state machine is initialised.

The registers' initial values are described in the Register bit description (section 4 of this data sheet).

During initialisation phase the HFC-S PCI A must not be accessed. Bit 1 of the STATUS register is cleared to '0' to indicate that the initialisation phase has been finished.

3 Functional description

3.1 PCI-interface

3.1.1 PCI access types used by HFC-S PCI A

C/BE3#	C/BE2#	C/BE1#	C/BE0#	Command Type	HFC-S PCI A mode
0	0	1	0	I/O Read	target mode
0	0	1	1	I/O Write	target mode
0	1	1	0	Memory Read	target mode and master mode
1	1	0	0	Memory Read Multiple	target mode
1	1	1	0	Memory Read Line	target mode
0	1	1	1	Memory Write	target mode and master mode
1	1	1	1	Memory Write and Invalidate	target mode
1	0	1	0	Configuration Read	target mode
1	0	1	1	Configuration Write	target mode

Table 1: PCI command types

Memory Read Line and Memory Read Multiple commands are aliased to Memory Read. Memory Write and Invalidate is aliased to Memory Write.

3.1.2 PCI modes supported

The HFC-S PCI A supports both target mode and master mode. Before the HFC-S PCI A can operate in master mode the 32K Memory Window Base Address register (MWBA) must be configured.
Afterwards all FIFO data accesses are done by the HFC-S PCI A automatically by PCI master accesses. Only control and configuration register accesses must be done by PCI target accesses by the host CPU.

3.1.3 PCI buffer signaling and power supply environment

The HFC-S PCI A supports 5V and 3.3V PCI bus environments. The environment mode is set during RESET (RST# low) by the input value of /ADR_WR.

PCI bus power and signaling environment	/ADR_WR during RST# low
3.3V	high *)
5V	low

Warning!

/ADR_WR is an output after reset. So do not connect it directly to GND or VDD.

*) external pull-up resistor required (10k)

3.1.4 PCI configuration registers

Byte 3	Byte 2	Byte 1	Byte 0	Hex Address
Device ID		**Vendor ID**		00h
Status Register		**Command Register**		04h
Class Code			**Revision ID**	08h
BIST	**Header Type**	**Latency Timer**	**Cache Line Size**	0Ch
I/O Base Address				10h
Memory Base Address				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
CardBus CIS Pointer				28h
Subsystem ID		**Subsystem Vendor ID**		2Ch
Expansion ROM Base Address				30h
Reserved			**Cap_Ptr**	34h
Reserved				38h
Max_Lat	**Min_Gnt**	**Interrupt Pin**	**Interrupt Line**	3Ch
PMC		**Next Item Ptr**	**Cap_ID**	40h
Data	**PMCSR BSE**	**PMCSR**		44h
32K Memory Window Base Address (MWBA)				80h

■ Register is implemented, value can be read from EEPROM
■ Register is implemented
□ Register is not implemented and returns all 0's when read

The external EEPROM is optional. If no EEPROM is available, EE_SCL/EN must be connected to GND. Without EEPROM the PCI configuration registers will be loaded with the default values shown in Table 2.
All registers which can be read from EEPROM can also be written by configuration write accesses. The addresses for configuration write are shown in the table below.

Register Name	Default Value	Remarks
Vendor ID	1397h	Value can be read from EEPROM. Base address for configuration write is C0h.
Device ID	2BD0h	Value can be read from EEPROM. Base address for configuration write is C0h.
Command Register		Bits Function 0 Enables/disables I/O space accesses. 1 Enables/disables memory space accesses. 2 Enables/disables master accesses. 5..3 fixed to '0' 6 **PERR#** enable/disable 7 fixed to '0' 8 **SERR#** enable/disable 15..9 fixed to '0'
Status Register	0210h	Bits[7:0] can be read from EEPROM. Base address for configuration write is C4h. Bits Function 3..0 reserved 4 fixed to '1' 5 66MHz capable 6 User definable features supported 7 fast Back-to-Back capable 8 data parity error detected 10..9 fixed to '01': timing of DEVSEL# is medium 11 signaled target abort (fixed to '0') 12 received target abort 13 received master abort 14 signaled system error (Addr. parity error) 15 detected partity error
Revision ID	02h	HFC-S PCI A
Class Code	02 80 00h	Value can be read from EEPROM. Base address for configuration write is C8h.
Latency Timer	10h	Set to 16 clocks, value is fixed.
Header Type	00h	Header Type 0
BIST	00h	No build in self test supported.
I/O Base Address		Bits[31:3] are r/w by configuration accesses
Memory Base Address		Bits[31:8] are r/w by configuration accesses
Subsystem Vendor ID	1397h	Value can be read from EEPROM. Base address for configuration write is ECh.
Subsystem ID	2BD0h	Value can be read from EEPROM. Base address for configuration write is ECh.
Cap_Ptr	40h	Offset to Power Management register block.

Register Name	Default Value	Remarks
Interrupt Line	FFh	This register must be configured by configuration write.
Interrupt Pin	01h	INTA supported
Min_Gnt	00h	Value can be read from EEPROM. Base address for configuration write is FCh.
Max_Lat	10h	Value can be read from EEPROM. Base address for configuration write is FCh.
Cap_ID	01h	Capability ID. 01h identifies the linked list item as PCI Power Management registers.
Next Ptr	00h	There are no next items in the linked list.
PMC	7E21h	Power Management Capabilities. See also PCI Bus Power Management Interface Specification. This register's value can be read from EEPROM. Base address for configuration write is E0h. **PME#** can be asserted from D0, D1, D2 and $D3_{hot}$. Device specific initialisation is required. The HFC-S PCI A does not require PCI-clock to generate PME# (if S/T change state is selected). This function complies with the PCI Power Management Spec. Version 1.0.
PMCSR	0000h	Power Management Control/Status Bits Function 15 **PME_Status** - This bit is set when the function would normally assert the **PME**# signal independent of the state of the **PME_En** bit. Writing a '1' to this bit will clear it and cause the function to stop asserting a **PME**# (if enabled). Writing a '0' has no effect. 14..9 fixed to '0' 8 **PME_En** - A '1' enables the function to assert **PME#.** When '0', **PME**# assertion is disabled. 7..2 fixed to '0' 1..0 **PowerState** - This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. 00b - ***D0*** 01b - ***D1*** 10b - ***D2*** 11b - $\boldsymbol{D3_{hot}}$ All States except D0 disable HFC-S PCI A master accesses.

Register Name	Default Value	Remarks
32K Memory Window Base Address (MWBA)	0000h	Bits[31:15] are r/w by configuration accesses. The 32K Memory Window is for HFC-S PCI A internal use and for the B- and D-channel FIFOs. This register must be written by a "DWORD Config Write" to enable the HFC-S PCI A to operate in master mode.

Table 2: PCI configuration registers' initial values

Unimplemented registers return all 0's when read.

3.2 Internal HFC-S PCI A register description

If the HFC-S PCI A is used in memory mapped mode all register can directly be accessed by adding their CIP address to the configured Memory Base Address.

In I/O address mapped mode the HFC-S PCI A occupies 8 bytes in the I/O address space. Byte 0 is for data read/write, byte 4 for register selection. The AUX-port address is selected by byte 3, AUX-port data is read/written by byte 1.

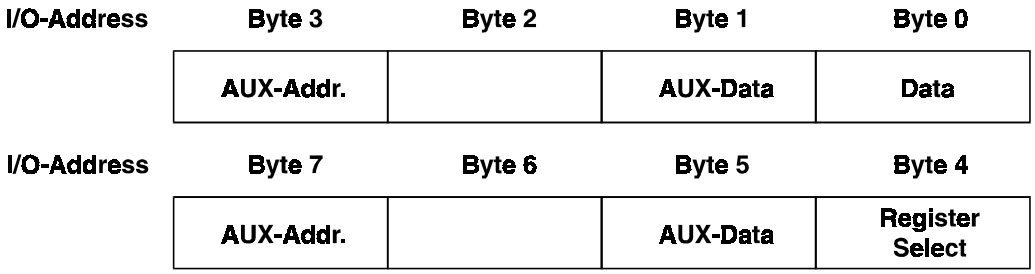


Figure 3: HFC-S PCI A in I/O address mapped mode

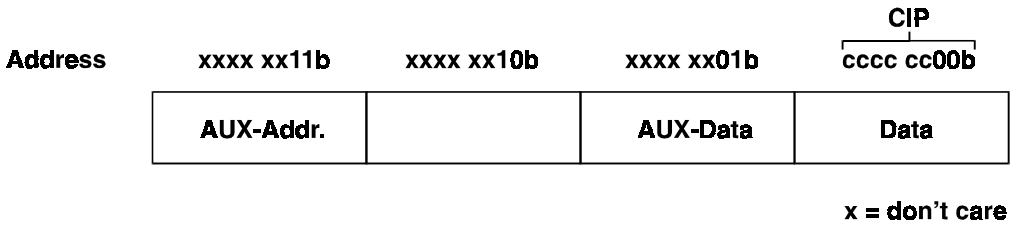


Figure 4: HFC-S PCI A in memory address mapped mode

3.2.1 Registers of the S/T section

CIP / I/O-address		Name	r/w	Function
1100 0000	C0h	STATES	r/w	State of the TE/NT state machine
1100 0100	C4h	SCTRL	w	S/T control register
1100 1000	C8h	SCTRL_E	w	S/T control register (extended)
1100 1100	CCh	SCTRL_R	w	receive enable for B-channels
1101 0000	D0h	SQ_REC SQ_SEND	r w	receive register for S/Q bits send register for S/Q bits
1101 1100	DCh	CLKDEL	w	setup of the delay time between receive and send direction (TE) receive data sample time (NT)
1111 0000	F0h	B1_REC*) B1_SEND*)	r w	B1-channel receive register B1-channel transmit register
1111 0100	F4h	B2_REC*) B2_SEND*)	r w	B2-channel receive register B2-channel transmit register
1111 1000	F8h	D_REC*) D_SEND*)	r w	D-channel receive register D-channel transmit register
1111 1100	FCh	E_REC*)	r	E-channel receive register

*) These registers are read/written automatically by the HDLC FIFO controller (HFC) or GCI/IOM2 bus controller and need not be accessed by the user. To read/write data the FIFOs in the Memory Window should be used.

3.2.2 Registers of the GCI/IOM2 bus section

GCI/IOM2 bus timeslot selection registers

CIP / I/O-address		Name	r/w	Function
0000 1000	08h	C/I	r/w	C/I command/indication register
0000 1100	0Ch	TRxR	r	Monitor Tx ready handshake
0010 1000	28h	MON1_D	r/w	first monitor byte
0010 1100	2Ch	MON2_D	r/w	second monitor byte

GCI/IOM2 bus timeslot selection registers

CIP / I/O-address		Name	r/w	Function
1000 0000	80h	B1_SSL	w	B1-channel transmit slot (0..31)
1000 0100	84h	B2_SSL	w	B2-channel transmit slot (0..31)
1000 1000	88h	AUX1_SSL	w	AUX1-channel transmit slot (0..31)
1000 1100	8Ch	AUX2_SSL	w	AUX2-channel transmit slot (0..31)
1001 0000	90h	B1_RSL	w	B1-channel receive slot (0..31)
1001 0100	94h	B2_RSL	w	B2-channel receive slot (0..31)
1001 1000	98h	AUX1_RSL	w	AUX1-channel receive slot (0..31)
1001 1100	9Ch	AUX2_RSL	w	AUX2-channel receive slot (0..31)

GCI/IOM2 bus data registers

CIP / I/O-address		Name	r/w	Function
1010 0000	A0h	B1_D*)	r/w	GCI/IOM2 bus B1-channel data register
1010 0100	A4h	B2_D*)	r/w	GCI/IOM2 bus B2-channel data register
1010 1000	A8h	AUX1_D	r/w	AUX1-channel data register
1010 1100	ACh	AUX2_D	r/w	AUX2-channel data register

*) These registers are read/written automatically by the HDLC FIFO controller (HFC) or by the S/T controller and need not be accessed by the user.

GCI/IOM2 bus configuration registers

CIP / I/O-address		Name	r/w	Function
1011 0100	B4h	MST_EMOD	w	extended mode register for GCI/IOM2 bus
1011 1000	B8h	MST_MODE	w	mode register for GCI/IOM2 bus
1011 1100	BCh	CONNECT	w	connect functions for S/T, HFC, GCI/IOM2

3.2.3 Interrupt and status registers

CIP / I/O address		Name	r/w	Function
0100 0100	44h	FIFO_EN	w	FIFO enable/disable
0100 1000	48h	TRM	w	transparent mode interrupt mode register
0100 1100	4Ch	B_MODE	w	mode of B-channels
0101 1000	58h	CHIP_ID	r	register for chip identification
0110 0000	60h	CIRM	w	interrupt selection and softreset register
0110 0100	64h	CTMT	w	transparent mode and timer control register
0110 1000	68h	INT_M1	w	interrupt mask register 1
0110 1100	6Ch	INT_M2	w	interrupt mask register 2
0111 1000	78h	INT_S1	r	interrupt status register 1
0111 1100	7Ch	INT_S2	r	interrupt status register 2
0111 0000	70h	STATUS	r	common status register

3.2.4 Register list

Registers by Address		
Address	**Name**	**Page**
08h	C/I	39
0Ch	TRxR	39
28h	MON1_D	19
2Ch	MON2_D	19
44h	FIFO_EN	41
48h	TRM	43
4Ch	B_MODE	42
58h	CHIP_ID	42
60h	CIRM	41
64h	CTMT	42
68h	INT_M1	43
6Ch	INT_M2	43
70h	STATUS	45
78h	INT_S1	44
7Ch	INT_S2	44
80h	B1_SSL	37
80h	B2_SSL	37
88h	AUX1_SSL	37
8Ch	AUX2_SSL	37
90h	B1_RSL	37
94h	B2_RSL	37
98h	AUX1_RSL	37
9Ch	AUX2_RSL	37
A0h	B1_D	37
A4h	B2_D	37
A8h	AUX1_D	37
ACh	AUX2_D	37
B4h	MST_EMOD	39
B8h	MST_MODE	38
BCh	CONNECT	40
C0h	STATES	34
C4h	SCTRL	35
C8h	SCTRL_E	35
CCh	SCTRL_R	36
D0h	SQ_REC	36
D0h	SQ_SEND	36
DCh	CLKDEL	36
F0h	B1_REC	18
F0h	B1_SEND	18
F4h	B2_REC	18
F4h	B2_SEND	18
F8h	D_REC	18
F8h	D_SEND	18
FCh	E_REC	18

Table 3: Register list by address

Registers by Name		
Address	**Name**	**Page**
A8h	AUX1_D	37
98h	AUX1_RSL	37
88h	AUX1_SSL	37
ACh	AUX2_D	37
9Ch	AUX2_RSL	37
8Ch	AUX2_SSL	37
4Ch	B_MODE	42
A0h	B1_D	37
F0h	B1_REC	18
90h	B1_RSL	37
F0h	B1_SEND	18
80h	B1_SSL	37
A4h	B2_D	37
F4h	B2_REC	18
94h	B2_RSL	37
F4h	B2_SEND	18
80h	B2_SSL	37
08h	C/I	39
58h	CHIP_ID	42
60h	CIRM	41
DCh	CLKDEL	36
BCh	CONNECT	40
64h	CTMT	42
F8h	D_REC	18
F8h	D_SEND	18
FCh	E_REC	18
44h	FIFO_EN	41
68h	INT_M1	43
6Ch	INT_M2	43
78h	INT_S1	44
7Ch	INT_S2	44
28h	MON1_D	19
2Ch	MON2_D	19
B4h	MST_EMOD	39
B8h	MST_MODE	38
C4h	SCTRL	35
C8h	SCTRL_E	35
CCh	SCTRL_R	36
D0h	SQ_REC	36
D0h	SQ_SEND	36
C0h	STATES	34
70h	STATUS	45
48h	TRM	43
0Ch	TRxR	39

Table 4: Register list by name

3.3 Power Management Support of HFC-S PCI A

Because of the very low power dissipitation of HFC-S PCI A device there is no need of reducing power in standby mode. Furthermore the main source of power dissipation is the 33MHz PCI clock. So the biggest reduction in power dissipation of the device can be achieved by stopping the PCI clock which can only be done by the PCI bridge generating the PCI clock for the PCI slot concerned. So the lowest power is needed in bus states B2 and B3.

Another minor reduction of power dissipation can be achieved by stopping the 12.288 MHz clock for the ISDN part of the HFC-S PCI A. If no awake (restart of oscillation) from S/T bus activity is selected the power dissipation can be reduced to less then 3mW if PCI clock is also stopped.

None of the settings above are accomplished by changing the power states from D0 to D1, D2 or $D3_{hot}$. The register settings are only implemented to be compatible to PCI Power Management Specification. So no reduction of power is achieved by purely changing the power states.

In the following paragraph the awake scenarios for asserting PME# from different power states are described.

3.3.1 PME events

Generally the source for PME# generation can be selected from:

1. **D-channel receive frame interrupt**
   This is only possible in power state D0 and bus state B0 because D-channel data is put into the memory window (MW) of the HFC-S PCI A which is located in the memory space of the host PC.

2. **S/T state change normally generated due to S/T interface activation from outside**
   This is the normal source of the PME# event. In this case the PME# pin can be asserted in any power state (D0 – $D3_{hot}$).

3.3.2 Special considerations for support of $D3_{cold}$

The HFC-S PCI A was not specially designed to support $D3_{cold}$. However it is possible to use the device even in $D3_{cold}$ applications if an external power supply or the Vaux3.3 is available.

The device should be powered in a way that if the main supply is switched off the device is automatically feed by the auxiliary power supply.

Because PME context (PME_Status and PME_En) bits in PCMCSR register is not maintained when the device is reset (RST# asserted) the device must be prevented from being reset if main power is off. This unwanted reset is normally done due to dropping of all PCI input signals to GND when power is switched off.

With the additional device in Figure 5 the ability to react on RST# asserted can be switched off and on by masking the RST# pin. Because of a power on reset circuitry connected to the auxiliary power source the RST# masking is switched off when power is first time switched on.

In the preparation process for $D3_{cold}$ e.g. when the context of the chip must be saved before power is switched off the device driver must set the RES# mask bit to prevent an unwanted reset when the PC is switched off.

After getting power again and the reinitialisation of the chip is initiated the RST# mask bit is reset again by the device driver.

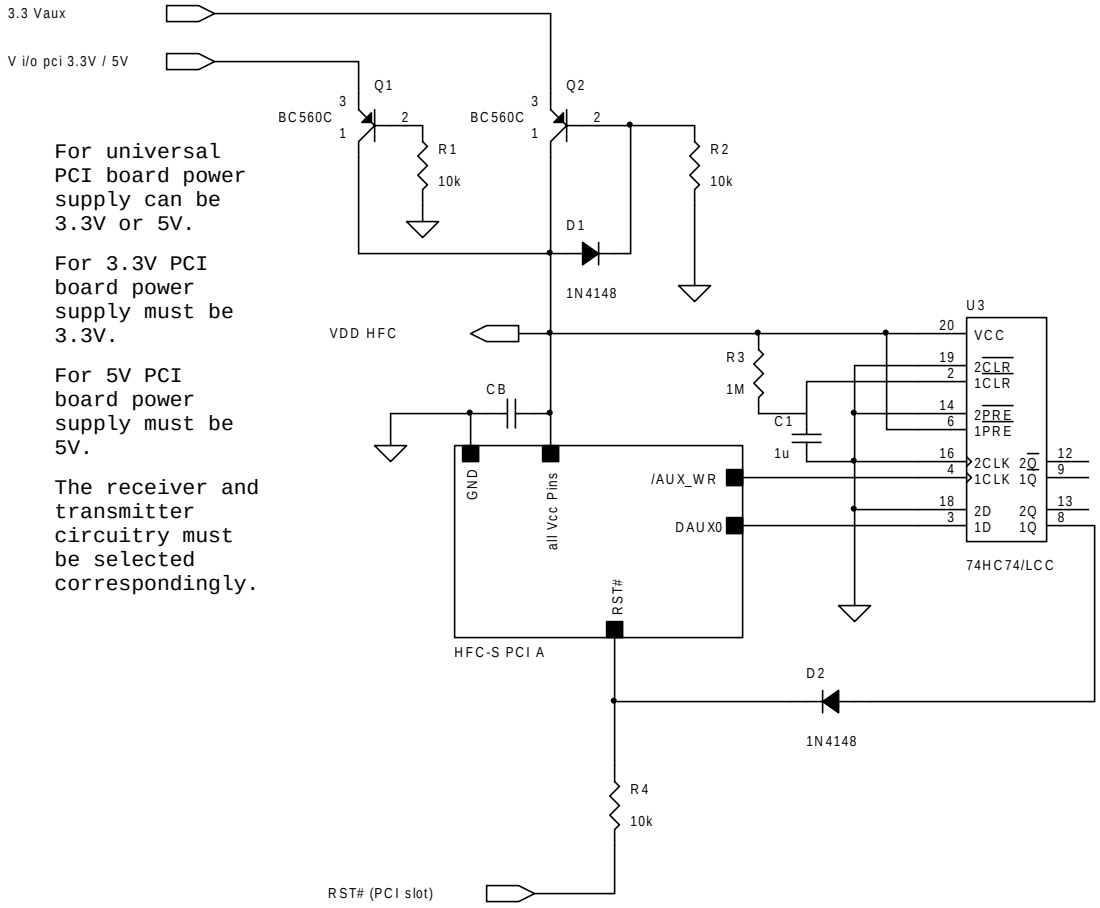


Figure 5: Masking RST# for $D3_{cold}$ Support

For 3.3V PCI boards Vcc must be 3.3V and the 3.3V receiver/transmitter circuitry must be used which can be found in the HFC-S PCI A datasheet.

For 5V PCI boards Vcc must be 5V and the 5V receiver/transmitter circuitry must be used which can be found in the HFC-S PCI A datasheet.

For the universal PCI board with auto power detection Vcc can be either 3.3V or 5V and the receiver/transmitter circuitry for the universal PCI board must be used which can be found in the universal PCI board sample circuitry for 3.3V and 5V power supply (see 12.5).

Literature

Further information about PCI Power Management can be found in the following specifications:

- PCI Local Bus Specification, Revision 2.2, December 18, 1998
- PCI Bus Power Management Interface Specification, Revision 1.1, December 18, 1998

3.4 Timer

The HFC-S PCI A includes a timer with interrupt capability. The timer counts F0IO pulses. So the timer counter is incremented every 125µs. It can be reset by bit 7 of of the CTMT register. Furthermore the timer is reset at every HFC-S PCI A access when bit 5 of the CTMT register is set. Seven different timer values can be selected.

3.5 FIFOs

All FIFOs are located in the 32K Memory Window (MW) in host PC's memory.

There are 6 FIFOs with 6 HDLC-Controllers handled by the HFC-S PCI A. The HDLC circuits are located on the S/T device side of the HFC-S PCI A. So always plain data is stored in the FIFO. Zero insertion and deletion is done in HDLC mode:

– if the data goes to the S/T or GCI/IOM device in send FIFOs and
– when the HDLC data comes from the S/T device or GCI/IOM2 bus in receive operation.

There are a send and a receive FIFO for each of the two B-channels and for the D-channel.

The FIFOs are realized as ring buffers in the 32K Memory Window in host PC's memory. To control them there are some counters.

	B-channel	D-channel
Z1: FIFO input counter	13 Bit	9 Bit
Z2: FIFO output counter	13 Bit	9 Bit

Each counter points to a byte position in the Memory Window. This is an offset to the 32K Memory Window Base Address in the configuration space. On a FIFO input operation Z1 is incremented. On an output operation Z2 is incremented.

After every pulse on the F0IO signal two HDLC-bytes are written into the S/T interface (FIFOs No. 0 and 2) and two HDLC-bytes are read from the S/T interface (FIFOs No. 1 and 3).
D-channel data is handled in a similar way but only 2 bits are processed.

> ☝ **important!**
> Instead of the S/T interface also GCI/IOM2 bus is selectable for each B-channel (see CONNECT register).

If Z1 = Z2 the FIFO is empty.

Additionally there are two counters F1 and F2 for every FIFO channel (5Bit for B-channel, 4Bit for D-channel). They count the HDLC-frames in the FIFOs and form a ring buffer as Z1 and Z2 do, too.

F1 is incremented when a complete frame has been received and stored in the FIFO. F2 is incremented when a complete frame has been read from the FIFO.

If F1 = F2 there is no complete frame in the FIFO.

When the RESET line is active or software reset is active Z1, Z2, F1 and F2 are all initialized to all 1s.

All Zx and Fx counters are also stored in the Memory Window. So it is easy to read and write the counters by simple host memory accesses.

Because the HFC-S PCI A is limited to the 32K Memory Window data in different regions of the host PC can not be overwritten even if counter and pointer values are handled in a wrong way.

> ☝ **important!**
> The counter state 0200h of the Z-counters follows counter state 1FFFh in the B-channel FIFOs.
> The counter state 000h of the Z-counters follows counter state 1FFh in the D-channel FIFOs.
>
> The counter state 00h of the F-counters follows counter state 1Fh in the B-channel FIFOs.
> The counter state 10h of the F-counters follows counter state 1Fh in the D-channel FIFOs.

3.5.1 FIFO counters location in Memory Window

For each FIFO one F1 and one F2 counter is available. The counters are located at the following offsets to the Memory Window Base Address (MWBA) in the Memory Window (MW).

FIFO	Counter	Offset to Memory Window Base Address	Counter Size in Bytes
B1-transmit	F1	2080h	1
	F2*)	2081h	1
B1-receive	F1*)	6080h	1
	F2	6081h	1
B2-transmit	F1	2180h	1
	F2*)	2181h	1
B2-receive	F1*)	6180h	1
	F2	6181h	1
D-transmit	F1	20A0h	1
	F2*)	20A1h	1
D-receive	F1*)	60A0h	1
	F2	60A1h	1

*) These counters are handled by the HFC-S PCI A automatically and must not be written by software.

For each FIFO an array of Z1 and Z2 counters is available. The offset of the counters to the Memory Window Base Address (MWBA) can be calculated as shown in the following table.

FIFO	Counter	Offset to Memory Window Base Address	Counter Size in Bytes
B1-transmit	Z1	2000h + (Fx * 4)	2
	Z2*)	2000h + (Fx * 4) + 2	2
B1-receive	Z1*)	6000h + (Fx * 4)	2
	Z2	6000h + (Fx * 4) + 2	2
B2-transmit	Z1	2100h + (Fx * 4)	2
	Z2*)	2100h + (Fx * 4) + 2	2
B2-receive	Z1*)	6100h + (Fx * 4)	2
	Z2	6100h + (Fx * 4) + 2	2
D-transmit	Z1	2080h + (Fx * 4)	2
	Z2*)	2080h + (Fx * 4) + 2	2
D-receive	Z1*)	6080h + (Fx * 4)	2
	Z2	6080h + (Fx * 4) + 2	2

*) These counters are handled by the HFC-S PCI A automatically and must not be written by software.

Fx is either F1 or F2. F1 is used for input data in transmit FIFOs, F2 is used for output data in receive FIFOs.

3.5.2 FIFO data location in Memory Window

FIFO	Starting at Offset	Ending at Offset	Offset to add to Z-counters value
B1-transmit	0200h	1FFFh	0000h
B1-receive	4200h	5FFFh	4000h
B2-transmit	2200h	3FFFh	2000h
B2-receive	6200h	7FFFh	6000h
D-transmit	0000h	01FFh	0000h
D-receive	4000h	41FFh	4000h

3.5.3 FIFO channel operation

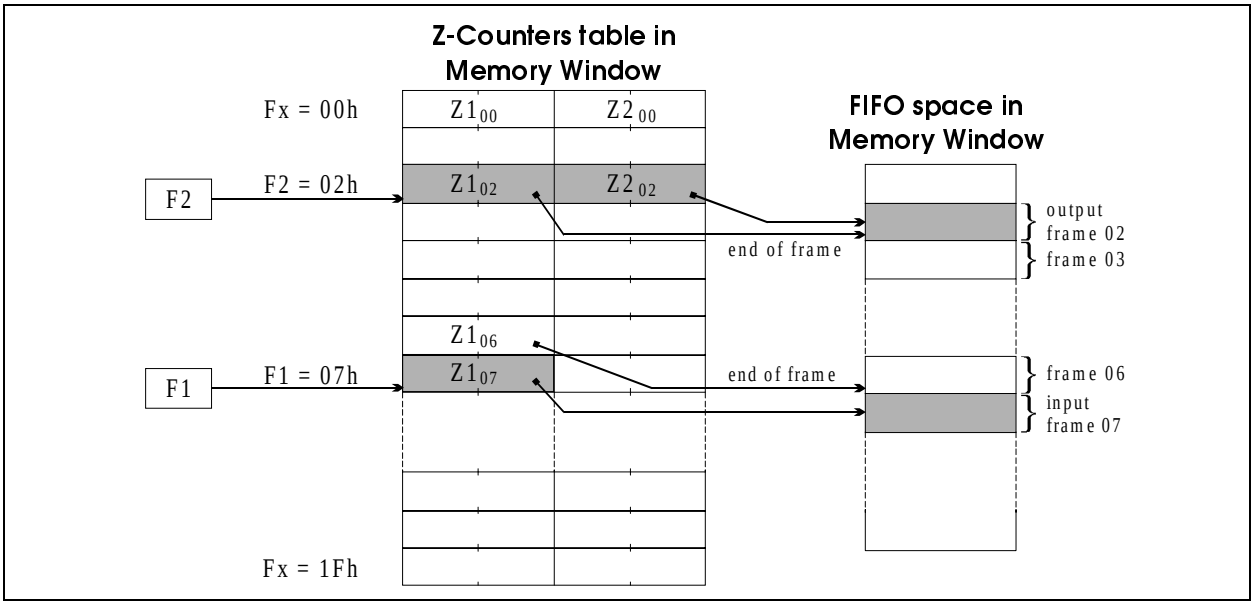


Figure 6: FIFO Organisation (shown for B-channel, similar for D-channel)

3.5.3.1 Send channels (B1, B2 and D transmit)

The send channels send data from the host bus interface to the FIFO and the HFC-S PCI A converts the data into HDLC code and tranfers it from the FIFO into the S/T or/and the GCI/IOM2 bus interface write registers.

The HFC-S PCI A checks Z1 and Z2. If Z1=Z2 (FIFO empty) the HFC-S PCI A generates a HDLC-Flag (01111110) and sends it to the S/T device. In this case Z2 is not incremented. If also F1=F2 only HDLC flags are sent to the S/T interface and all counters remain unchanged. If the frame counters are unequal F2 is incremented and the HFC-S PCI A tries to send the next frame to the output device. After the end of a frame (Z2 reaches Z1) it automatically generates the 16 bit CRC checksum and adds the ending flag. If there is another frame in the FIFO (F1≠F2) the F2 counter is incremented.

With every byte being sent from the host bus side to the FIFO Z1 is incremented automatically. If a complete frame has been sent F1 must be incremented to send the next frame. If the frame counter F1 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 6).
Z1(F1) is used for the frame which is just written from the PC-bus side. Z2(F2) is used for the frame which is just beeing transmitted to the S/T device side of the HFC-S PCI A. Z1(F2) is the end of frame pointer of the current output frame.

In the send channels F1 is only changed from the PC interface side if the software driver wants to say „end of send frame“. Then the current value of Z1 is stored, F1 is incremented and Z1 is used as start address of the next frame. Z1(F2) and Z2(F2) can not be accessed.

3.5.3.2 Automatically D-channel frame repetition

The D-channel send FIFO has a special feature. If the S/T interface signals a D-channel contention before the CRC is sent the Z2 counter is set to the starting address of the current frame and the HFC-S PCI A tries to repeat the frame automatically.

> ☝ **important!**
> The HFC-S PCI A begins to transmit bytes from a FIFO at the moment Z1 ≠ Z2. So if the Z1 pointer is updated by software after writing the transmit data into the FIFO space of the Memory Window the transmission starts.

3.5.3.3 FIFO full condition in send channels

FIFO full condition can easily be calculated from the Z1/Z2 table in the Memory Window.

Remember that an increment of Z-value 1FFFh is 0200h in the B-channels!

There are two different FIFO full conditions. The first one is met when the FIFO contents comes up to 31 frames (B-channel) or 15 frames (D-channel). There is no possibility for the HFC-S PCI A to manage more frames even if the frames are very small.

The second limitation is the size of the FIFO which is 512 byte for the D-channel and 7.5 KByte for the B-channels.

3.5.3.4 Receive Channels (B1, B2 and D receive)

The receive channels receive data from the S/T or GCI/IOM2 bus interface read registers. The data is converted from HDLC into plain data and sent to the FIFO. The data can then be read via the host bus interface.

The HFC-S PCI A checks the HDLC data coming in. If it finds a flag or more than 5 consecutive 1s it does not generate any output data. In this case Z1 is not incremented. Proper HDLC data being received is converted by the HFC-S PCI A into plain data. After the ending flag of a frame the HFC-S PCI A checks the HDLC CRC checksum. If it is correct one byte with all 0s is inserted behind the CRC data in the FIFO named STAT. This last byte of a frame in the FIFO is different from all 0s if there is no correct CRC field at the end of the frame.

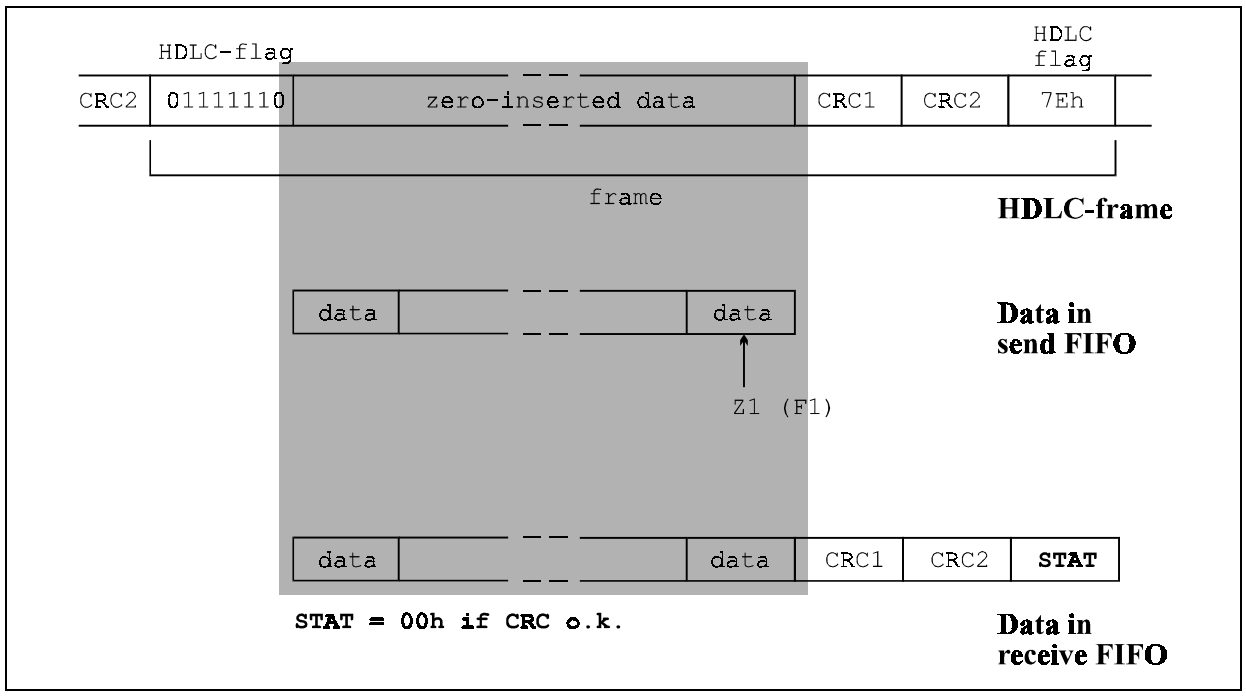


Figure 7: FIFO Data Organisation

The ending flag of a HDLC-frame can also be the starting flag of the next frame.

After a frame is received completely F1 is incremented by the HFC-S PCI A automatically and the next frame can be received.

After reading a frame via the host bus interface F2 must be incremented. If the frame counter F2 is incremented also the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2) and Z2(F2) (see Figure 6).
Z1(F1) is used for the frame which is just received from the S/T device side of the HFC. Z2(F2) is used for the frame which is just beeing transmitted to the host bus interface. Z1(F2) is the end of frame pointer of the current output frame.

To calculate the length of the current receive frame the software has to evaluate Z1-Z2+1.

In the receive channels F2 must be incremented to point to the next Z1/Z2 pair. If Z1 = Z2 and F1 = F2 the FIFO is totally empty.

3.5.3.5 FIFO full condition in receive channels

Because the ISDN-B-channels and the ISDN-D-channels have no hardware based flow control there is no possibility to stop input data if a receive FIFO is full.

So there is no FIFO full condition implemented in the HFC-S PCI A. The HFC-S PCI A assumes that the FIFOs are so deep that the host processor hard- and software is able to avoid any overflow of the receive FIFOs. Overflow conditions are again more than 31 input frames (15 frames for D-channel) or a real overflow of the FIFO because of excessive data.

Because HDLC procedures only know a window size of 7 frames no more than 7 frames are sent without software intervention. Due to the great size of the FIFOs of the HFC-S PCI A it is easy to poll counters in the Memory Window even in large time intervalls without having to fear a FIFO overflow condition.

However to avoid any undetected FIFO overflows the software driver should check the number of frames in the FIFO which is F1-F2. An overflow exists if the number (F1-F2) is less than the number in the last reading even if there was no reading of a frame in between.

After a detected FIFO overflow condition this FIFO must be reset.

3.5.3.6 FIFO initialisation

All counters Z1, Z2, F1 and F2 of all FIFOs are initialized to all 1s after a RESET.

Then the result is Z1 = Z2 = 1FFFh and F1 = F2 = 1Fh for the B-channels and Z1 = Z2 = 1FFh and F1 = F2 = 1Fh for the D-channel. This information is written in the Memory Window for initialisation.

Please mask bit 4 of D-channel from counter F1, F2.

The same initialisation is done if the bit 3 in the CIRM register is set (soft reset).

During initialisation phase the HFC-S PCI A must not be accessed. Bit 1 of the STATUS register is cleared to '0' to indicate that the initialisation phase has been finished.

3.5.4 Transparent mode of HFC-S PCI A

You can switch off HDLC operation for each B-channel independently. There is one bit for each B-channel in the CTMT control register. If this bit is set data in the FIFO is sent directly to the S/T or GCI/IOM2 bus interface and data from the S/T or GCI/IOM2 bus interface is sent directly to the FIFO.

Be sure to switch into transparent mode only if F1=F2. Being in transparent mode the Fx counters remain unchanged. Z1 and Z2 are the input and output pointers respectively. Because F1=F2 both Z-counters are always accessable and have valid data.

If a send FIFO channel changes to FIFO empty condition no CRC is generated and the last data byte written into the FIFO is repeated until there is new data.

In receive channels there is no check on flags or correct CRCs and no status byte is added.

The byte bounderies are not arbitrary like in HDLC mode where byte synchronisation is achieved with HDLC-flags. The data is just the same as it comes from the S/T or GCI/IOM2 bus interface or is sent to this.

Send and receive transparent data can be handled in two ways. The usual way is transmitting B-channel data with the LSB first as it is usual in HDLC mode. The second way is sending the bytes in reverse bit order as it is usual for PWM data. So the first bit is the MSB. The bit order can be reversed by setting the corresponding bits in the CIRM register.

3.6 Configuring test loops

For electrical tests of layer 1 it is useful to create a S/T test loop for the B1/B2 channel. The test loop described here transmits the data that has been received on the B1 or B2 channel to the same channel on the S/T interface. The 32K Memory Window Base Address (MWBA) PCI configuration register must be written first to enable PCI master accesses of the HFC-S PCI A. To configure the test loop the following must be done:

- write **0Fh** to register CLKDEL (**DCh**) // Adjust the phase offset between receive and
  // transmit direction (the value depends on the external
  // circuitry).
- write **43h** to register SCTRL (**C4h**) // 03h is to enable B1, B2 at the S/T interface for
  // transmission
  // 40h is for TX_LO setup (capacitive line mode)
- write **00h** to register STATES (**C0h**) // Release S/T state machine for activation over the
  // S/T interface by incoming INFO 2 or INFO 4.
- write **03h** to register SCTRL_R (**CCh**) // Configure S/T B1 and B2 channel to normal
  // receive operation.
- write **36h** to register CONNECT (**BCh**) // Configure CONNECT register for B1/B2 channel
  // test loop.
- write **80h** to register B1_SSL (**80h**) // Enable transmit channel for GCI/IOM2 bus, pin
  // STIO1 is used as output, use time slot #0.
- write **C0h** to register B1_RSL (**90h**) // Enable receive channel for GCI/IOM2 bus, pin
  // STIO1 is used as input, use time slot #0.
- write **81h** to register B2_SSL (**84h**) // Enable transmit channel for GCI/IOM2 bus, pin
  // STIO1 is used as output, use transmission slot #1.
- write **C1h** to register B2_RSL (**94h**) // Enable receive channel for GCI/IOM2 bus, pin
  // STIO1 is used as input, use time slot #1.
- write **01h** to register MST_MODE (**B8h**) // Configure HFC-S PCI A as GCI/IOM2 bus master.

4 Register bit description

4.1 Register bit description of S/T section

Name	Addr.	Bits	r/w	Function
STATES (read)	C0h	3..0	r	binary value of actual state (NT: Gx, TE: Fx)
		4	r	Frame-Sync ('1'=synchronized)
		5	r	'1' timer T2 expired (NT mode only, see also 8.1 S/T interface activation/deactivation layer 1 for finite state matrix for NT on page 62)
		6	r	'1' receiving INFO0
		7	r	'0' no operation '1' in NT mode allows transition from G2 to G3. This bit is automatically cleared after the transition.
STATES (write)	C0h	3..0	w	binary value of new state (NT: Gx, TE: Fx) (bit 4 must also be set to load the state).
		4	w	'1' loads the prepared state (bit 3..0) and stops the state machine.This bit needs to be set for a minimum period of 5.21µs and must be cleared by software. (reset default) '0' enables the state machine (bits 3..0 are ignored). After writing an invalid state the state machine goes to deactivated state (G1, F2)
		6..5	w	'00' no operation '01' no operation '10' start deactivation '11' start activation The bits are automatically cleared after activation/deactivation.
		7	w	'0' no operation '1' in NT mode allows transition from G2 to G3. This bit is automatically cleared after the transition.

☝ **important!**
The state machine is stuck to '0' after a reset. Writing a '0' to bit 4 of the STATES register restarts the state machine.
In this state the HFC-S PCI A sends no signal on the S/T-line and it is not possible to activate it by incoming INFOx.

NT mode:
The NT state machine does not change automatically from G2 to G3 if the TE side sends INFO3 frames. This transition must be activated each time by bit 7 of the STATES register.

Fix the NT state machine to state G3 when activated (by writing 13h into STATES register). This prevents deactivation of NT mode S/T interface due to sporadically errors on NT input data.

Name	Addr.	Bits	r/w	Function
SCTRL	C4h			B-channel enable
		0	w	'0' B1 send data disabled (permanent 1 sent in activated states, reset default) '1' B1 data enabled
		1	w	'0' B2 send data disabled (permanent 1 sent in activated states, reset default) '1' B2 data enabled
		2	w	S/T interface mode '0' TE mode (reset default) '1' NT mode
		3	w	D-channel priority '0' high priority 8/9 (reset default) '1' low priority 10/11
		4	w	S/Q bit transmission '0' S/Q bit disable (reset default) '1' S/Q bit and multiframe enable
		5	w	'0' normal operation (reset default) '1' send 96kHz transmit test signal (alternating zeros)
		6	w	TX_LO line setup This bit must be configured depending on the used S/T module and circuitry to match the 400Ω pulse mask test. '0' capacitive line mode (reset default) '1' non capacitive line mode
		7	w	Power down '0' power up, oscillator active (reset default) '1' power down, oscillator stopped
SCTRL_E	C8h	0	w	Power down mode bit '0' S/T awake disable (reset default) Power up can only be programmed by register access (SCTRL bit 7). '1' S/T awake enable. Oscillator starts on every non INFO0 S/T signal.
		1	w	must be '0'
		2	w	D reset '0' normal operation (reset default) '1' D bits are forced to '1'
		3	w	D_U enable '0' normal operation (reset default) '1' D channel is always send enabled regardless of E receive bit
		6..4	w	must be '0'
		7	w	'0' normal operation (reset default) '1' B1/B2 are exchanged in the S/T interface

Name	Addr.	Bits	r/w	Function
SCTRL_R	CCh	0	w	B1-channel receive enable
		1	w	B2-channel receive enable '0' B-receive bits are forced to '1' '1' normal operation
		7..2	w	unused
SQ_REC	D0h	3..0	r	TE mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4) NT mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)
		4	r	'1' a complete S or Q multiframe has been received Reading SQ_REC clears this bit.
		6..5	r	not defined
		7	r	'1' ready to send a new S or Q multiframe Writing to SQ_SEND clears this bit.
SQ_SEND	D0h	3..0	w	TE mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4) NT mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)
		7..4	w	not defined
CLKDEL	DCh	3..0	w	TE: 4 bit delay value to adjust the 2 bit delay time between receive and transmit direction. The delay of the external S/T-interface circuit can be compensated. The lower the value the smaller the delay between receive and transmit direction (see also Figure 15) NT: Data sample point. The lower the value the earlier the input data is sampled. The steps are 163ns.
		6..4	w	NT mode only early edge input data shaping Low pass characteristic of extended bus configurations can be compensated. The lower the value the earlier input data pulse is sampled. No compensation means a value of 6 (110b). Step size is the same as for bits 3-0.
		7	w	unused

☝ **note!**
The register is not initialized with a '0' after reset. The register should be initialized as follows before activating the TE/NT state machine:
TE mode: 0Dh .. 0Fh NT mode: 6Ch

4.2 Register bit description of GCI/IOM2 bus section

Timeslots for transmit direction

Name	Addr.	Bits	r/w	Function
B1_SSL	80h	4..0	w	select GCI/IOM2 bus transmission slot (0..31)
B2_SSL	84h	5	w	unused
AUX1_SSL AUX2_SSL	88h 8Ch	6	w	select GCI/IOM2 bus data lines '0' STIO1 output '1' STIO2 output
		7	w	transmit channel enable for GCI/IOM2 bus '0' disable (reset default) '1' enable

☝ **important!**
Enabling more than one channel on the same slot causes undefined output data.

Timeslots for receive direction

Name	Addr.	Bits	r/w	Function
B1_RSL	90h	4..0	w	select GCI/IOM2 bus receive slot (0..31)
B2_RSL	94h	5	w	unused
AUX1_RSL AUX2_RSL	98h 9Ch	6	w	select GCI/IOM2 bus data lines '0' STIO2 is input '1' STIO1 is input
		7	w	receive channel enable for GCI/IOM2 bus '0' disable (reset default) '1' enable

Data registers

Name	Addr.	Bits	r/w	Function
B1_D	A0h	0..7	r/w	read/write data registers for selected timeslot data
B2_D	A4h			
AUX1_D	A8h			
AUX2_D	ACh			

☝ **note!**
If the data registers AUX1_D and AUX2_D are not overwritten, the transmisson slots AUX1_SSL and AUX2_SSL mirror the data received in AUX1_RSL and AUX2_RSL slots. This is useful for an internal connection between two CODECs. This mirroring is disabled by setting bit 1 in MST_EMOD register

Name	Addr.	Bits	r/w	Function
MST_MODE	B8h	0	w	GCI/IOM2 bus mode '0' slave (reset default) (C4IO and F0IO are inputs) '1' master (C4IO and F0IO are outputs)
		1	w	polarity of C4- and C2O-clock '0' F0IO is sampled on negative clock transition '1' F0IO is sampled on positive clock transition
		2	w	polarity of F0-signal '0' F0 positive pulse '1' F0 negative pulse
		3	w	duration of F0-signal '0' F0 active for one C4-clock (244ns) (reset default) '1' F0 active for two C4-clocks (488ns)
		5, 4	w	time slot for codec-A signal F1_A '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' signal C2O → pin F1_A (C2O is 2048 kHz clock)
		7, 6	w	time slot for codec-B signal F1_B '00' B1 receive slot '01' B2 receive slot '10' AUX1 receive slot '11' AUX2 receive slot

The pulse shape and polarity of the codec signals F1_A and F1_B is the same as the pulseshape of the F0IO signal. The polarity of C2O can be changed by bit 1.

RESET sets register MST_MODE to all '0's.

Name	Addr.	Bits	r/w	Function
MST_EMOD	B4h	0	w	slow down C4IO clock adjustment (see Figure 18) '0' C4IO clock is adjusted in the 31th time slot twice for one half clock cycle (reset default) '1' C4IO clock is adjusted in the 31th time slot once for one half clock cycle
		1	w	enable/disable AUX channel mirroring '0' normal opration (reset default) '1' disable AUX channel data mirroring
		2	w	unused
		5..3	w	select D-channel data flow (see also: CONNECT register) destination ← source bit 3: '0' D-HFC ← D-S/T '1' D-HFC ← D-GCI/IOM2 bit 4: '0' D-S/T ← D-HFC '1' D-S/T ← D-GCI/IOM2 bit 5: '0' D-GCI/IOM2 ← D-HFC '1' D-GCI/IOM2 ← D-S/T
		6	w	unused
		7	w	enable GCI/IOM2 write slots '0' disable GCI/IOM2 write slots; slot #2 and slot #3 may be used for normal data '1' enables slot #2 and slot #3 as master, D- and C/I-channel
C/I	08h	3..0	r/w	on read: indication on write: command
		7..4		unused
TRxR	0Ch	0	r	'1' monitor receive ready (2 bytes received) This bit is reset after read of second monitor byte (MON2_D)
		1	r	'1' Monitor transmitter ready Writing on MON2_D starts transmisssion and resets this bit.
		5..2	r	reserved
		6	r	STIO2 in
		7	r	STIO1 in

RESET sets register MST_EMOD to all '0's.

4.3 Register bit description of CONNECT register

Name	Addr.	Bits	r/w	Function
CONNECT	BCh	2..0	w	select B1-channel data flow destination ← source bit 0: '0' B1-HFC ← B1-S/T '1' B1-HFC ← B1-GCI/IOM2 bit 1: '0' B1-S/T ← B1-HFC '1' B1-S/T ← B1-GCI/IOM2 bit 2: '0' B1-GCI/IOM2 ← B1-HFC '1' B1-GCI/IOM2 ← B1-S/T
		5..3	w	select B2-channel data flow destination ← source bit 3: '0' B2-HFC ← B2-S/T '1' B2-HFC ← B2-GCI/IOM2 bit 4: '0' B2-S/T ← B2-HFC '1' B2-S/T ← B2-GCI/IOM2 bit 5: '0' B2-GCI/IOM2 ← B2-HFC '1' B2-GCI/IOM2 ← B2-S/T
		7..6	w	unused

RESET sets CONNECT register to all '0's.

The following figure shows the different options for switching the B-channels with the CONNECT register.

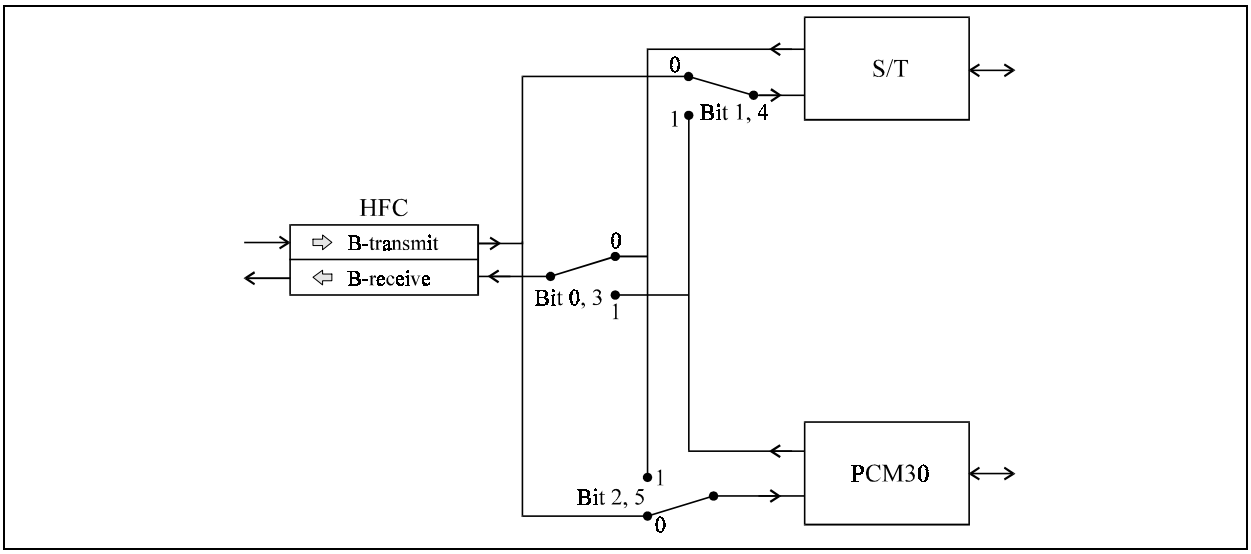


Figure 8: Function of the CONNECT register bits

4.4 Register bit description of auxiliary and cross data registers

Name	Addr.	Bits	r/w	Function
CIRM	60h	2..0	w	defines the length of the auxiliary port access: Value Cycle time (AUX_WR or AUX_RD low) 000b 1 PCI-Clock 001b 3 PCI-Clocks 010b 5 PCI-Clocks 011b 7 PCI-Clocks 100b 9 PCI-Clocks 101b 11 PCI-Clocks 110b 13 PCI-Clocks 111b 15 PCI-Clocks
		3	w	soft reset, similar as hardware reset; the registers CIP, CIRM and CTMT are not changed. The PCI interface is not reset. The reset is active until the bit is cleared. '0' deactivate reset (reset default) '1' activate reset
		5..4	w	must be '0'
		6	w	select bit order for B1 channel '0' normal read/write data operation '1' reverse bit order read/write data operation
		7	w	select bit order for B2 channel '0' normal read/write data operation '1' reverse bit order read/write data operation
FIFO_EN	44h	5..0	w	FIFO enable/disable ('1' = enable (reset default)) Bit FIFO 0 B1-transmit 1 B1-receive 2 B2-transmit 3 B2-receive 4 D-transmit 5 D-receive The enable/disable change becomes valid between 0 and 250µs after the bit has been written. All PCI bus accesses and FIFO activities are disabled for the selected FIFOs. To avoid unnecessary PCI transfers all unused FIFOs should be disabled. **At least one FIFO (usually D-receive) must be enabled.**
		7..6	w	unused, should be '0'

Name	Addr.	Bits	r/w	Function
CTMT	64h	0	w	HDLC/transparent mode for B1-channel '0' HDLC mode (reset default) '1' transparent mode
		1	w	HDLC/transparent mode for B2-channel '0' HDLC mode (reset default) '1' transparent mode
		4..2	w	select timer (bit 4 = MSB) timer '000' off '001' 3.125ms '010' 6.25ms '011' 12.5ms '100' 25ms '101' 50ms '110' 400ms '111' 800ms
		5	w	timer reset mode '0' reset timer by CTMT bit 7 (reset default) '1' automatically reset timer at each access to HFC-S PCI A
		6	w	ignored
		7	w	reset timer '1' reset timer This bit is automatically cleared.
CHIP_ID	58h	0	r	power supply '0' 5V PCI signaling environment '1' 3.3V PCI signaling environment
		3..1	r	reserved
		7..4	r	Chip identification 0011b HFC-S PCI A
B_MODE	4Ch	1..0	w	unused
		2	w	in 64 kbit/s mode: bit is ignored in 56 kbit/s mode: value of the LSB in 7-bit mode
		3	w	unused
		4	w	56 kbit/s mode selection bit for B1-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		5	w	56 kbit/s mode selection bit for B2-channel '0' 64 kbit/s mode (reset default) '1' 56 kbit/s mode
		6	w	'0' Data not inverted for B1-channel (reset default) '1' Data inverted for B1-channel
		7	w	'0' Data not inverted for B2-channel (reset default) '1' Data inverted for B2-channel

Name	Addr.	Bits	r/w	Function
INT_M1	68h	0	w	interrupt mask for channel B1 in transmit direction
		1	w	interrupt mask for channel B2 in transmit direction
		2	w	interrupt mask for channel D in transmit direction
		3	w	interrupt mask for channel B1 in receive direction
		4	w	interrupt mask for channel B2 in receive direction
		5	w	interrupt mask for channel D in receive direction
		6	w	interrupt mask for state change of TE/NT state machine
		7	w	interrupt mask for timer

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits to '0'.

Name	Addr.	Bits	r/w	Function
INT_M2	6Ch	0	w	interrupt mask for processing/non processing phase transition
		1	w	interrupt mask for GCI I-change
		2	w	interrupt mask for GCI monitor receive
		3	w	enable for interrupt output ('1' = enable)
		6..4	w	unused
		7	w	PMESEL '0' PME triggered on D-channel receive int '1' PME triggered on S/T interface state change

For mask bits a '1' enables and a '0' disables interrupt. RESET clears all bits to '0'.

Name	Addr.	Bits	r/w	Function
TRM	48h	1..0	w	interrupt in transparent mode is generated if Z1 in receive FIFOs or Z2 in transmit FIFOs change from: 00: x xxxx x011 1111 → x xxxx x100 0000 01: x xxxx 0111 1111 → x xxxx 1000 0000 10: x xxx0 1111 1111 → x xxx1 0000 0000 11: x 0111 1111 1111 → x 1000 0000 0000
		4..2	w	must be '0'
		5	w	E → B2 receive channel When set the E receive channel of the S/T interface is connected to the B2 receive channel.
		6	w	B1+B2 mode '0' normal operation (reset default) '1' B1+B2 are combined to one HDLC or transparent channel. All settings for data shape and connect are derived from B1. **Both B1 and B2 channel FIFOs must be enabled to use B1+B2 mode.**
		7	w	IOM test loop When set MST output data is looped to the MST input.

Name	Addr.	Bits	r/w	Function
INT_S1	78h	0	r	B1-channel interrupt status in transmit direction
		1	r	B2-channel interrupt status in transmit direction in HDLC mode: '1' a complete frame has been transmitted, the frame counter F2 has been incremented in transparent mode: '1' interrupt as selected in TRM register bits 1..0
		2	r	D-channel interrupt status in transmit direction '1' a complete frame was transmitted, the frame counter F2 was incremented
		3	r	B1-channel interrupt status in receive direction
		4	r	B2-channel interrupt status in receive direction in HDLC mode: '1' a complete frame has been transmitted, the frame counter F1 has been incremented in transparent mode: '1' interrupt as selected in TRM register bits 1..0
		5	r	D-channel interrupt status in receive direction '1' a complete frame was received, the frame counter F1 was incremented
		6	r	TE/NT state machine interrupt status '1' state of state machine changed
		7	r	timer interrupt status '1' timer is elapsed
INT_S2	7Ch	0	r	processing/non processing transition interrupt status '1' The HFC-S PCI A has changed from processing to non processing state.
		1	r	GCI I-change interrupt '1' a different I-value on GCI was detected
		2	r	receiver ready (RxR) of monitor channel '1' 2 monitor bytes have been received
		6..3	r	unused, '0'
		7	r	'1' fatal error: synchronisation lost. PCI performance too low for HFC-S PCI A. Only soft reset recovers from this situation.

☝ **important!**
Reading the INT_S1 or INT_S2 register resets all active read interrupts in the INT_S1 or INT_S2 register. New interrupts may occur during read. These interrupts are reported at the next read of INT_S1 or INT_S2.
All interrupt bits are reported regardless of the mask registers settings (INT_M1 and INT_M2). The mask register settings only influence the interrupt output condition.
The interrupt output goes inactive during the read of INT_S1 or INT_S2. If interrupts occur during this read the interrupt line goes active immediately after the read is finished. So processors with level or transition triggered interrupt inputs can be connected.

Name	Addr.	Bits	r/w	Function
STATUS	70h	0	r	always '0'
		1	r	processing/non processing status '1' the HFC-S PCI A is in processing phase (every 125µs) '0' the HFC-S PCI A is not in processing phase
		2	r	processing/non processing transition interrupt status '1' The HFC-S PCI A has finished internal processing phase (every 125µs)
		3	r	always '0'
		4	r	timer status '0' timer not elapsed '1' timer elapsed
		5	r	TE/NT state machine interrupt state '1' state of state machine has changed
		6	r	FRAME interrupt has occured (any data channel interrupt) all masked D-channel and B-channel interrupts are "ored"
		7	r	ANY interrupt all masked interrupts are "ored"

Reading the STATUS register clears no bit.

5 Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Rating
Supply voltage	V_{DD}	-0.3V to +7.0V
Input voltage	V_I	-0.3V to V_{DD} + 0.3V
Output voltage	V_O	-0.3V to V_{DD} + 0.3V
Operating temperature	T_{opr}	-10°C to +85°C
Storage temperature	T_{stg}	-40°C to +125°C

Recommended operating conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.
Supply voltage	V_{DD}	V_{DD}=5V V_{DD}=3.3V	4.75V 3.15V	5.0V 3.3V	5.25V 3.45V
Operating temperature	T_{opr}		0°C		+70°C

Electrical characteristics for 5V power supply

V_{DD} = 4.75V to 5.25V, T_{opr} = 0°C to +70°C

Parameter	Symbol	Condition	TTL level			CMOS level		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Input LOW voltage	V_{IL}				0.8V			1.0V
Input HIGH voltage	V_{IH}		2.0V			3.5V		
Output LOW voltage	V_{OL}				0.4V			0.4V
Output HIGH voltage	V_{OH}		4.3V			4.3V		
Output leakage current	$\lvert I_{OZ} \rvert$	High Z			10µA			10µA
Pull-up resistor input current	$\lvert I_{IL} \rvert$	$V_I = V_{SS}$		50µA			50µA	

Electrical characteristics for 3.3V power supply

V_{DD} = 3.15V to 3.45V, T_{opr} = 0°C to +70°C

Parameter	Symbol	Condition	TTL level			CMOS level		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Input LOW voltage	V_{IL}				0.8V			1.0V
Input HIGH voltage	V_{IH}		2.0V			2.3V		
Output LOW voltage	V_{OL}				0.4V			0.4V
Output HIGH voltage	V_{OH}		2.4V			2.4V		

DC current consumption of HFC-S PCI A

25°C ambient temperature, 5 V operating voltage, 33 MHz PCI clock

Condition	MIN.	TYP.	MAX.
PCI master, PCM master (full operational)		24,5 mA	
power down, no S/T awake (12.288 MHz OSC off)		15 mA	
All pins GND (except power supply)			1 mA

I/O Characteristics

Input	Interface Level
AD0-31	PCI
PAR	PCI
C/BE0-3	PCI
RST#	PCI
FRAME#	PCI
IRDY#	PCI
TRDY#	PCI
STOP#	PCI
IDSEL	PCI
DEVSEL#	PCI
GNT#	PCI
PERR#	PCI
DAUX0-7	TTL
C4IO	TTL, internal pull-up resistor
F0IO	TTL, internal pull-up resistor
STIO1-2	TTL, internal pull-up resistor
EE_SDA	TTL, internal pull-up resistor
EE_SCL/EN	TTL, internal pull-up resistor

	Driver Capability		
	Low		High
Output	0.4V	0.6V	V_{DD} - 0.4V
AD0-31 *)	6mA		3mA
PAR *)	6mA		3mA
C/BE0-3 *)	6mA		3mA
FRAME# *)	6mA		3mA
IRDY# *)	6mA		3mA
TRDY# *)	6mA		3mA
STOP# *)	6mA		3mA
DEVSEL# *)	6mA		3mA
REQ# *)	6mA		3mA
PERR# *)	6mA		3mA
SERR# *)	6mA		3mA
PME	2mA		1mA
INTA# *)	6mA		3mA
DAUX0-7	4mA		2mA
/AUX_WR	2mA		1mA
/AUX_RD	2mA		1mA
/ADR_WR	8mA		4mA
TX2_HI	6mA		3mA
/TX1_LO	6mA		3mA
/TX_EN	4mA		2mA
/TX2_LO	6mA		3mA
TX1_HI	6mA		3mA
ADJ_LEV	1mA		0.5mA
C4IO	8mA		4mA
F0IO	8mA		4mA
STIO1-2	8mA		4mA
F1_A-B	6mA		3mA
EE_SDA	1mA		0.5mA
EE_SCL/EN	1mA		0.5mA

*) PCI buffer is PCI Spec. 2.2 compliant.

6 Timing characteristics

6.1 PCI bus timing

The timing characteristics of the HFC-S PCI As integrated PCI bus interface is compliant with version 2.1 of the PCI Local Bus specification.

6.2 GCI/IOM2 bus clock and data alignment for Mitel ST™ bus

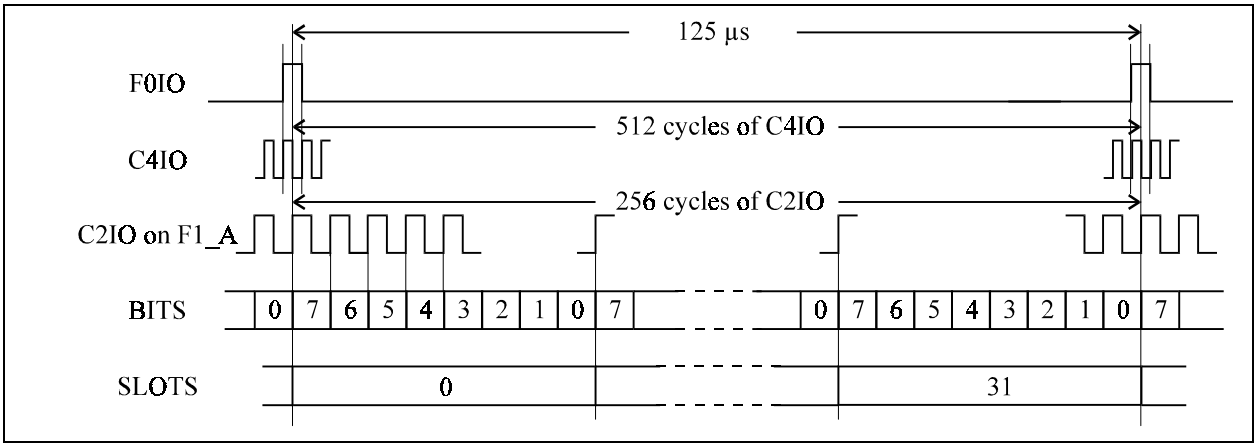
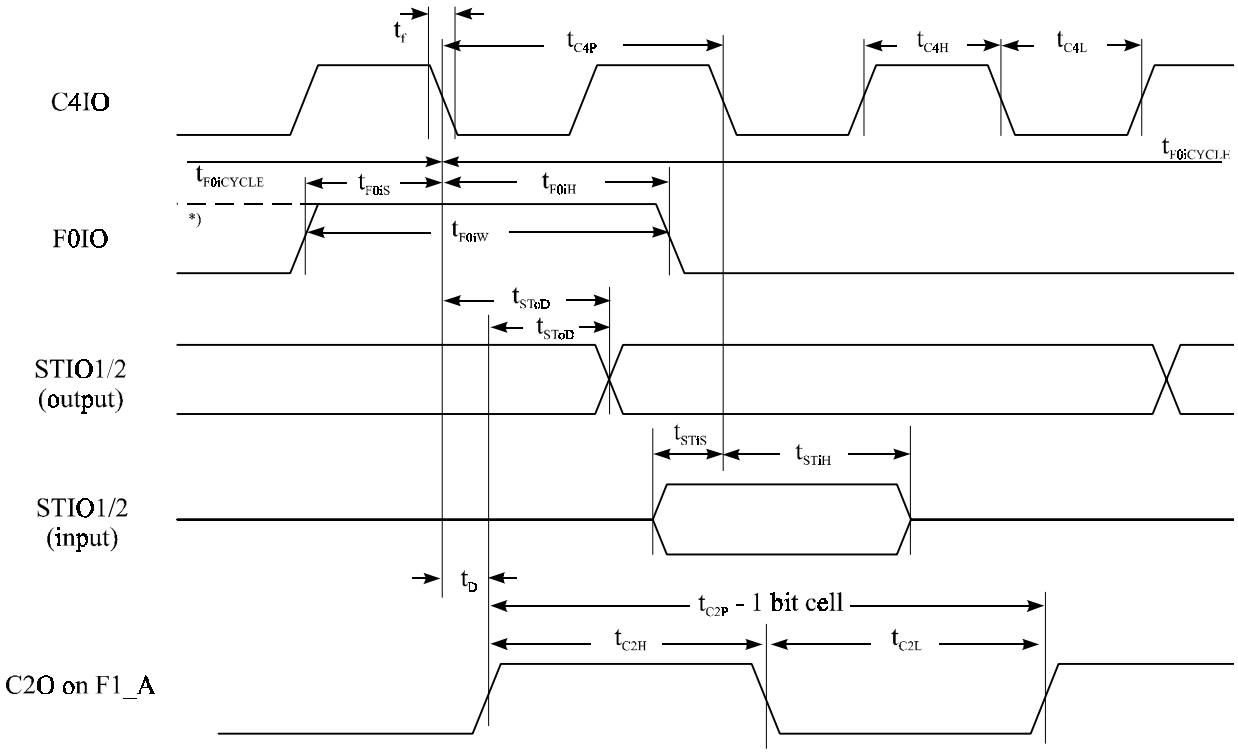


Figure 9: GCI/IOM2 bus clock and data alignment

6.3 GCI/IOM2 timing



Timing diagram 1: GCI/IOM2 timing

*) F0IO starts one C4IO clock earlier if bit 3 in MST_MODE register is set. If this bit is set F0IO is also awaited one C4IO clock cycle earlier.

6.3.1 Master mode

To configure the HFC-S PCI A as GCI/IOM2 bus master bit 0 of the MST_MODE register must be set. In this case C4IO and F0IO are outputs.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.
t_{C4P}	Clock C4IO period (4.096 MHz)	180 ns *)	244.14 ns*)	308 ns*)
t_{C4H}	Clock C4IO High Width	78 ns *)	122 ns *)	166 ns*)
t_{C4L}	Clock C4IO Low Width	78 ns *)	122 ns *)	166 ns *)
t_{C2P}	Clock C2O Period	360 ns	488.28 ns	616 ns
t_{C2H}	Clock C2O High Width	180 ns	244.14 ns	308 ns
t_{C2L}	Clock C2O Low Width	180 ns	244.14 ns	308 ns

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.
t_{F0iW}	F0IO Width	Short F0IO	230 ns	244 ns	260 ns
		Long F0IO	460 ns	488 ns	520 ns
t_{STOD}	STIO1/2 Delay fom C4IO ↓ Level 1 Output			10 ns	25 ns
$t_{F0iCYCLE}$	F0IO Cycle Time	1 half clock adjust	124.955 us	125.000 us	125.045 us
		2 half clocks adjust	124.910 us	125.000 us	125.090 us

All specifications are for 2.048 Mb/s Streams and f_{CLK} = 12.288 Mhz.

*) Time depends on accuracy of OSC_IN frequency. Because of clock adjustment in the 31st time slot these are the worst case timings when C4IO is adjusted.

6.3.2 Slave mode

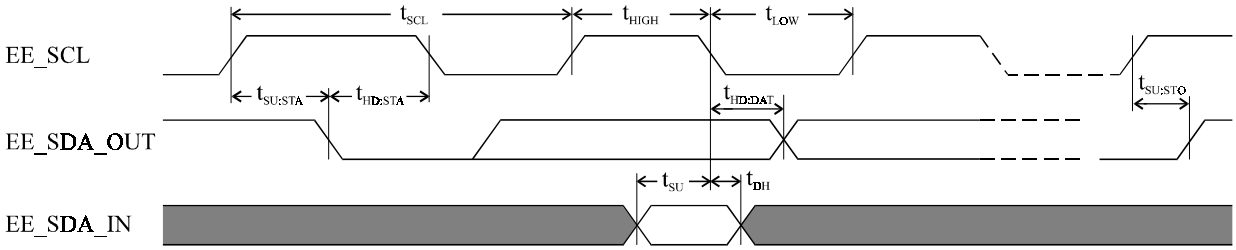
To configure the HFC-S PCI A as GCI/IOM2 bus slave bit 0 of the MST_MODE register must be cleared (reset default). In this case C4IO and F0IO are inputs.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.
t_{C4P}	Clock C4IO period (4.096 MHz)		244.14 ns*)	
t_{C4H}	Clock C4IO High Width	20 ns		
t_{C4L}	Clock C4IO Low Width	20 ns		
t_{C2P}	Clock C2O Period		488.28 ns*)	
t_{C2H}	Clock C2O High Width	25 ns		
t_{C2L}	Clock C2O Low Width	25 ns		
t_{F0iS}	F0IO Setup Time to C4IO ↓	20 ns		
t_{F0iH}	F0IO Hold Time after C4IO ↓	20 ns		
t_{F0iW}	F0IO Width	40 ns		
t_{STiS}	STIO2 Setup Time	20 ns		
t_{STiH}	STIO2 Hold Time	20 ns		

All specifications are for 2.048 Mb/s Streams and f_{CLK} = 12.288 Mhz.

*) If the S/T interface is synchronized from C4IO (NT mode) the frequency must be stable to $\pm 10^{-4}$.

6.4 EEPROM access



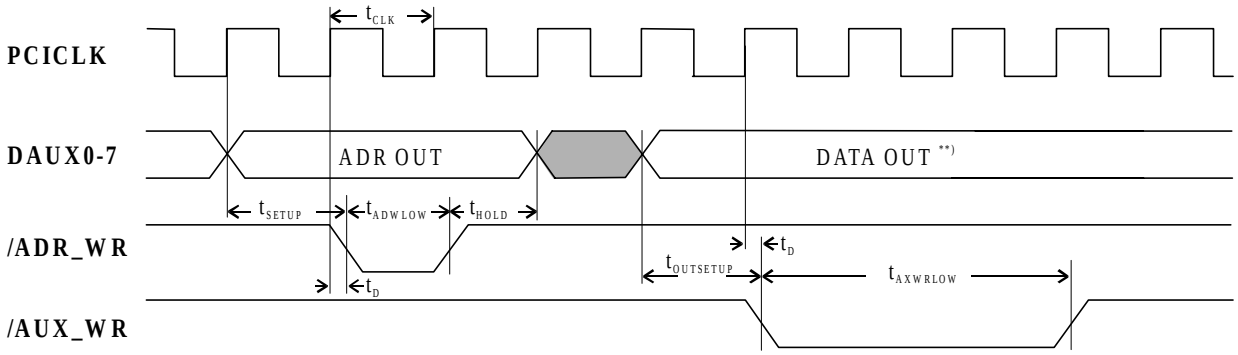
Timing diagram 2: EEPROM access

SYMBOL	CHARACTERISTICS	TYP.
f_{SCL}	Serial Clock Frequency	32.2 KHz *)
t_{SCL}	Serial Clock Period	1 / f_{SCL}
$t_{HD:STA}$	Start Condition Hold Time	¾ t_{SCL}
t_{LOW}	Clock Low Period	½ t_{SCL}
t_{HIGH}	Clock High Period	½ t_{SCL}
$t_{SU:STA}$	Start Condition Setup Time	¾ t_{SCL}
$t_{HD:DAT}$	Output Data Change after Clock ↓	10 ns
t_{SU}	Data In Setup Time	100 ns
t_{DH}	Data In Hold Time	100 ns

*) with 33 MHz PCI clock

6.5 Auxiliary port access

6.5.1 Write access



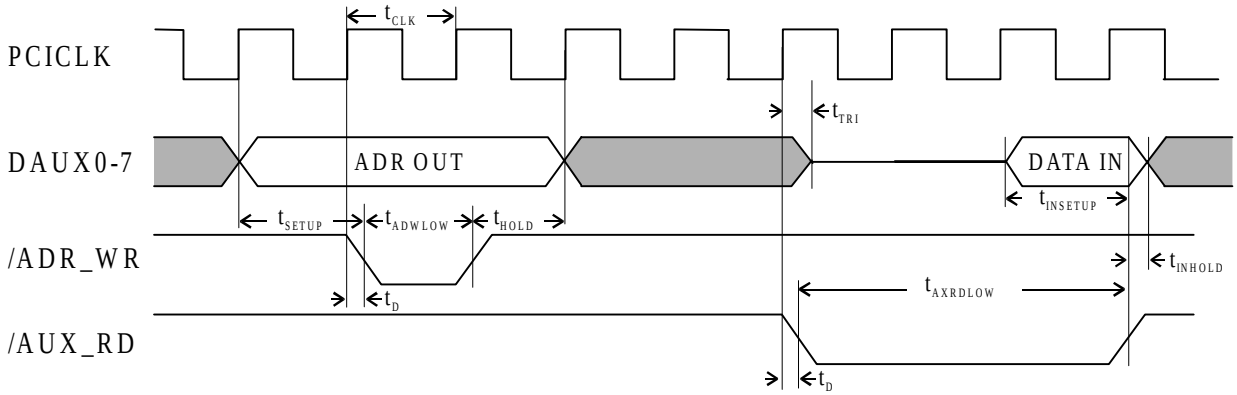
Timing diagram 3: Auxiliary port write access

SYMBOL	CHARACTERISTICS	TYP.
t_{CLK}	PCI Clock Period (33 MHz)	30 ns
t_{SETUP}	Address Setup Time before /ADR_WR ↓	t_{CLK}
t_{ADWLOW}	/ADR_WR Low Time	t_{CLK}
t_{HOLD}	Address Hold Time after /ADR_WR ↑	t_{CLK}
$t_{OUTSETUP}$	Data Out Setup Time before /AUX_WR ↓	t_{CLK}
t_{AXWLOW}	/AUX_WR Low Time	3 x t_{CLK} *)
t_D	Delay Time between PCICLK ↑ and /ADR_WR ↓ or /AUX_WR ↓	10 ns

*) configurable (see also: CIRM register bit description)

**) data out is valid until the next auxiliary port write access is initiated

6.5.2 Read access



Timing diagram 4: Auxiliary port read access

SYMBOL	CHARACTERISTICS	TYP.
t_{CLK}	PCI Clock Period (33 MHz)	30 ns
t_{SETUP}	Address Setup Time before /ADR_WR ↓	t_{CLK}
t_{ADWLOW}	/ADR_WR Low Time	t_{CLK}
t_{HOLD}	Address Hold Time after /ADR_WR ↑	t_{CLK}
$t_{INSETUP}$	Minimum Data In Setup Time before /AUX_RD ↑	20 ns
$t_{AXRDLOW}$	/AUX_RD Low Time	3 x t_{CLK} *)
t_{INHOLD}	Data In Hold Time after /AUX_RD ↑	0 ns
t_D	Delay Time between PCICLK ↑ and /ADR_WR ↓ or /AUX_RD ↓	10 ns
t_{TRI}	Time Data Floating after PCICLK ↑	20 ns

*) configurable (see also: CIRM register bit description)

7 S/T interface circuitry

In order to comply to the physical requirements of ITU-T recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the HFC-S PCI A needs some additional circuitry, which are shown in the following figures.

7.1 External receiver circuitry

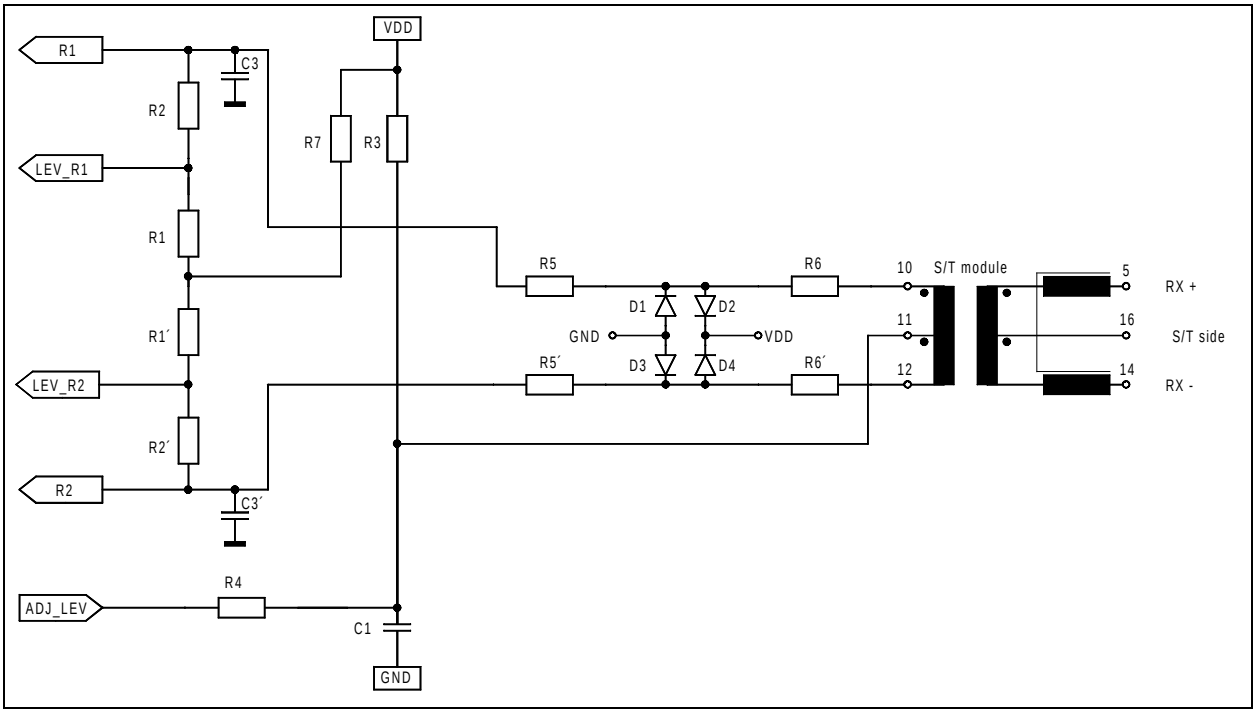


Figure 10: External receiver circuitry

Part list

VDD	**5V**	**3.3V**
R1, R1'	33 kΩ	
R2, R2'	100 kΩ	
R3	1 MΩ	680kΩ
R4	3.9 kΩ	
R5, R5'	4.7 kΩ	
R6, R6'	4.7 kΩ	
R7	1.8 MΩ	1.2MΩ

C1	47 nF
C3, C3'	22pF
D1, D2	1N4148 or LL4148
D3, D4	1N4148 or LL4148
S/T module	see Table 5 on page 59.

C3, C3' are for reduction of high frequency input noise and should be located as close as possible to the HFC-S PCI A.

7.2 External transmitter circuitry

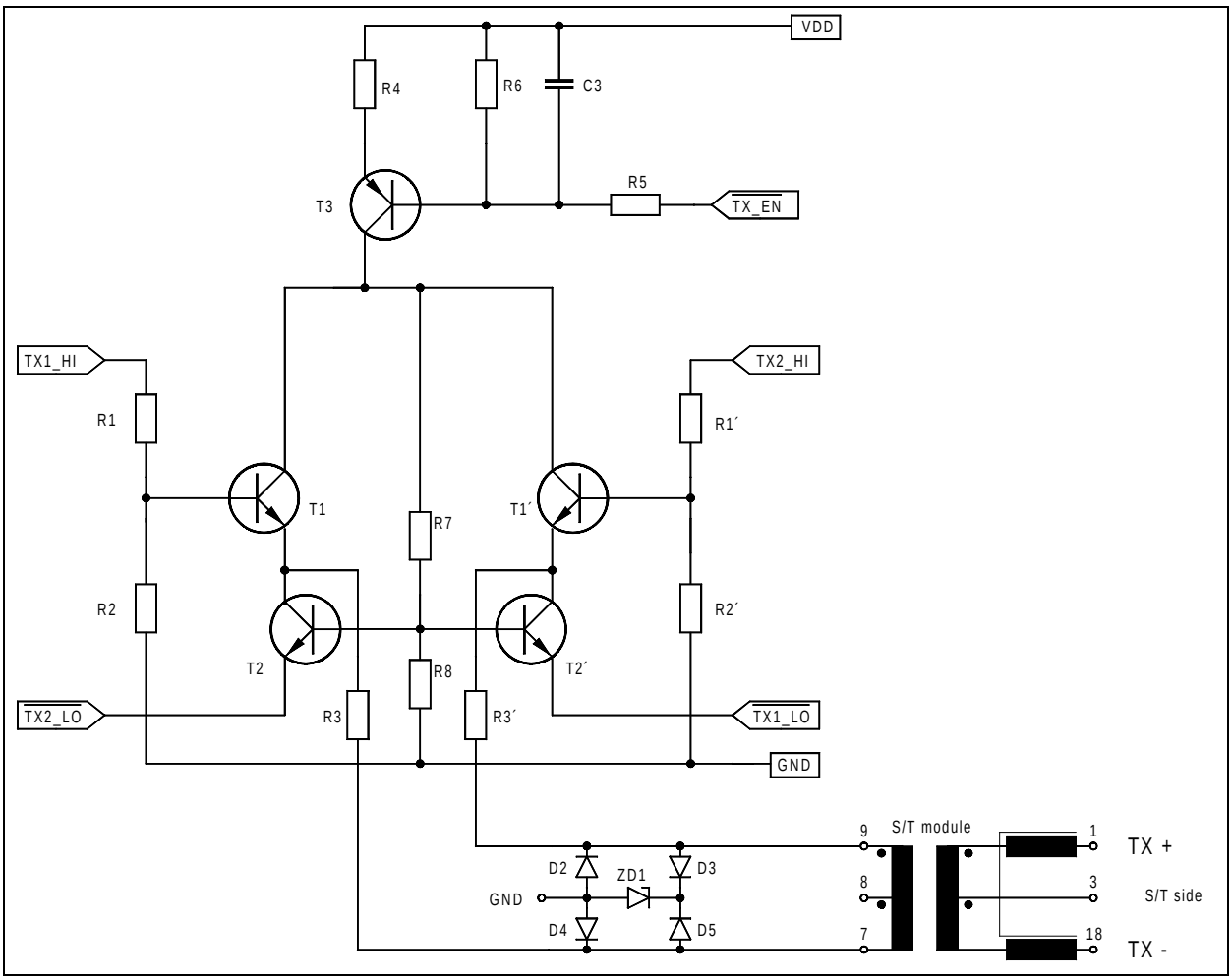


Figure 11: External transmitter circuitry

Part List

VDD	**5V**	**3.3V**
R1	2.2 kΩ ± 1%	560 Ω ± 1%
R2	3.0 kΩ ± 1%	3.9 kΩ ± 1%
R3, R3' *)	18 Ω	18 Ω
R4	100 Ω	50 Ω
R5	5.6 kΩ	3.3 kΩ
R6	3.3 kΩ	2.2 kΩ
R7	3.3 kΩ	1.8 kΩ
R8	2.2 kΩ	2.2 kΩ

C3	470 pF
D2, D3	1N4148 or LL4148
D4, D5	1N4148 or LL4148
ZD1	Z-Diode 2.7 V (e. g. BZV 55C 2V7)
T1, T1'	BC550C, BC850C or similar
T2, T2'	BC550C, BC850C or similar
T3	BC560C, BC860C or similar
S/T module	see Table 5 on page 59.

*) value is depending on the used S/T module

S/T module part number	manufacturer
APC 56624-1 APC 40495S (SMD) S-Hybrid modules with receiver and transmitter circuitry included: APC 5568-3V APC 5568-5V APC 5568DS-3V APC 5568DS-5V	**Advanced Power Components** *United Kingdom* Phone: +44 1634-290588 Fax: +44 1634-290591 http://www.apcisdn.com
FE 8131-55Z	**FEE GmbH** *Singapore* Phone: +65 741-5277 Fax: +65 741-3013 *Bangkok* Phone: +662 718-0726-30 Fax: +662 718-0712 *Germany* Phone: +49 6106-82980 Fax: +49 6106-829898
transformers: PE-64995 PE-64999 PE-65795 (SMD) PE-65799 (SMD) PE-68995 PE-68999 T5006 (SMD) T5007 (SMD) S_0-modules: T5012 T5034 T5038	**Pulse Engineering, Inc.** *United States* Phone: +1-619-674-8100 Fax: +1-619-674-8262 http://www.pulseeng.com
transformers: SM TC-9001 SM ST-9002 SM ST-16311F S_0-modules: SM TC-16311 SM TC-16311A	**Sun Myung** *Korea* Phone: +82-348-943-8525 Fax: +82-348-943-8527 http://www.sunmyung.com
transformers UT21023 S_0-modules: UT 20795 (SMD) UT 21624 UT 28624 A	**UMEC GmbH** *Germany* Phone: +49 7131-7617-0 Fax: +49 7131-7617-20 *Taiwan* Phone: +886-4-359-009-6 Fax: +886-4-359-012-9 *United States* Phone: +1-310-326-707-2 Fax: +1-310-326-705-8 http://www.umec.de

S/T module part number	manufacturer
T 6040... transformers: 3-L4021-X066 3-L4025-X095 3-L5024-X028 3-L4096-X005 3-L5032-X040 S_0-modules: 7-L5026-X010 (SMD) 7-L5051-X014 7-M5051-X032 7-L5052-X102 (SMD) 7-M5052-X110 7-M5052-X114	**VAC GmbH** *Germany* Phone: +49 6181/ 38-0 Fax: +49 6181/ 38-2645 http://www.vacuumschmelze.de
transformers: ST5069 S_0-modules: PT5135 ST5201 ST5202	**Valor Electronics, Inc.** *Asia* Phone: +852 2333-0127 Fax: +852 2363-6206 *North America* Phone: +1 800 31VALOR Fax: +1 619 537-2525 *Europe* Phone: +44 1727-824-875 Fax: +44 1727-824-898 http://www.valorinc.com
543 76 009 00 503 740 010 0 (SMD)	**Vogt electronic AG** *Germany* Phone: +49 8591/ 17-0 Fax: +49 8591/ 17-240 http://www.vogt-electronic.com

Table 5: S/T module part numbers and manufacturer

7.3 Oscillator circuitry

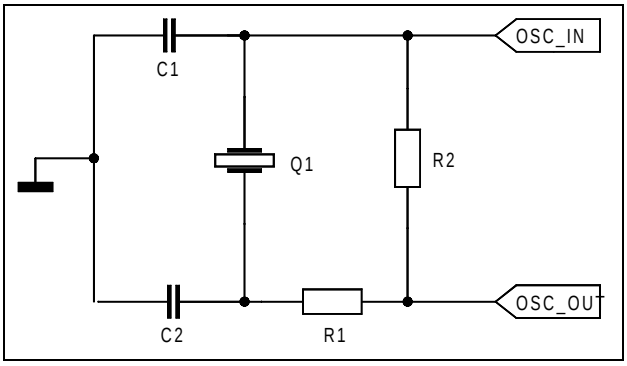


Figure 12: Oscillator Circuitry

Part list:

Q1	12.288 MHz quartz
R1	0..50 Ω
R2	1 MΩ
C1, C2	47 pF

The values of C1, C2 and R1 depend on the used quartz.

For a load-free check of the oscillator frequency the C4O clock of the GCI/IOM2 bus should be measured (HFC-S PCI A as master, S/T interface deactivated, 4.096 MHz frequency intented on the C4IO).

7.4 EEPROM circuitry

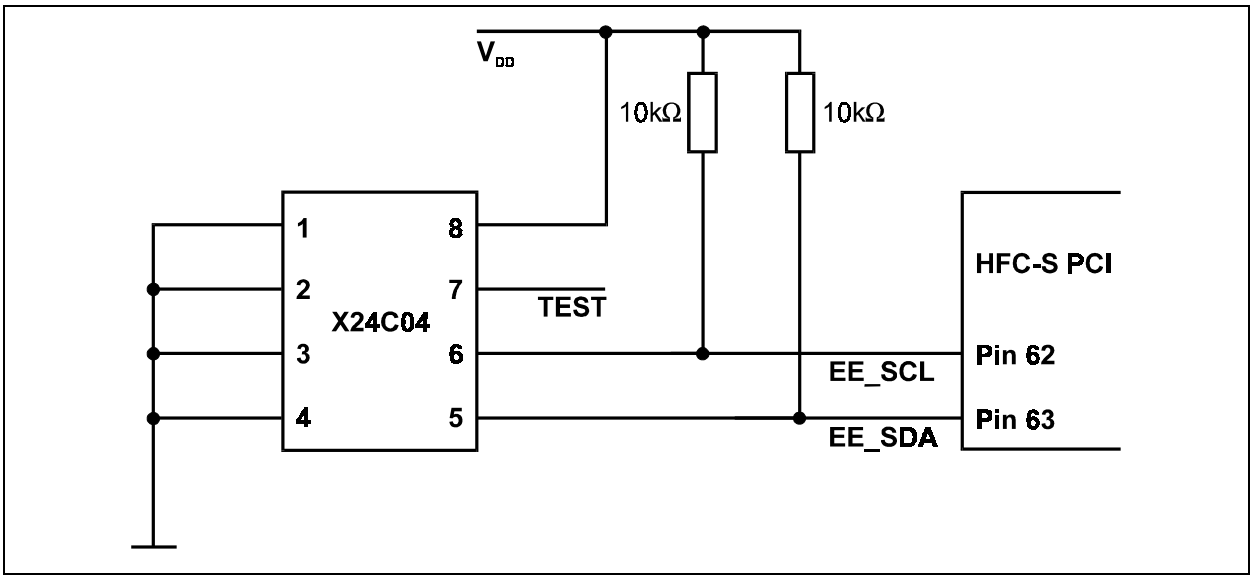


Figure 13: EEPROM circuitry

7.5 PME pin circuitry

The PME pin (pin 53) on the HFC-S PCI A is high active. To connect it to the low active PME# pin on the PCI bus, the following circuitry is neccessary.

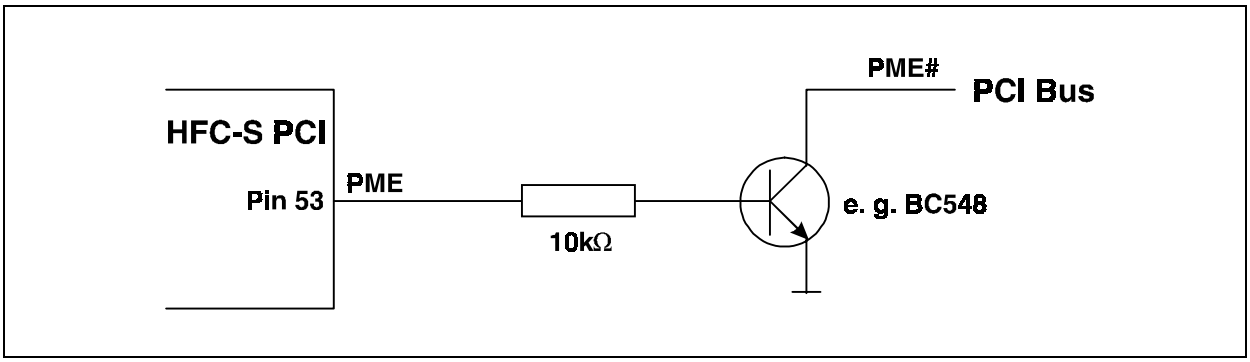


Figure 14: PME pin circuitry

8 State matrices for NT and TE

8.1 S/T interface activation/deactivation layer 1 for finite state matrix for NT

State name / State number / Event / INFO sent	Reset	Deactive	Pending activation	Active	Pending deactivation
State number	G0	G1	G2	G3	G4
INFO sent	INFO 0	INFO 0	INFO 2	INFO 4	INFO 0
State machine release (Note 3)	G2	|	|	|	|
Activate request	G2 (Note 1)	G2 (Note 1)	|	|	G2 (Note 1)
Deactivate request	—	|	Start timer T2 G4	Start timer T2 G4	|
Expiry T2 (Note 2)	—	—	—	—	G1
Receiving INFO 0	—	—	—	G2	G1
Receiving INFO 1	—	G2 (Note 1)	—	/	—
Receiving INFO 3	—	/	G3 (Note 1)	—	—

Table 6: Activation/deactivation layer 1 for finite state matrix for NT

— No state change
/ Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
| Impossible by the definition of the physical layer service

Note 1: Timer 1 (T1) is not implemented in the HFC-S PCI A and must be implemented in software.

Note 2: Timer 2 (T2) prevents unintentional reactivation. Its value is 32ms (256 x 125µs). This implies that a TE has to recognize INFO 0 and to react on it within this time.

Note 3: After reset the state machine is fixed to G0.

> ☝ **hint!**
>
> Fix the NT state machine to state G3 when activated (by writing 13h into STATES register). This prevents deactivation of NT mode S/T interface due to sporadically errors on NT input data.

8.2 Activation/deactivation layer 1 for finite state matrix for TE

Event \ State name		Reset	Sensing	Deactivated	Awaiting signal	Identifying input	Synchronized	Activated	Lost framing
State number		F0	F2	F3	F4	F5	F6	F7	F8
Info sent		INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
State machine release (Note 1)		F2	/	/	/	/	/	/	/
Activate Request	Receiving any signal	—	|	F5	|	|	—	|	—
	Receiving INFO 0	—	|	F4	|	|	—	|	—
Expiry T3 (Note 5)		—	/	—	F3	F3	F3	—	—
Receiving INFO 0		—	F3	—	—	—	F3	F3	F3
Receiving any signal (Note 2)		—	—	—	F5	—	/	/	—
Receiving INFO 2 (Note 3)		—	F6	F6	F6	F6	—	F6	F6
Receiving INFO 4 (Note 3)		—	F7	F7	F7	F7	F7	—	F7
Lost framing (Note 4)		—	/	/	/	/	F8	F8	—

Table 7: Activation/deactivation layer 1 for finite state matrix for TE

— No change, no action
| Impossible by the definition of the layer 1 service
/ Impossible situation

Notes

Note 1: After reset the state machine is fixed to F0.

Note 2: This event reflects the case where a signal is received and the TE has not (yet) determined wether it is INFO 2 or INFO 4.

Note 3: Bit- and frame-synchronisation achieved.

Note 4: Loss of Bit- or frame-synchronisation.

Note 5: Timer 3 (T3) is not implemented in the HFC-S PCI A and must be implemented in software.

9 Binary organisation of the frames

9.1 S/T frame structure

The frame structures are different for each direction of transmission. Both structures are illustrated in Figure 15.

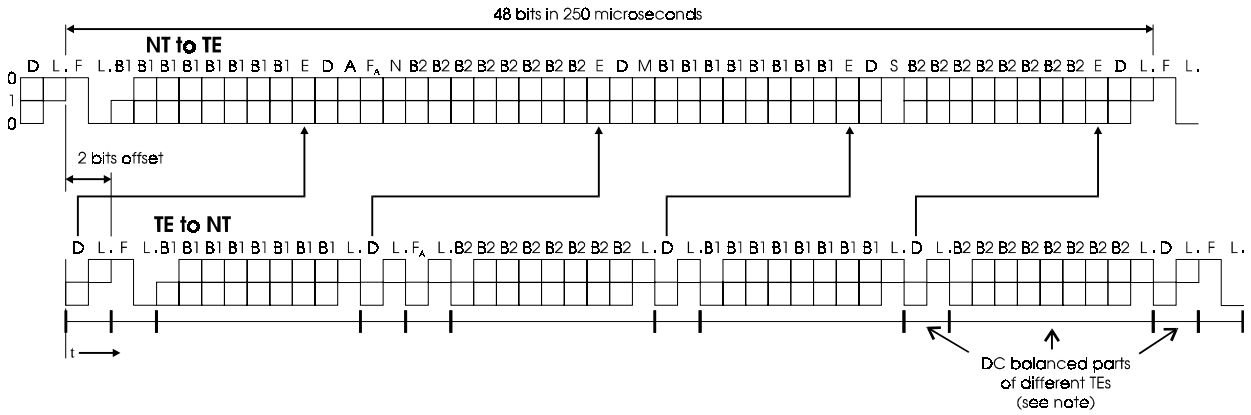


Figure 15: Frame structure at reference point S and T

F	Framing bit	N	Bit set to a binary value N = $\overline{F}_A$ (NT to TE)
L	D.C. balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit	S	S-channel bit
M	Multiframing bit		

☝ **note!**
Lines demarcate those parts of the frame that are independently d.c.-balanced.
The F_A bit in the direction TE to NT is used as Q bit in every fifth frame if S/Q bit transmission is enabled (see SCTRL register).
The nominal 2-bit offset is as seen from the TE. The offset can be adjusted with the CLKDEL register in TE mode. The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.
HDLC-B-channel data start with the LSB, PCM-B-channel data start with the MSB.

9.2 GCI frame structure

The binary organistation of a single GCI channel frame is described below. C4IO clock frequency is 4.096MHz.

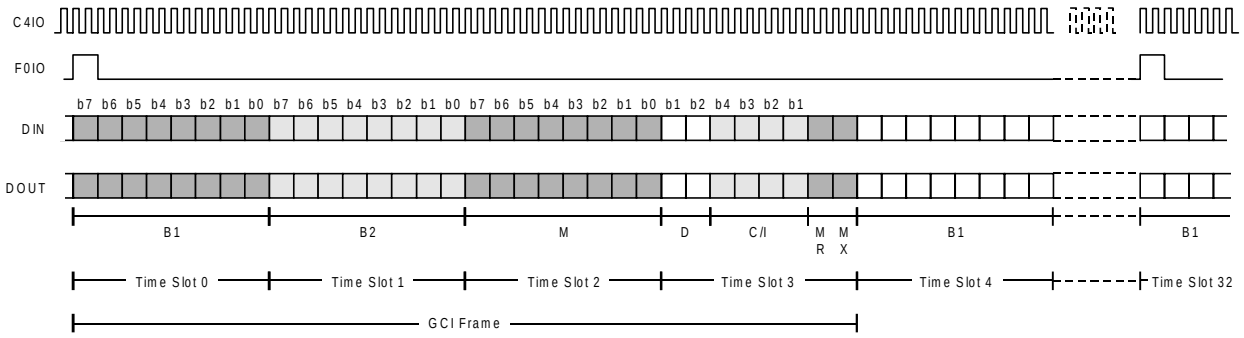


Figure 16: Single channel GCI format

B1 B-channel 1 data
B2 B-channel 2 data
M Monitor channel data
D D-channel data
C/I Command/indication bits for controlling activation/deactivation and for additional control functions
MR Handshake bit for monitor channel
MX Handshake bit for monitor channel

10 Clock synchronisation

10.1 Clock synchronisation in NT-mode

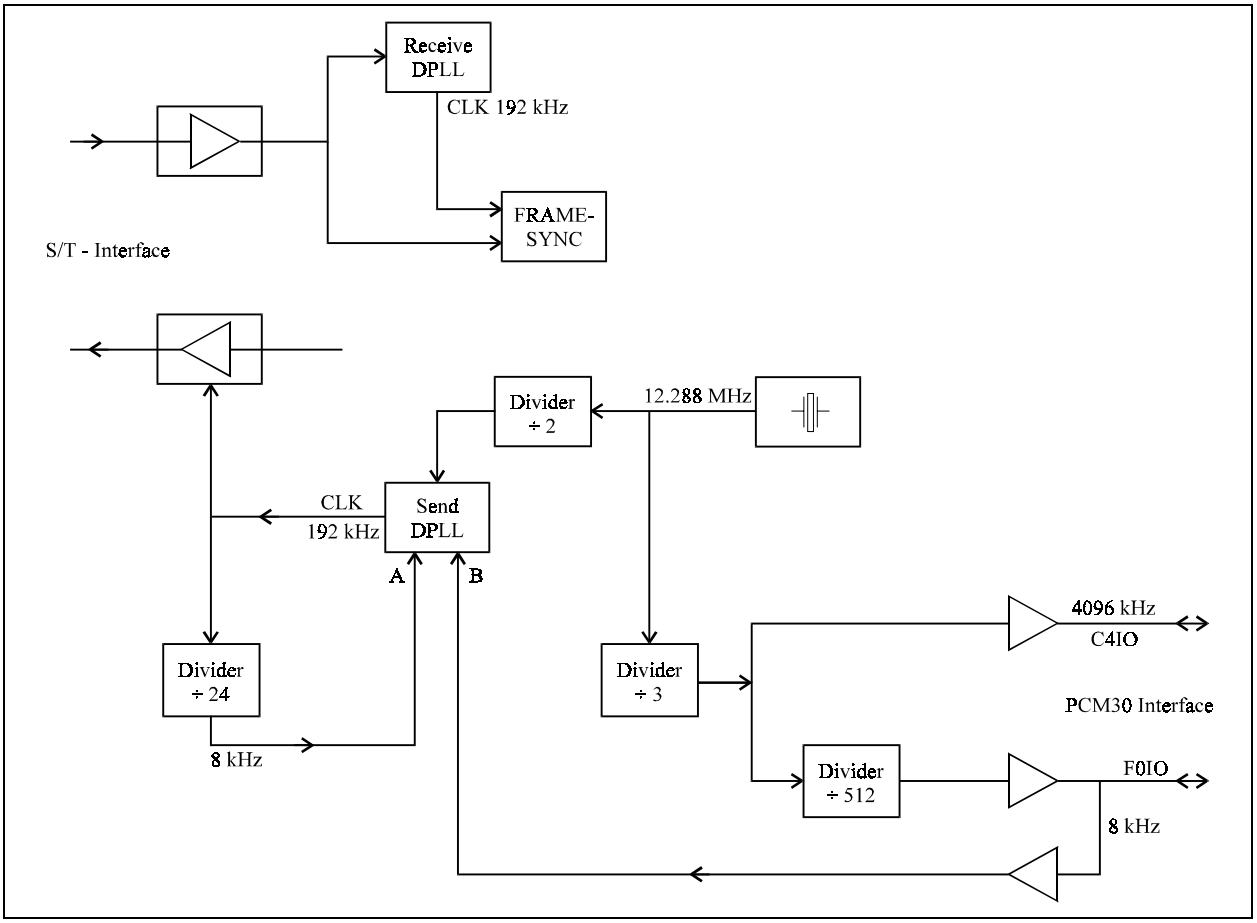


Figure 17: Clock synchronisation in NT-mode

10.2 Clock synchronisation in TE-mode

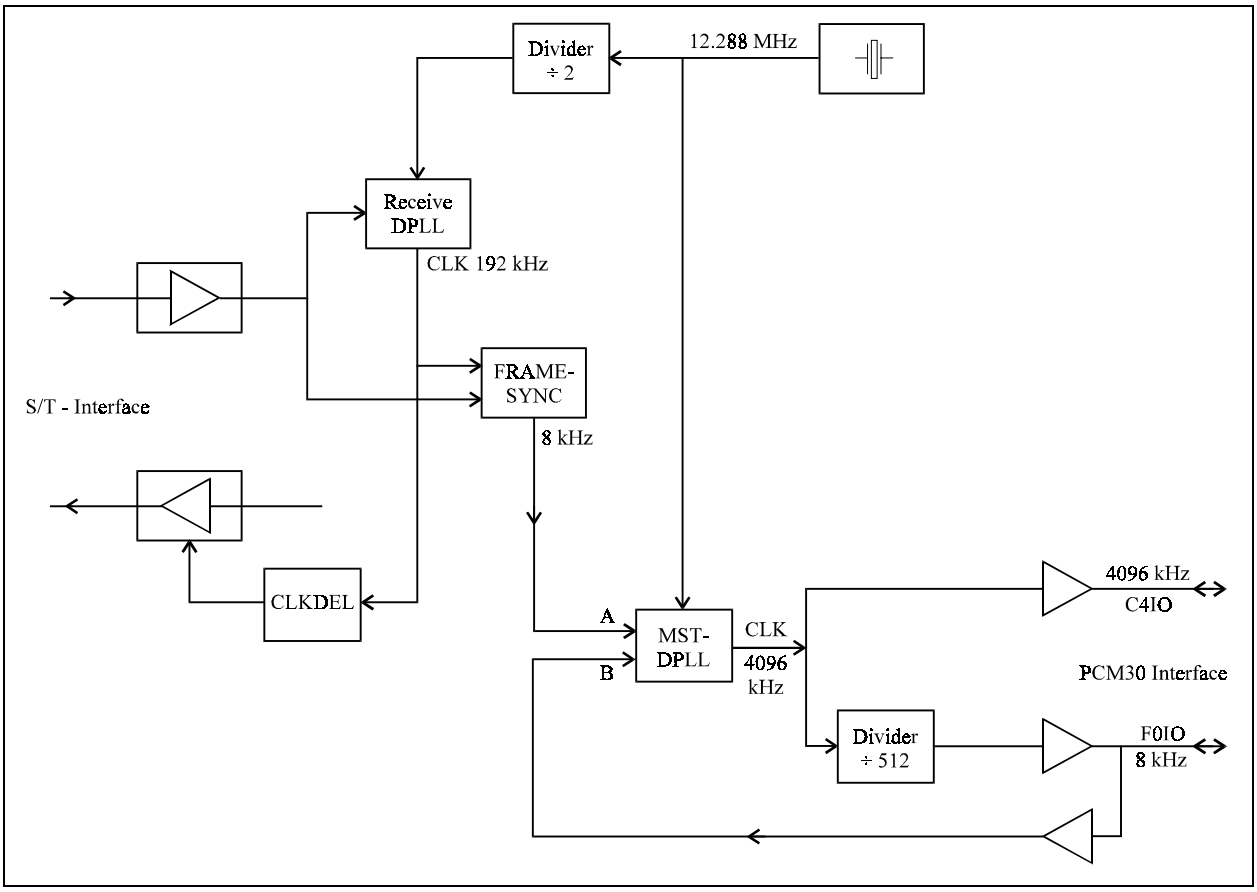


Figure 18: Clock synchronisation in TE-mode

The C4IO clock is adjusted in the 31th time slot at the GCI/IOM bus twice for one half clock cycle. This can be reduced to one adjustment of a half clock cycle. This is useful if another HFC-S, HFC-S+, HFC-SP or HFC-S PCI A is connected as slave in NT mode to the GCI/IOM2 bus.

11 HFC-S PCI A package dimensions

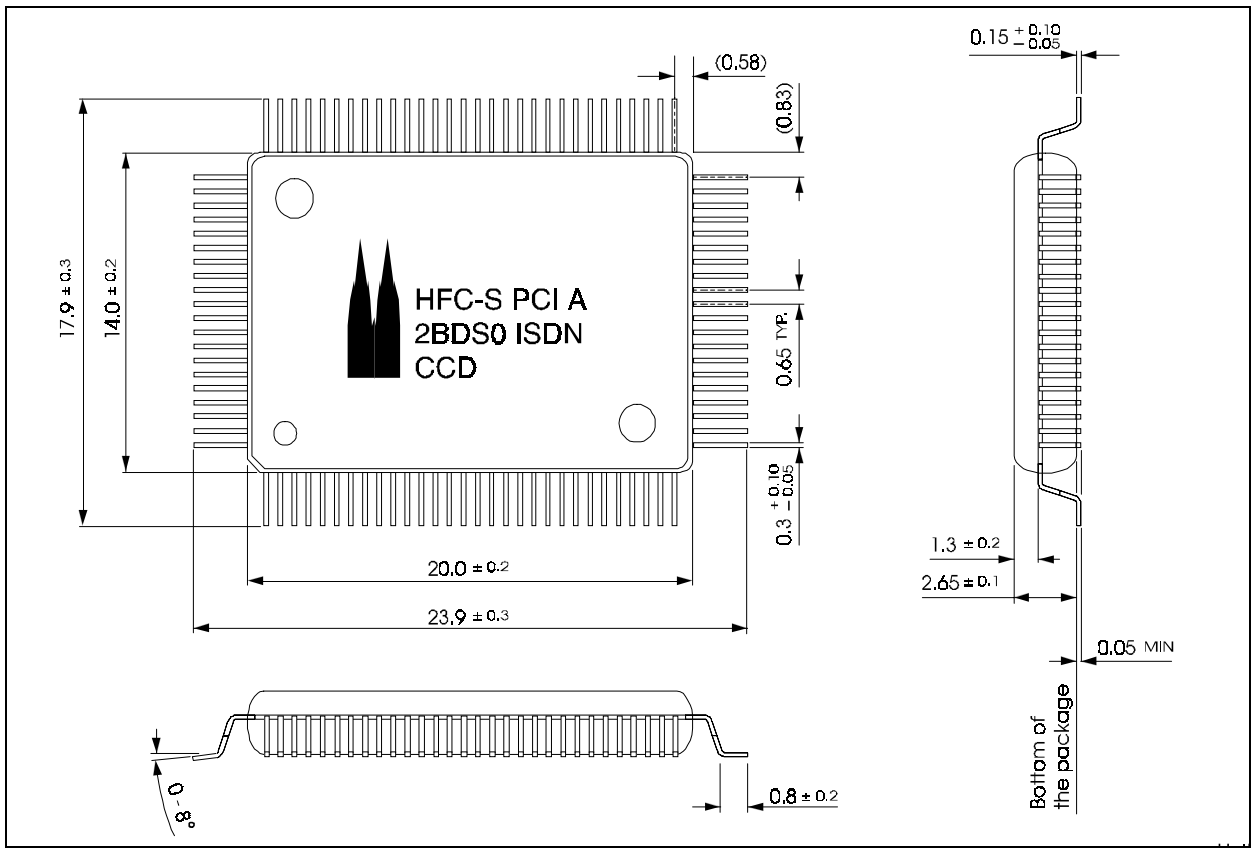
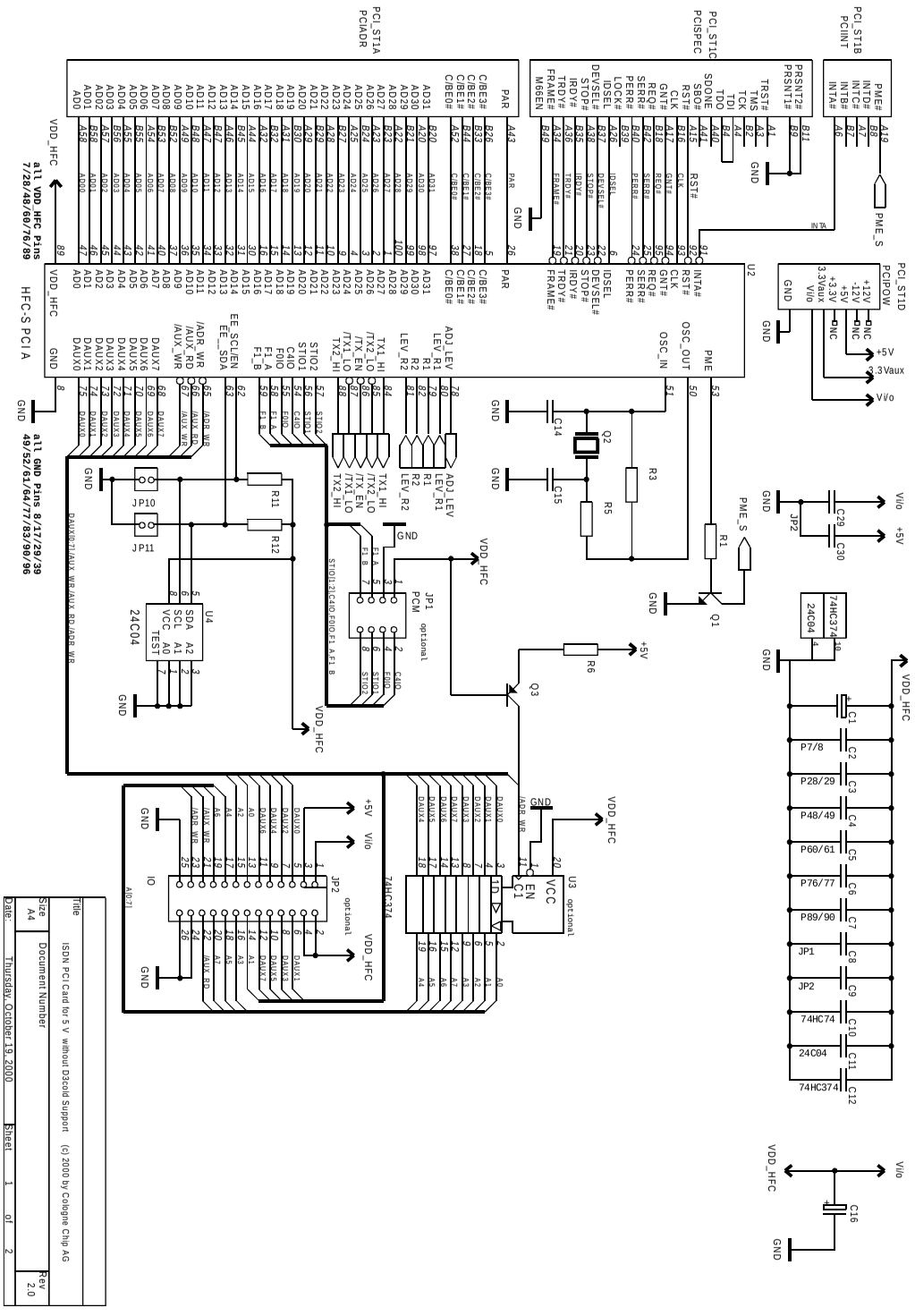


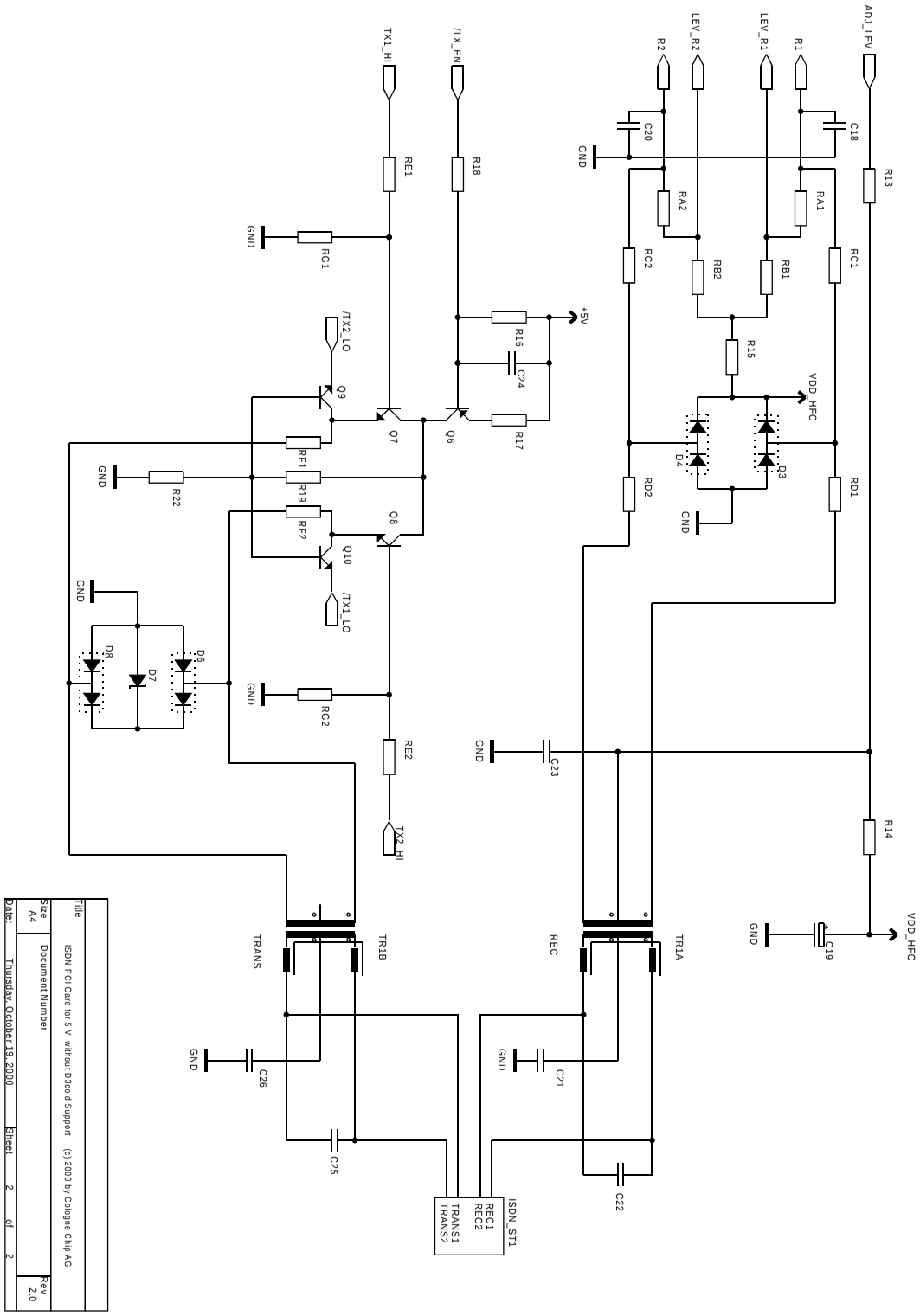
Figure 19: HFC-S PCI A package dimensions

12 ISDN PCI card sample circuitries with HFC-S PCI A

12.1 ISDN PCI card for 5V power supply (no $D3_{cold}$ support)

Please see chapter 3.3 for details on power management support of HFC-S PCI A and special considerations for support of power management state $D3_{cold}$.





Size A4	Title	ISDN PCI Card for 5 V without D3cold Support (c) 2000 by Cologne Chip AG
Document Number		Rev 2.0
Date: Thursday, October 19, 2000	Sheet 2 of 2	

ISDN PCI Card for 5 V without D3cold support

Capacitors

C01	33µ	
C02	33n	nearby U2
C03	33n	nearby U2
C04	33n	nearby U2
C05	33n	nearby U2
C06	33n	nearby U2
C07	33n	nearby U2
C08	33n	nearby JP1 *optional*
C09	33n	nearby JP2 *optional*
C10	33n	nearby U1
C11	33n	nearby U4
C12	33n	nearby U3 *optional*
C14	47p	depends on crystal
C15	47p	depends on crystal
C16	33µ	
C18	22p	nearby U2
C19	33µ	
C20	22p	nearby U2
C21	0	*optional*
C22	0	*optional*
C23	47n	
C24	470p	
C25	0	*optional*
C26	0	*optional*
C29	33n	nearby JP2 *optional*
C30	33n	nearby JP2 *optional*
C31	0R	Resistor or connect to GND
C32	0	optional

Resistors

R01	10k	
R03	1M	
R05	330	
R06	10k	
R11	10k	
R12	10k	
R13	3k9	
R14	680k	
R15	1M2	
R16	3k3	
R17	100	
R18	5k6	
R19	3k3	
R22	2k2	
RA1	100k	
RA2	100k	
RB1	33k	
RB2	33k	
RC1	4k7	
RC2	4k7	
RD1	4k7	
RD2	4k7	
RE1	2k2	1%
RE2	2k2	1%
RF1	15	
RF2	15	
RG1	3k	1%
RG2	3k	1%

IC's

U2	HFC-S PCI A	*Cologne Chip AG*
U3	74HC374	*optional*
U4	24C04	

Connectors

JP1	PCM	*optional*
JP2	IO	*optional*
JP10	EEPROM options	*optional*
JP11	EEPROM options	*optional*

Transistors / Crystals

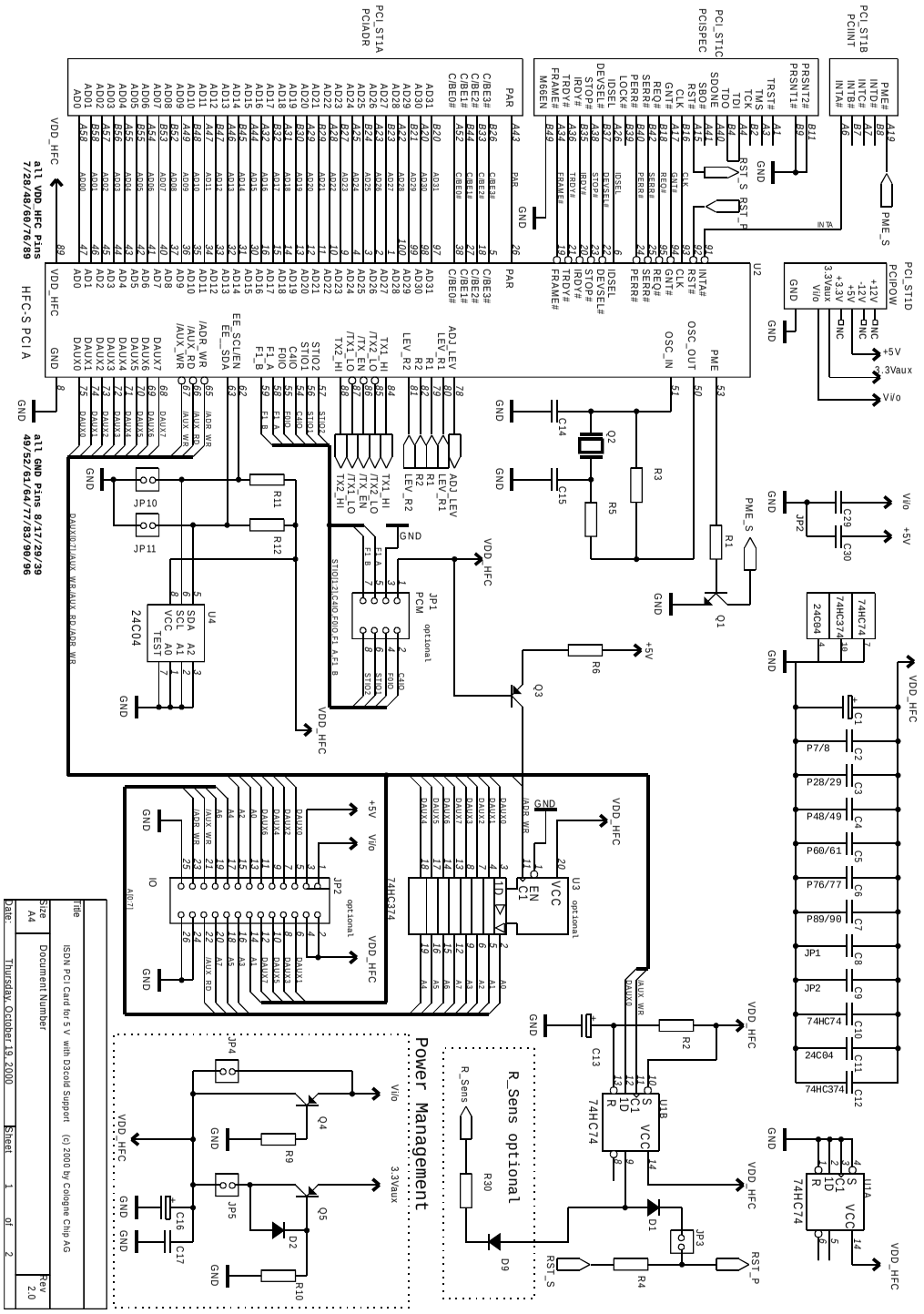
Q1	BC850C	CMPT5088 or similar
Q2	12.288M	
Q3	BC860C	CMPT5087 or similar
Q6	BC860C	CMPT5087 or similar
Q7	BC850C	CMPT5088 or similar
Q8	BC850C	CMPT5088 or similar
Q9	BC850C	CMPT5088 or similar
Q10	BC850C	CMPT5088 or similar

Diodes

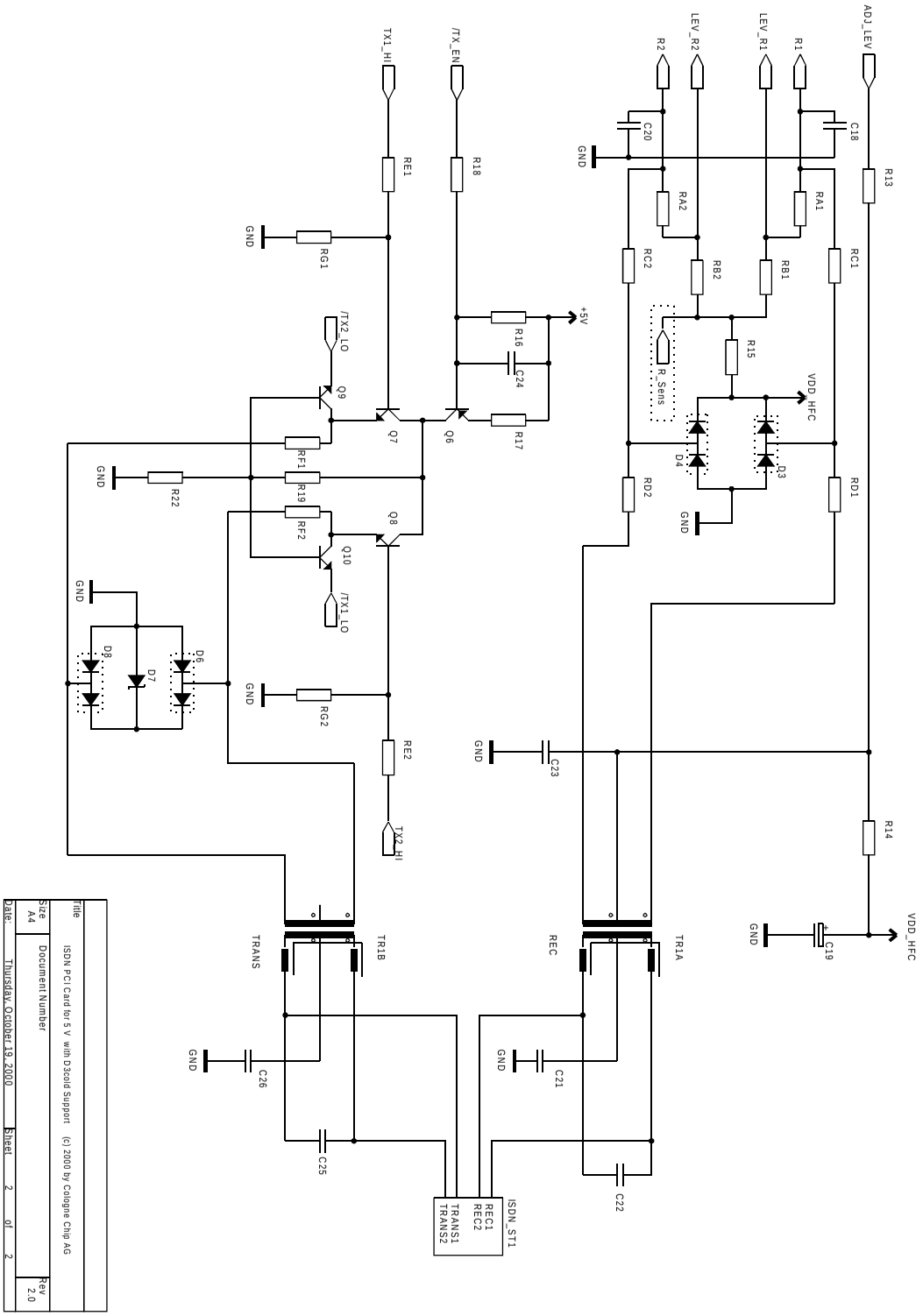
D3	BAV99	can also be 2*4148
D4	BAV99	can also be 2*4148
D6	BAV99	can also be 2*4148
D7	2V7	
D8	BAV99	can also be 2*4148

12.2 ISDN PCI card for 5V power supply with $D3_{cold}$ support

Please see chapter 3.3 for details on power management support of HFC-S PCI A and special considerations for support of power management state $D3_{cold}$.



The R_Sens part is optional. It is used to decrease the receiver sensitivity for wake-up signals to avoid a wake-up caused by disturbance on the ISDN line.


ADJ_LEV
LEV_R1
LEV_R2
R1
R2
C18
C20
GND
R13
RA1
RA2
RB1
RB2
RC1
RC2
R_Sens
R15
VDD_HFC
D3
D4
RD1
RD2
R14
C19
C23
TX1_H
/TX_EN
RE1
R18
RG1
/TX2_LO
Q9
Q7
Q6
R16
C24
+5V
R17
RF1
R19
RF2
R22
Q8
Q10
/TX1_LO
D6
D7
D8
RG2
RE2
TX2_H
TRANS
TR1B
REC
TR1A
C26
C21
C25
C22
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REC2
TRANS1
TRANS2
Title
ISDN PCI Card for 5 V with D3cold Support (c) 2000 by Cologne Chip AG
Size
A4
Document Number
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2.0
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2

ISDN PCI Card for 5 V with D3cold support

Capacitors

C01	33µ	
C02	33n	nearby U2
C03	33n	nearby U2
C04	33n	nearby U2
C05	33n	nearby U2
C06	33n	nearby U2
C07	33n	nearby U2
C08	33n	nearby JP1 *optional*
C09	33n	nearby JP2 *optional*
C10	33n	nearby U1
C11	33n	nearby U4
C12	33n	nearby U3 *optional*
C13	1µ	
C14	47p	depends on crystal
C15	47p	depends on crystal
C16	33µ	
C17	33n	
C18	22p	nearby U2
C19	33µ	
C20	22p	nearby U2
C21	0	*optional*
C22	0	*optional*
C23	47n	
C24	470p	
C25	0	*optional*
C26	0	*optional*
C29	33n	nearby JP2 *optional*
C30	33n	nearby JP2 *optional*
C31	0R	Resistor or connect to GND
C32	0	optional

Diodes

D1	LL4148	or similar
D2	LL4148	or similar
D3	BAV99	can also be 2*4148
D4	BAV99	can also be 2*4148
D6	BAV99	can also be 2*4148
D7	2V7	
D8	BAV99	can also be 2*4148
D9	LL4148 *	or similar

Resistors

R01	10k	
R02	1M	
R03	1M	
R04	10k	
R05	330	
R06	10k	
R09	10k	
R10	10k	
R11	10k	
R12	10k	
R13	3k9	
R14	680k	
R15	1M2	
R16	3k3	
R17	100	
R18	5k6	
R19	3k3	
R22	2k2	
R30	680k *	
RA1	100k	
RA2	100k	
RB1	33k	
RB2	33k	
RC1	4k7	
RC2	4k7	
RD1	4k7	
RD2	4k7	
RE1	2k2	1%
RE2	2k2	1%
RF1	15	
RF2	15	
RG1	3k	1%
RG2	3k	1%

* optional, not on PCB Layout V 2.0

IC's

U1	74HC74	
U2	HFC-S PCI A	Cologne Chip AG
U3	74HC374	*optional*
U4	24C04	

Connectors

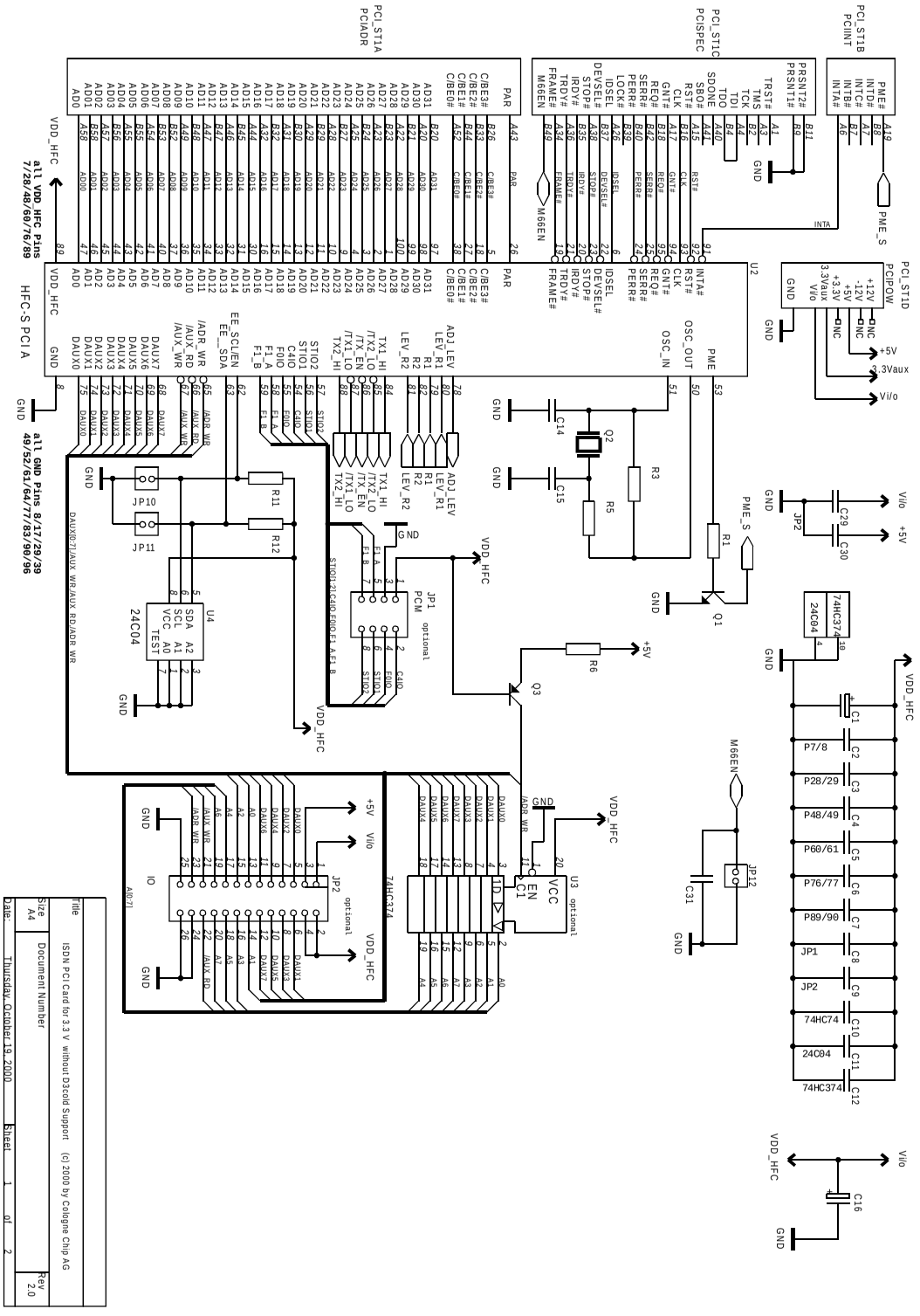
JP1	PCM	*optional*
JP2	IO	*optional*
JP3	Reset options	
JP4	Power options	
JP5	Power options	
JP10	EEPROM options	*optional*
JP11	EEPROM options	*optional*

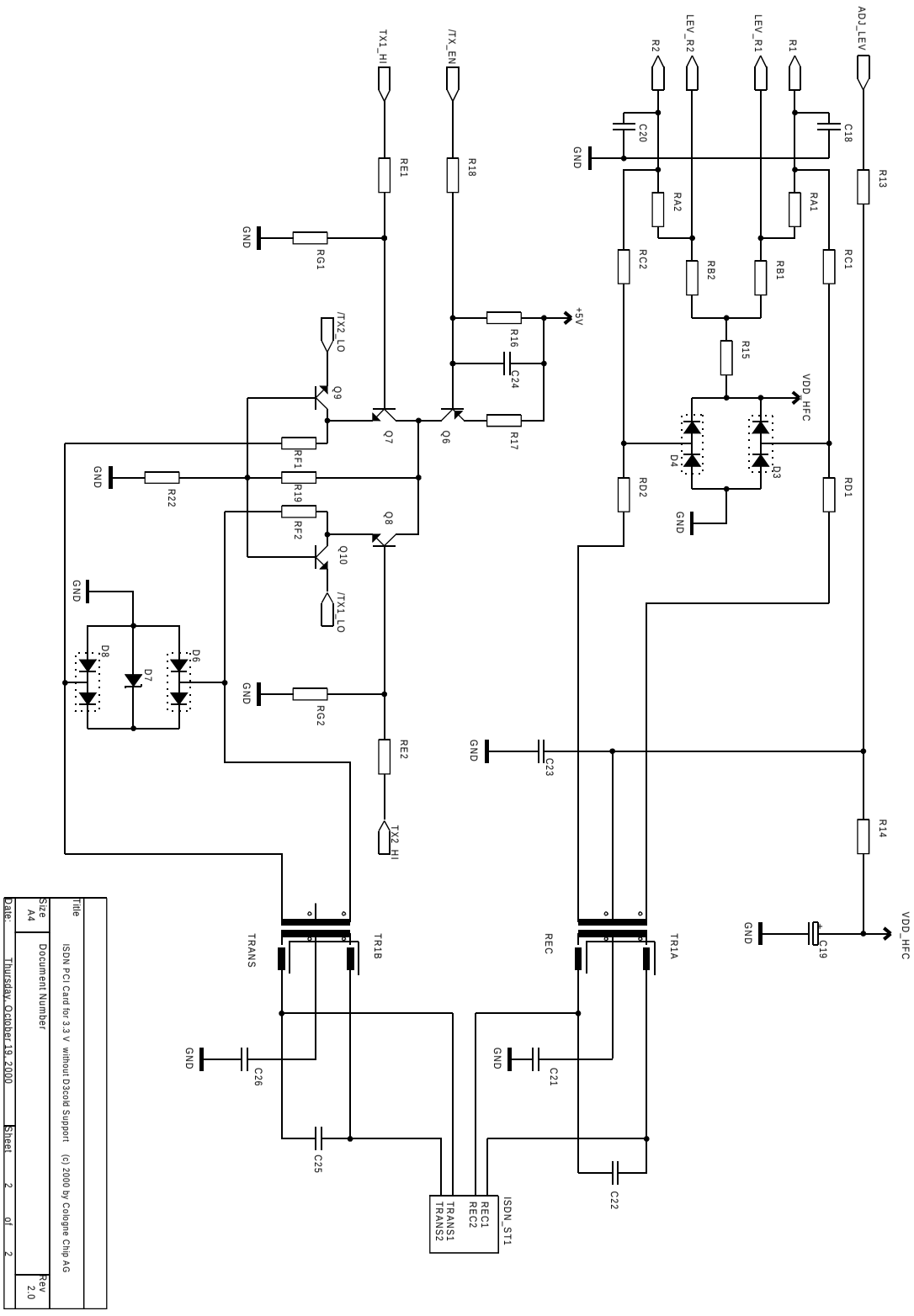
Transistors / Crystals

Q1	BC850C	CMPT5088 or similar
Q2	12.288M	
Q3	BC860C	CMPT5087 or similar
Q4	BC860C	CMPT5087 or similar
Q5	BC860C	CMPT5087 or similar
Q6	BC860C	CMPT5087 or similar
Q7	BC850C	CMPT5088 or similar
Q8	BC850C	CMPT5088 or similar
Q9	BC850C	CMPT5088 or similar
Q10	BC850C	CMPT5088 or similar

12.3 ISDN PCI card for 3.3V power supply (no $D3_{cold}$ support)

Please see chapter 3.3 for details on power management support of HFC-S PCI A and special considerations for support of power management state $D3_{cold}$.

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LEV_R1
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GND
R13
RA2
RA1
RC2
RB2
RB1
RC1
R15
VDD_HFC
D4
D3
RD2
RD1
GND
R14
C19
VDD_HFC
C23
GND
TX1_H
/TX_EN
RE1
R18
RG1
GND
/TX2_LO
Q9
R16
C24
+5V
Q7
Q6
R17
RF1
R19
RF2
R22
GND
Q8
Q10
/TX1_LO
GND
D8
D7
D6
GND
RG2
RE2
TX2_H
TRANS
TR1B
REC
TR1A
GND
C26
C21
C25
C22
TRANS1
TRANS2
REC1
REC2
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ISDN PCI Card for 3.3 V without D3cold Support (c) 2000 by Cologne Chip AG
Size
A4
Document Number
Rev
2.0
Date: Thursday, October 19, 2000
Sheet 2 of 2

ISDN PCI Card for 3.3 V without D3cold support

Capacitors

C01	33µ	
C02	33n	nearby U2
C03	33n	nearby U2
C04	33n	nearby U2
C05	33n	nearby U2
C06	33n	nearby U2
C07	33n	nearby U2
C08	33n	nearby JP1 *optional*
C09	33n	nearby JP2 *optional*
C10	33n	nearby U1
C11	33n	nearby U4
C12	33n	nearby U3 *optional*
C14	47p	depends on crystal
C15	47p	depends on crystal
C16	33µ	
C18	22p	nearby U2
C19	33µ	
C20	22p	nearby U2
C21	0	*optional*
C22	0	*optional*
C23	47n	
C24	470p	
C25	0	*optional*
C26	0	*optional*
C29	33n	nearby JP2 *optional*
C30	33n	nearby JP2 *optional*
C31	10n	optional

Resistors

R01	10k	
R03	1M	
R05	330	
R06	10k	
R11	10k	
R12	10k	
R13	3k9	
R14	680k	
R15	1M2	
R16	3k3	
R17	100	
R18	5k6	
R19	3k3	
R22	2k2	
RA1	100k	
RA2	100k	
RB1	33k	
RB2	33k	
RC1	4k7	
RC2	4k7	
RD1	4k7	
RD2	4k7	
RE1	430	1%
RE2	430	1%
RF1	15	
RF2	15	
RG1	3k9	1%
RG2	3k9	1%

IC's

U2	HFC-S PCI A	*Cologne Chip AG*
U3	74HC374	*optional*
U4	24C04	

Connectors

JP1	PCM	*optional*
JP2	IO	*optional*
JP10	EEPROM options	*optional*
JP11	EEPROM options	*optional*
JP12	33/66 MHz	*optional*

Transistors / Crystals

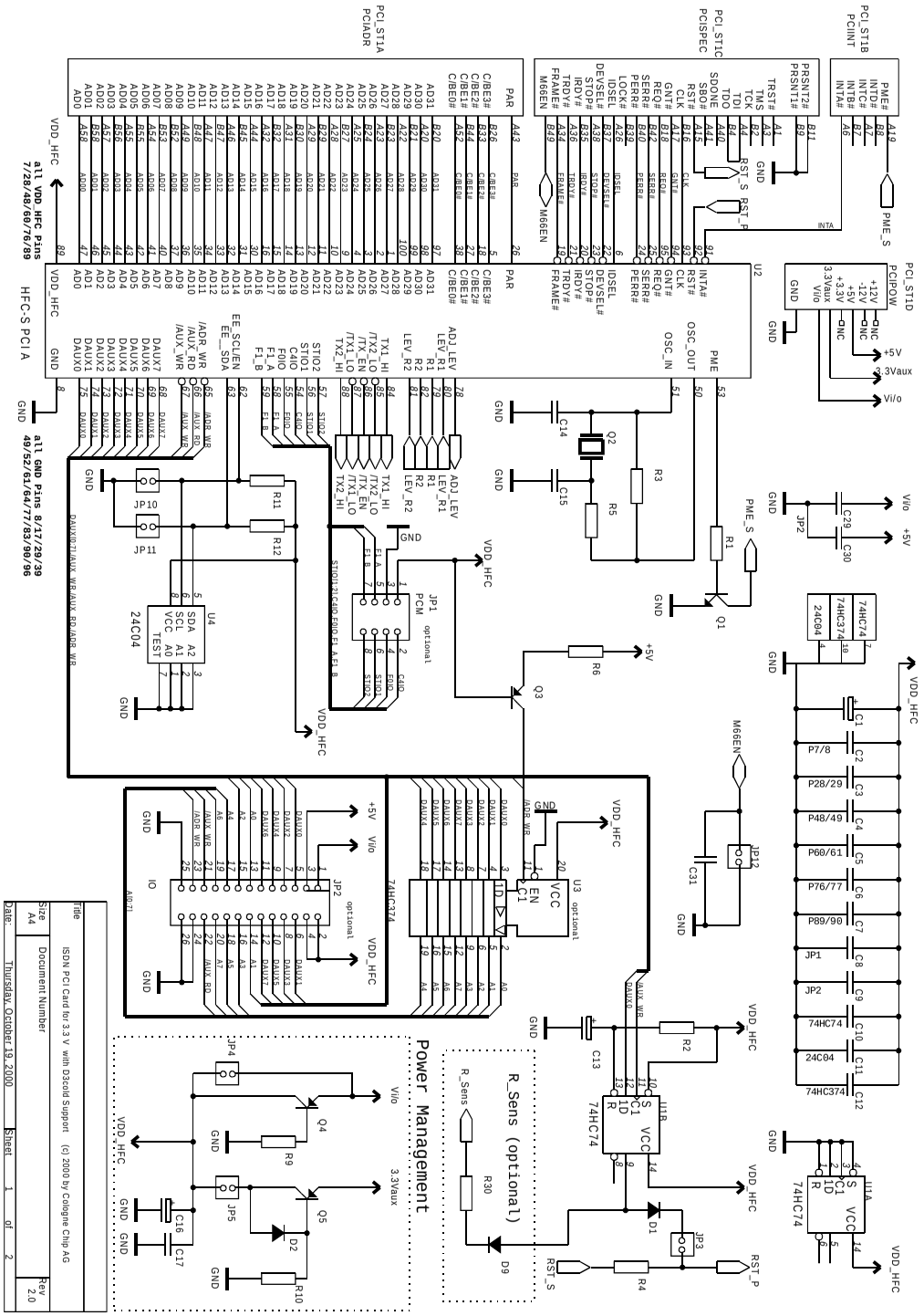
Q1	BC850C	CMPT5088 or similar
Q2	12.288M	
Q3	BC860C	CMPT5087 or similar
Q6	BC860C	CMPT5087 or similar
Q7	BC850C	CMPT5088 or similar
Q8	BC850C	CMPT5088 or similar
Q9	BC850C	CMPT5088 or similar
Q10	BC850C	CMPT5088 or similar

Diodes

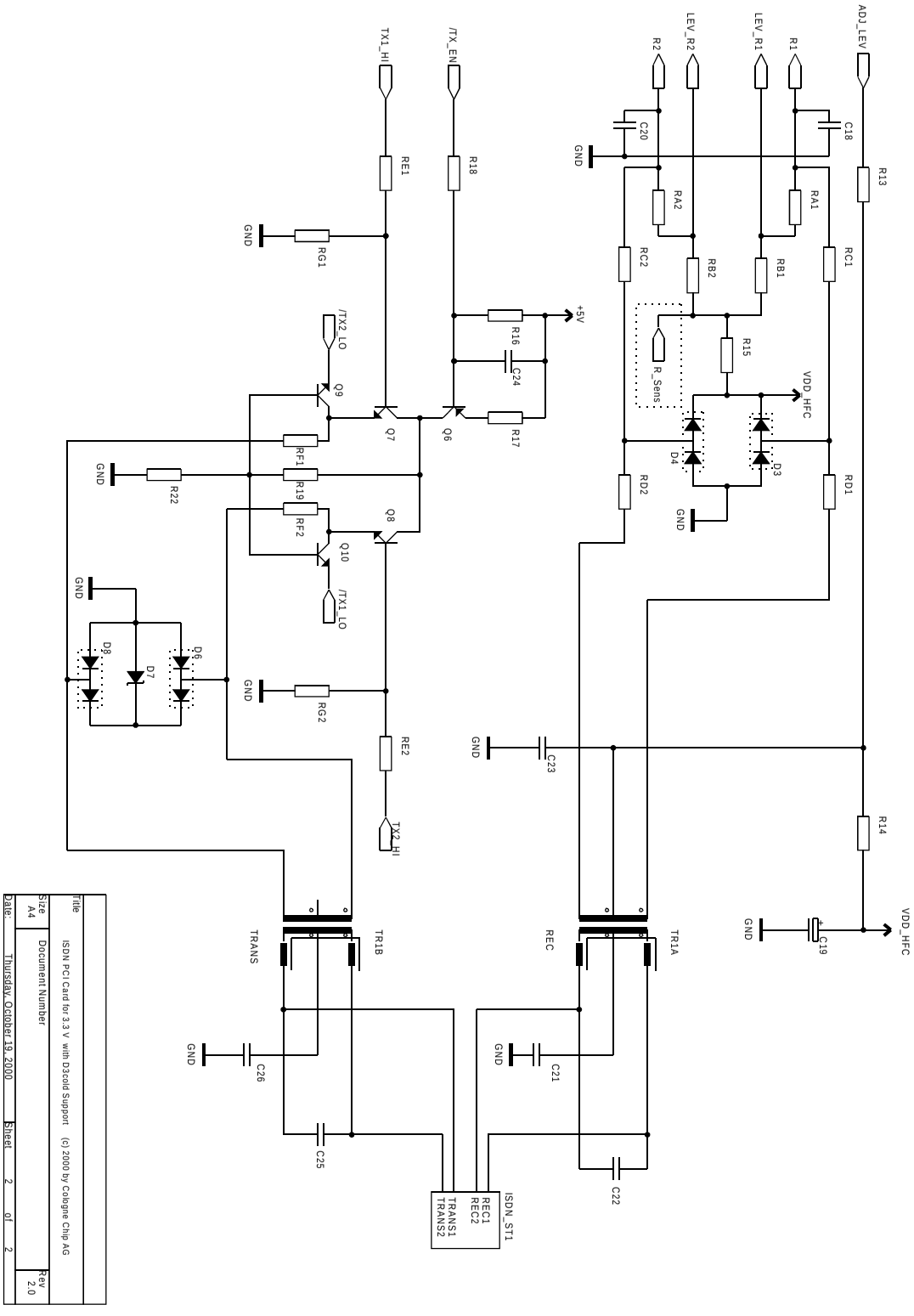
D3	BAV99	can also be 2*4148
D4	BAV99	can also be 2*4148
D6	BAV99	can also be 2*4148
D7	2V7	
D8	BAV99	can also be 2*4148

12.4 ISDN PCI card for 3.3V power supply with $D3_{cold}$ support

Please see chapter 3.3 for details on power management support of HFC-S PCI A and special considerations for support of power management state $D3_{cold}$.



The R_Sens part is optional. It is used to decrease the receiver sensitivity for wake-up signals to avoid a wake-up caused by disturbance on the ISDN line.


ADJ_LEV
LEV_R2
LEV_R1
R2
R1
C20
C18
GND
R13
RA2
RA1
RC2
RB2
RB1
RC1
R15
R_Sens
VDD_HFC
D4
D3
RD2
RD1
GND
R14
C19
VDD_HFC
C23
GND
TX1_HI
/TX_EN
RE1
R18
GND
RG1
+5V
R16
C24
/TX2_LO
Q9
Q7
Q6
R17
RF1
GND
R22
R19
RF2
Q8
Q10
/TX1_LO
GND
D8
D7
D6
GND
RG2
RE2
TX2_HI
TRANS
TR1B
REC
TR1A
GND
C26
GND
C21
C25
C22
ISDN_ST1
TRANS1
TRANS2
REC1
REC2
Title
ISDN PCI Card for 3.3 V with D3cold Support (c) 2000 by Cologne Chip AG
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ISDN PCI Card for 3.3 V with D3cold support

Capacitors

C01	33µ	
C02	33n	nearby U2
C03	33n	nearby U2
C04	33n	nearby U2
C05	33n	nearby U2
C06	33n	nearby U2
C07	33n	nearby U2
C08	33n	nearby JP1 *optional*
C09	33n	nearby JP2 *optional*
C10	33n	nearby U1
C11	33n	nearby U4
C12	33n	nearby U3 *optional*
C13	1µ	
C14	47p	depends on crystal
C15	47p	depends on crystal
C16	33µ	
C17	33n	
C18	22p	nearby U2
C19	33µ	
C20	22p	nearby U2
C21	0	*optional*
C22	0	*optional*
C23	47n	
C24	470p	
C25	0	*optional*
C26	0	*optional*
C29	33n	nearby JP2 *optional*
C30	33n	nearby JP2 *optional*
C31	10n	optional

Resistors

R01	10k	
R02	1M	
R03	1M	
R04	10k	
R05	330	
R06	10k	
R09	10k	
R10	10k	
R11	10k	
R12	10k	
R13	3k9	
R14	680k	
R15	1M2	
R16	3k3	
R17	100	
R18	5k6	
R19	3k3	
R22	2k2	
R30	680k *	
RA1	100k	
RA2	100k	
RB1	33k	
RB2	33k	
RC1	4k7	
RC2	4k7	
RD1	4k7	
RD2	4k7	
RE1	430	1%
RE2	430	1%
RF1	15	
RF2	15	
RG1	3k9	1%
RG2	3k9	1%

IC's

U1	74HC74	
U2	HFC-S PCI A	Cologne Chip AG
U3	74HC374	*optional*
U4	24C04	

Connectors

JP1	PCM	*optional*
JP2	IO	*optional*
JP3	Reset options	
JP4	Power options	
JP5	Power options	
JP10	EEPROM options	*optional*
JP11	EEPROM options	*optional*
JP12	33/66 MHz	*optional*

Transistors / Crystals

Q1	BC850C	CMPT5088 or similar
Q2	12.288M	
Q3	BC860C	CMPT5087 or similar
Q4	BC860C	CMPT5087 or similar
Q5	BC860C	CMPT5087 or similar
Q6	BC860C	CMPT5087 or similar
Q7	BC850C	CMPT5088 or similar
Q8	BC850C	CMPT5088 or similar
Q9	BC850C	CMPT5088 or similar
Q10	BC850C	CMPT5088 or similar

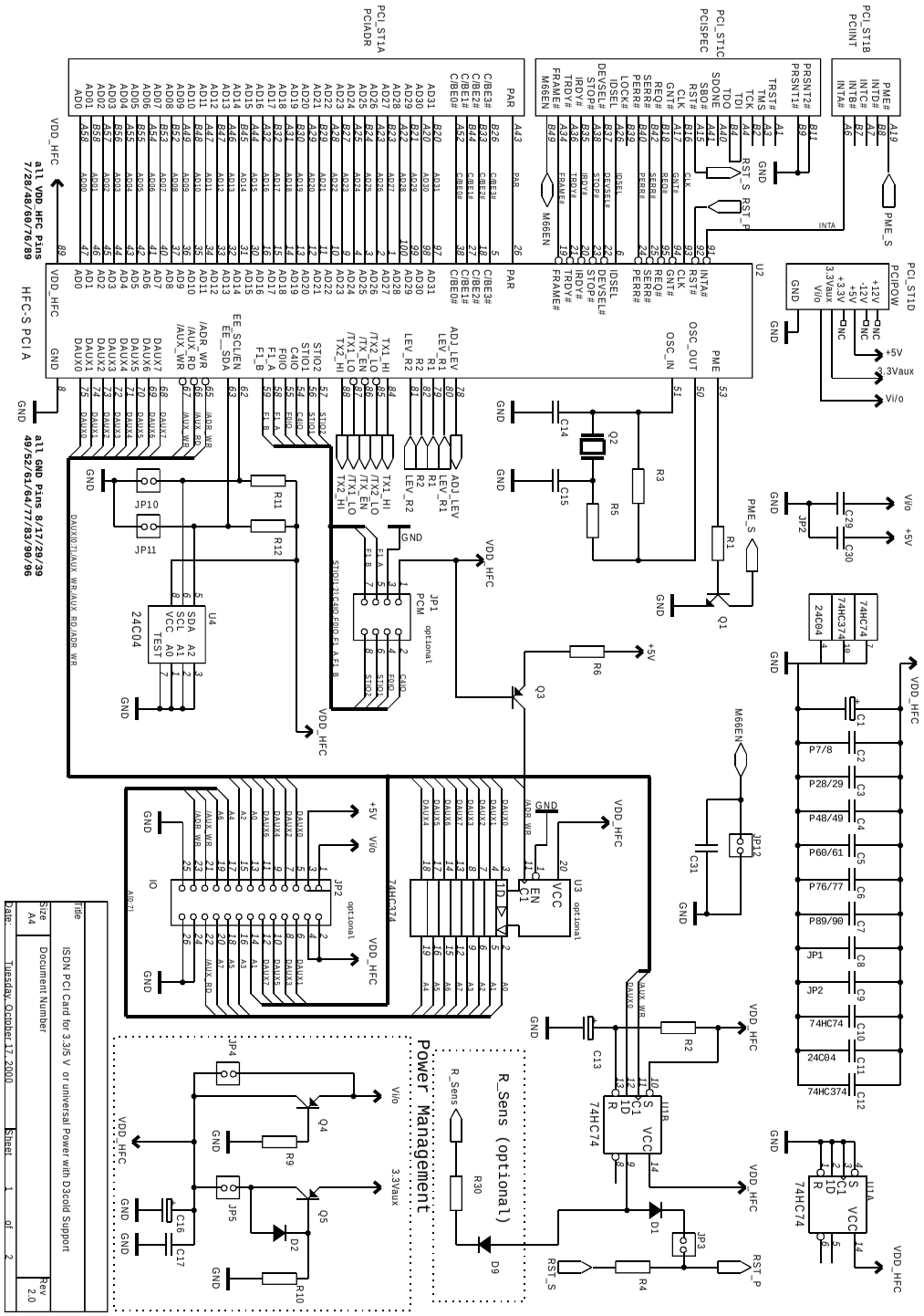
Diodes

D1	LL4148	or similar
D2	LL4148	or similar
D3	BAV99	can also be 2*4148
D4	BAV99	can also be 2*4148
D6	BAV99	can also be 2*4148
D7	2V7	
D8	BAV99	can also be 2*4148
D9	LL4148 *	or similar

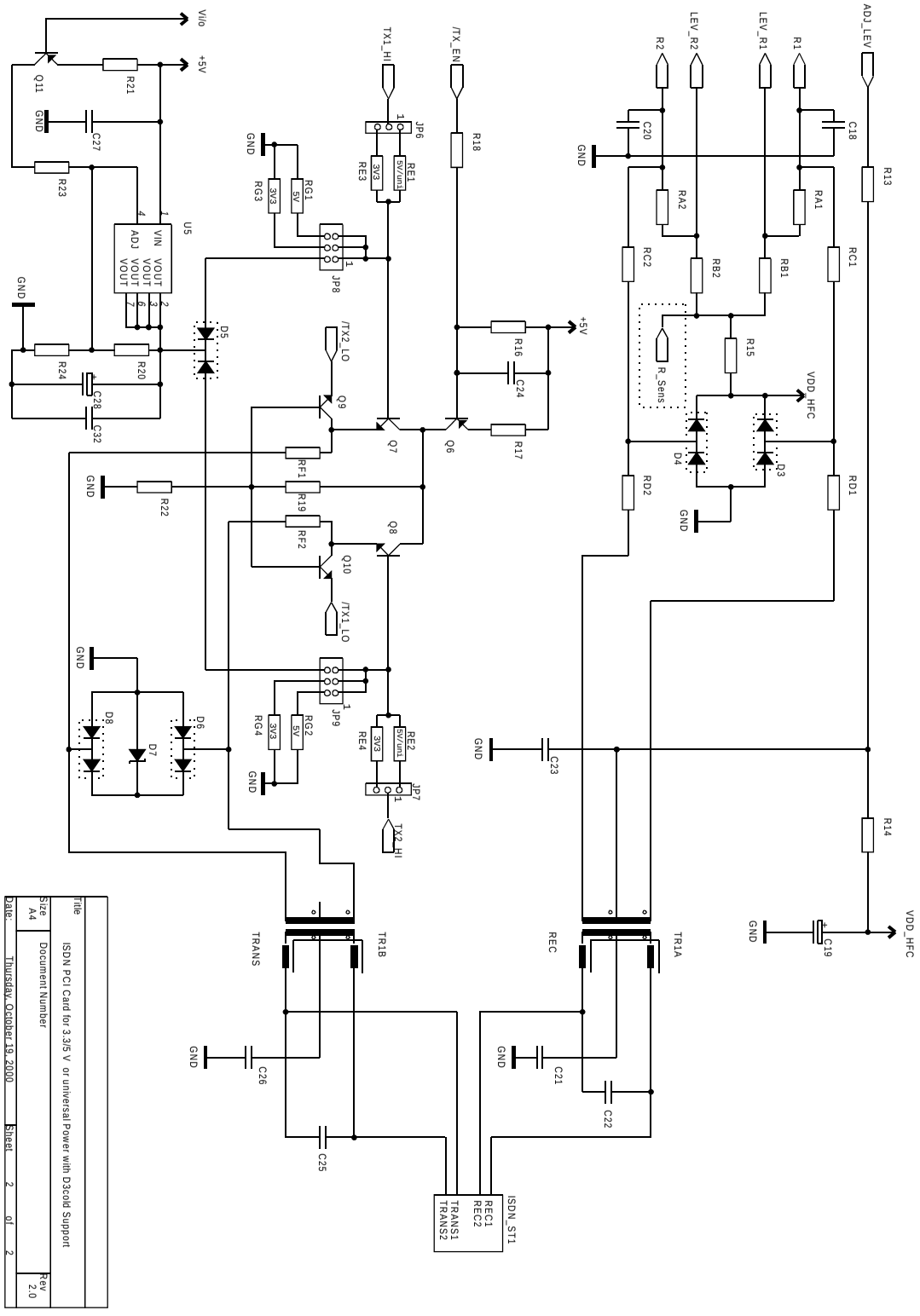
* optional, not on PCB Layout V 2.0

12.5 ISDN PCI card for 3.3 and 5V power supply (auto detect) with $D3_{cold}$ support

Please see chapter 3.3 for details on power management support of HFC-S PCI A and special considerations for support of power management state $D3_{cold}$.



The R_Sens part is optional. It is used to decrease the receiver sensitivity for wake-up signals to avoid a wake-up caused by disturbance on the ISDN line.


Vio
+5V
Q11
R21
GND
C27
R23
U5
VIN
ADJ
VOUT
VOUT
VOUT
VOUT
R24
R20
C28
C32
D5
TX1_HI
/TX_EN
JP6
RE1
RE3
3V3
5V/uns
RG3
RG1
5V
JP8
/TX2_LO
Q9
Q7
Q6
R18
R16
C24
R17
RF1
R19
RF2
Q8
Q10
/TX1_LO
R22
JP9
RG4
RG2
RE4
JP7
TX2_HI
D8
D7
D6
LEV_R2
LEV_R1
ADJ_LEV
R2
R1
C20
C18
R13
RA2
RA1
RC2
RB2
RB1
RC1
R_Sens
R15
VDD_HFC
D4
D3
RD2
RD1
R14
C19
C23
TR1B
TR1A
TRANS
REC
C26
C21
C22
C25
ISDN_ST1
TRANS1
TRANS2
REC1
REC2
Title
ISDN PCI Card for 3.3/5 V or universal Power with D3cold Support
Size
A4
Document Number
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2.0
Date:
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2

ISDN PCI Card for 3.3/5 V or Universal Power with D3cold Support

Capacitors

C01	33µ	
C02	33n	nearby U2
C03	33n	nearby U2
C04	33n	nearby U2
C05	33n	nearby U2
C06	33n	nearby U2
C07	33n	nearby U2
C08	33n	nearby JP1 *optional*
C09	33n	nearby JP2 *optional*
C10	33n	nearby U1
C11	33n	nearby U4
C12	33n	nearby U3 *optional*
C13	1µ	
C14	47p	depends on crystal
C15	47p	depends on crystal
C16	22µ	
C17	33n	
C18	22p	nearby U2
C19	33µ	
C20	22p	nearby U2
C21	0	*optional*
C22	0	*optional*
C23	47n	
C24	470p	
C25	0	*optional*
C26	0	*optional*
C27	33n	
C28	1µ	
C29	33n	nearby JP2 *optional*
C30	33n	nearby JP2 *optional*
C31	10n	*only for 3.3V systems*
C32	0	*optional*

Diodes

D1	LL4148	or similar
D2	LL4148	or similar
D3	BAV99	can also be 2*4148 *
D4	BAV99	can also be 2*4148 *
D5	BAV70	can also be 2*4148 *
D6	BAV99	can also be 2*4148 *
D7	2V7	
D8	BAV99	can also be 2*4148 *
D9	LL4148 **	or similar

Resistors

R01	10k	
R02	1M	
R03	1M	
R04	10k	
R05	330	
R06	10k	
R09	10k	
R10	10k	
R11	10k	
R12	10k	
R13	3k9	
R14	680k	
R15	1M2	
R16	3k3	
R17	100	
R18	5k6	
R19	3k3	
R20	180	
R21	1k	
R22	2k2	
R23	2k7	
R24	150	
R30	680k **	
RA1	100k	
RA2	100k	
RB1	33k	
RB2	33k	
RC1	4k7	
RC2	4k7	
RD1	4k7	
RD2	4k7	
RE1	2k2	1%
RE2	2k2	1%
RE3	430	1%
RE4	430	1%
RF1	15	
RF2	15	
RG1	3k	1%
RG2	3k	1%
RG3	3k9	1%
RG4	3k9	1%

IC's

U1	74HC74	
U2	HFC-S PCI A	Cologne Chip AG
U3	74HC374	*optional*
U4	24C04	
U5	LM317L/SO	

Connectors

JP1	PCM	*optional*
JP2	IO	*optional*
JP3	Reset options	
JP4	Power options	
JP5	Power options	
JP6	Power options	
JP7	Power options	
JP8	Power options	
JP9	Power options	
JP10	EEPROM options	
JP11	EEPROM options	
JP12	66 MHz options	only for 3.3V systems

Transistors / Crystals

Q1	BC850C	CMPT5088 or similar
Q2	12.288M	
Q3	BC860C	CMPT5087 or similar
Q4	BC860C	CMPT5087 or similar
Q5	BC860C	CMPT5087 or similar
Q6	BC860C	CMPT5087 or similar
Q7	BC850C	CMPT5088 or similar
Q8	BC850C	CMPT5088 or similar
Q9	BC850C	CMPT5088 or similar
Q10	BC850C	CMPT5088 or similar
Q11	BC860C	CMPT5087 or similar

* alternative footprint required
** optional, not on PCB Layout V 2.0