AL1201G
24-Bit Digital-to-Analog Converter
Lead Free – Complies with RoHS Directive

ClockEZ™ DAC Converter AL1201G

General Description

The AL1201G is a 24-bit sigma-delta stereo digital-to-analog audio converter using Wavefront's ClockEZ™ technology. With dynamic range of 107dB, simplified interface, and low power consumption, the AL1201G (and its companion AL1101G ADC) is a best-in-class solution for 44.1kHz and 48kHz operation.

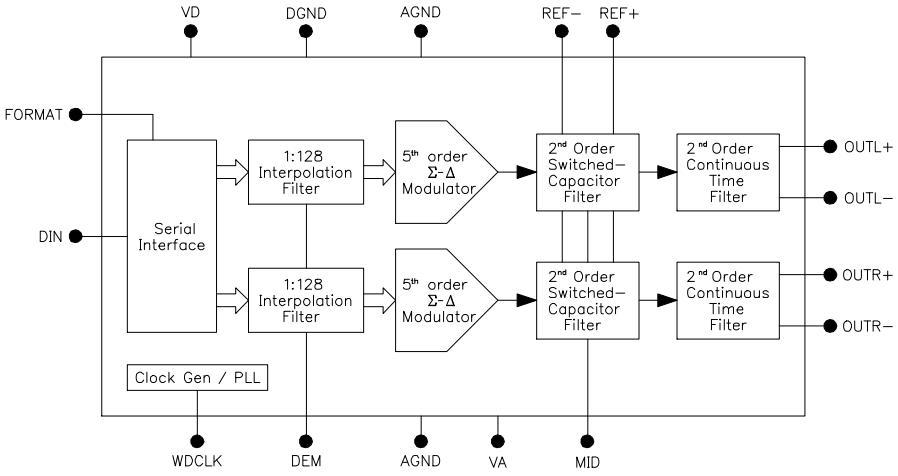
Applications

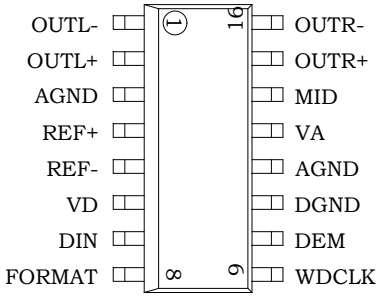
- Digital Mixing Boards
- Signal Processors
- Digital Effects Boxes
- Digital Recorders
- Computer Sound Boards
- Karaoke Systems
- Car Audio Systems
- CD Audio Systems

Features

- 24-bit conversion
- 107dB dynamic range (A-wt)
- 0.003% THD at fullscale input
- ClockEZ™ circuitry: internal PLL derives all necessary timing signals from one external Fs clock
- 128X oversampling, 5th order 1-bit Σ-Δ modulator
- 2nd order switched capacitor filter and 2nd order continuous-time filter on-chip
- Sample rate: 24kHz to 55kHz
- Selectable deemphasis (15µs/50µs at Fs=44.1kHz)
- Serial input selectable: 32/24 bits/frame
- Full scale differential input = ±4V
- 5V operation
- **Lead Free – Complies with RoHS Directive**

Architecture Block diagram and Package





16 pin SOIC
150 mils wide

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Table of Contents

Pin Descriptions

Pin#	Name	Pin Type	Description
1	OUTL-	Out	Negative analog output, left channel.
2	OUTL+	Out	Positive analog output, left channel.
3	AGND	Ground	Analog ground.
4	REF+	Power	Positive reference, connect to V_{DD} thru 220Ω resistor, connect 0.1µF bypass capacitor to REF-.
5	REF-	Ground	Negative reference, connect to GND
6	VD	Power	Digital supply, connect 0.1µF bypass capacitor to GND.
7	DIN	In	Serial data input.
8	FORMAT	In	Format select: 0=32 bits/frame, 1=24bits/frame.
9	WDCLK	In	Sample frequency wordclock, 24kHz<Fs<55kHz.
10	DEM	In	Deemphasis select: 0: no deemphasis, 1=deemphasis.
11	DGND	Ground	Digital ground.
12	AGND	Ground	Analog ground.
13	VA	Power	Analog supply, connect 0.1µF bypass capacitor to GND.
14	MID	I/O	Mid reference, connect 0.1µF bypass capacitor to GND.
15	OUTR+	Out	Positive analog output, right channel.
16	OUTR-	Out	Negative analog output, right channel.

Electrical Characteristics

Parameter	Description/Condition	Min	Typ	Max	Units
Recommended Operating Conditions					
VA	Analog supply voltage	4.5	5.0	5.5	V
VD	Digital supply voltage	4.5	5.0	5.5	V
AGND	Analog ground	-	0.0	-	V
DGND	Digital ground	-	0.0	-	V
Fs	Sample rate	24	48	50	kHz
Temp	Temperature	0	25	70	°C
R_{LOAD}	Differential load resistance	12k			Ω
Analog Characteristics [1]					
Dynamic Range	Output = -60dBFS (A-weighted)		107		dB
THD+N	Output = 0dBFS -20dBFS -60dBFS		-90 -84 -44		dB
Crosstalk	Output = 0dBFS		-118		dB
Output Voltage	[OUT+]-[OUT-] fullscale [2] Interchannel match Differential DC offset Common mode DC bias		±4.0 0.05 1 2.5		V dB mV V
Max Output Current			±0.4		mA
Output Impedance	Differential		3		Ω
REF Current	I_{REF} [3]		190		µA
Power Consumption			170		mW
Gain Error				±0.69	%
PSRR	Power supply rejection ratio		70		dB
Combined Digital/Anaglog Filter Characteristics [4]					
Passband	±0.1dB bandwidth [5] Ripple	0		21.77k ±0.007	Hz dB
Stopband	Frequency [5] Attenuation	26.23k -70			Hz dB
Group Delay			28.5		1/Fs
Deemphasis Filter	'Pole' time constant (Fs = 44.1kHz) 'Zero' time constant (Fs = 44.1kHz)		50 15		µs µs
Digital Inputs (WDCLK, DIN, DEM, FORMAT)					
V_{IH}	Logical "1" input voltage	0.55VD			V
V_{IL}	Logical "0" input voltage			0.1VD	V
I_{IN}	Input leakage current			1	µA
C_{IN}	Input capacitance		5		pF

Note 1: Temp = 25°C, VA = VD = REF+ = 5V, Fs = 48kHz, F_{INPUT} = 24-bit @ 1kHz, Bandwidth = 20Hz-20kHz.

Note 2: Full scale output scales linearly with REF potential ([REF+]-[REF-]).

Note 3: REF current scales linearly with Fs.

Note 4: Temp = 25°C, VA = VD = REF+ = 5V, Fs = 48kHz.

Note 5: Passband, stopband, and deemphasis frequencies scale with Fs.

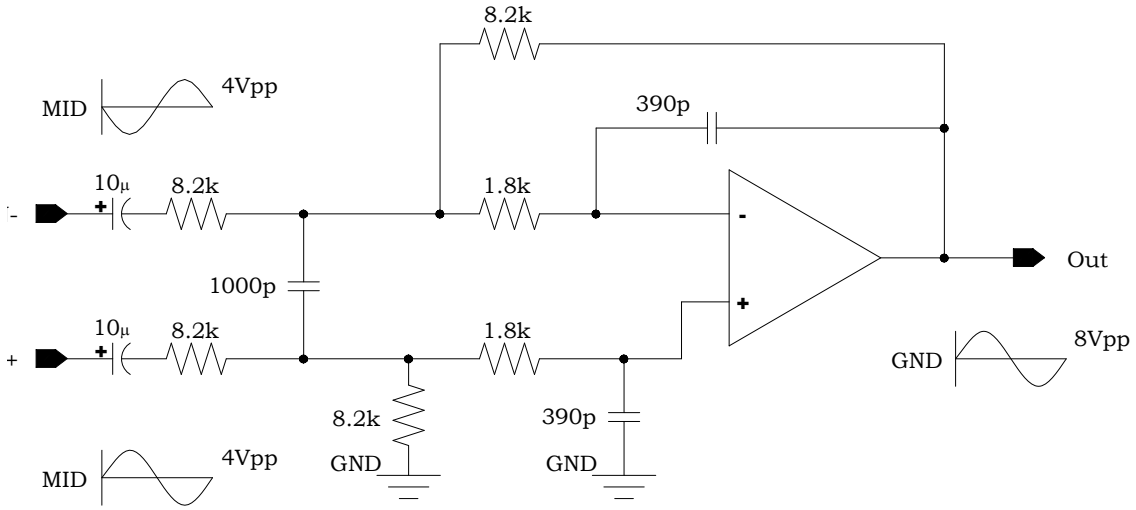
Architecture Details

Differential Analog Outputs

The AL1201G outputs are self-biased to MID potential. Maximum output signal level is ±4V differential, or +0.5V to +4.5V at the pin.

The outputs have been internally filtered to reduce out-of-band noise, and further filtering is suggested where this is considered critical. The differential-to-single-ended filter shown is a two-pole 48kHz lowpass filter whose frequency response is flat from DC to 20kHz ±0.03dB. Its group delay deviation from flat is 1.3µs at 20kHz.

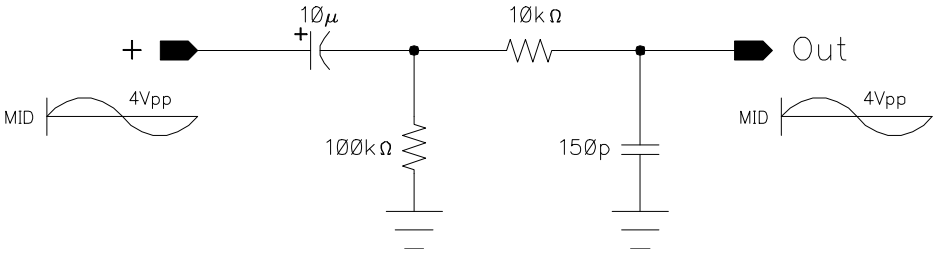
Single-Ended Output Conditioning Circuit



*Note: Film or high quality ceramic capacitor suggested.

If decreasing component count is an important factor, and a decrease in performance specifications is acceptable, the AL1201G outputs may be taken unbalanced with a simple passive component conditioning circuit. The highpass filter has fc = 0.16Hz, the lowpass filter has
fc = 106kHz.

Unbalanced Output Conditioning Circuit



*Note: Film or high quality ceramic capacitor suggested.

The AL1201G can properly receive input logical "1" voltages of 0.55VD. This means the AL1201G can interface directly with logic signals supplied from 3.3V systems. No special interface circuitry is required.

Serial Input Interface

The AL1201G receives its two's complement serial input data in a standard MSB-first format. Two bitrates are provided: The 32-bits-per-frame rate (FORMAT low) is suitable for use in systems where 256*Fs master clocks are present. The 24-bits-per-frame rate (FORMAT high) is convenient when interfacing with circuits where 384*Fs master clocks are present.

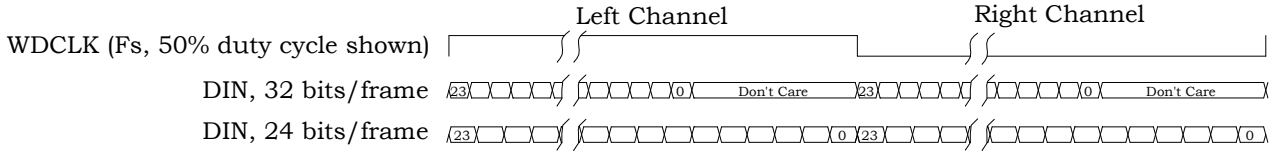
The input sample period is defined between rising edges of wordclock (WDCLK) input. Nominally, this is a 50% duty-cycle clock at frequency Fs, but it can be a pulse with

$$Ts/256 < \text{Pulse Width} < (255/256)*Ts; \quad Ts=1/Fs.$$

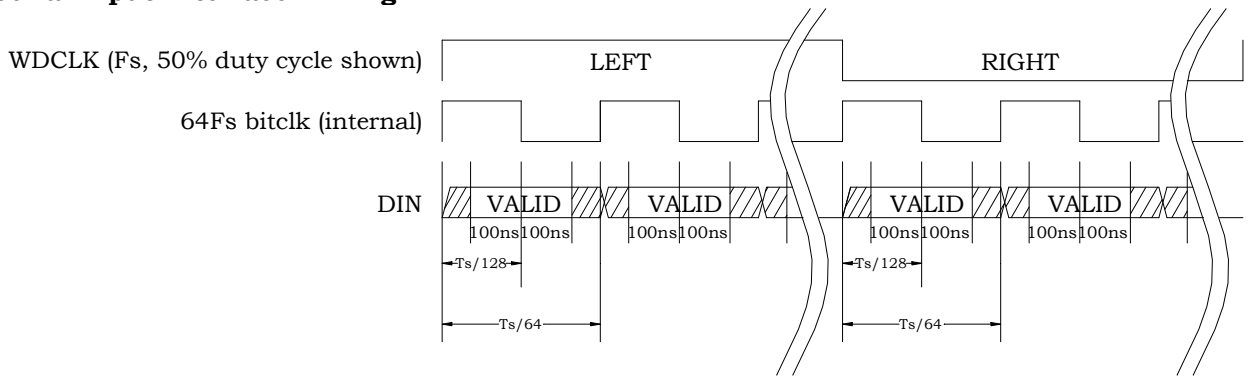
Left channel data input should start when WDCLK rises, and right channel data input should start Ts/2 seconds later (on falling edge of WDCLK if WDCLK has a 50% duty cycle).

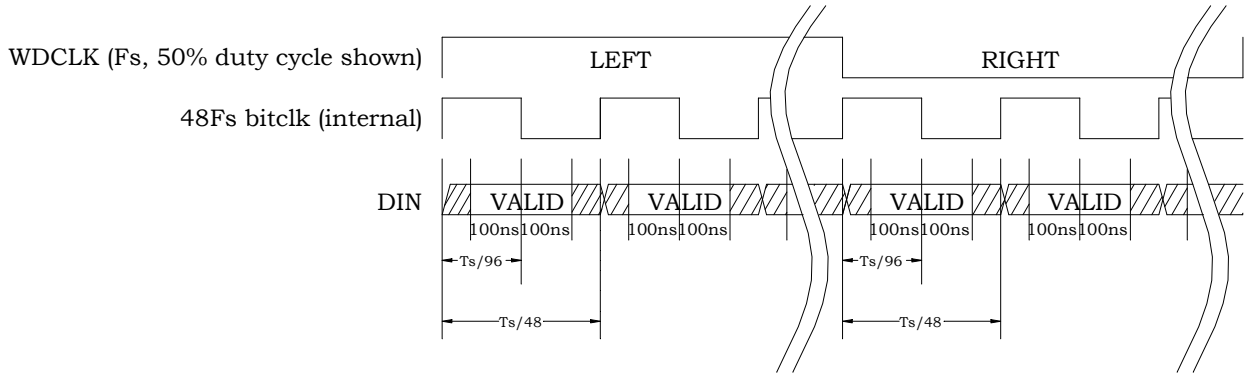
The serial bits are clocked in on the rising edge of an internally generated bitclock (whose rising edge is aligned with rising edge of WDCLK) that runs at 64*Fs when FORMAT is low (32-bits-per-frame), or 48*Fs when FORMAT is high (24-bits-per-frame). The data should be valid ±100ns from the center of these bit-frames.

Serial Input Interface Formats



Serial Input Interface Timing





Clock Generator and PLL

The AL1201G contains an internal PLL that locks to the rising edge of WDCLK and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock (jitter rejection corner at approximately 4kHz).

The PLL allows a simplified user interface and eliminates the need of running high frequency clocks to the part on PCB traces. This reduces unwanted RF noise and coupling problems that can occur when such clock signals are required on input pins for a device.

Reference and MID

The differential potential between the REF+ and REF- pins (connected to +5V and GND respectively) determines the amount of charge that is added to or removed from the switched capacitor filter input for each Σ-Δ modulator output (128*Fs). It is very important that REF+ is well bypassed to REF- (0.1µF ceramic capacitor as close as possible to the pins) to remove the unwanted effects of high frequency noise.

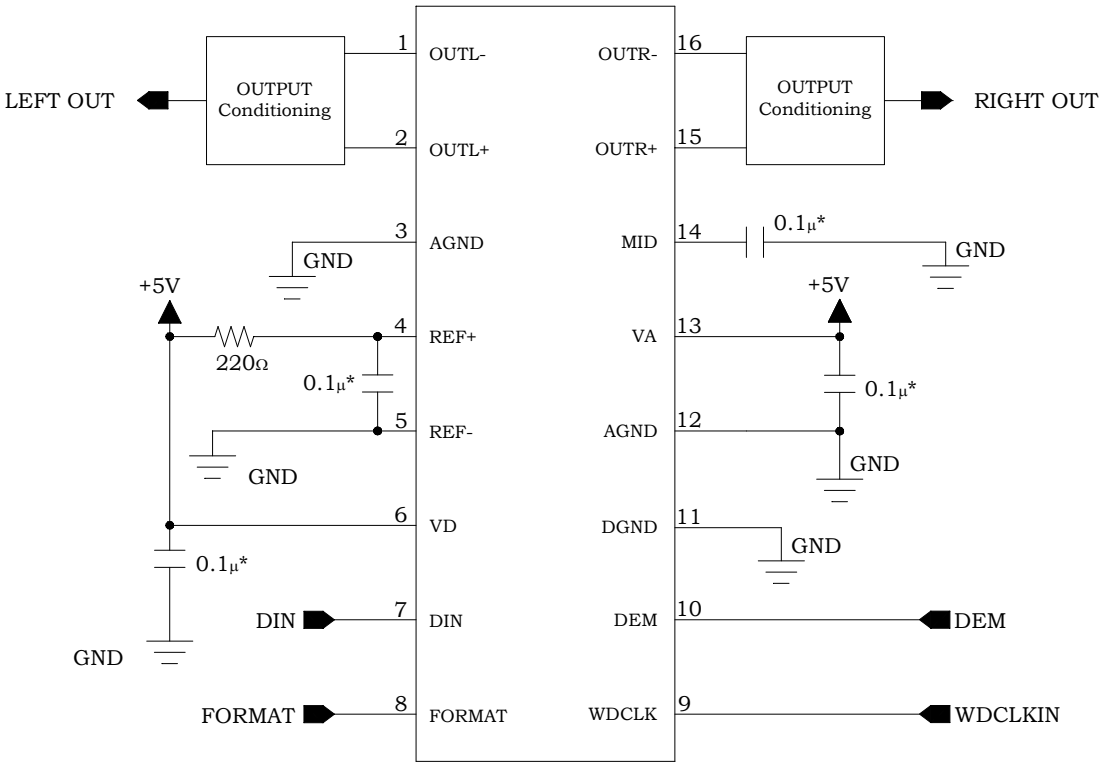
The MID potential is developed on-chip (VA/2 Volts) and is used to bias the internal amplifiers in the switched capacitor and continuous time filters. It requires a 0.1µF bypass capacitor to GND at the pin. No load current should be taken from the MID pin.

Power Supplies and Ground

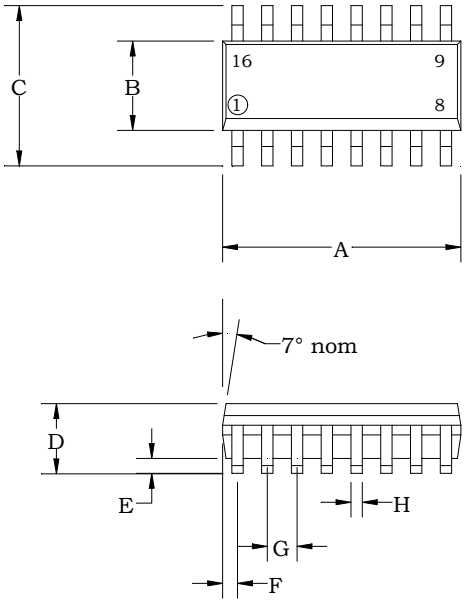
A single low-impedance +5V supply is all that is required to achieve the specified performance. A +5V supply plane on the PCB is recommended if possible. VA and VD may be directly connected to +5V, and REF+ should be isolated with a 220Ω resistor to +5V.

A single low impedance ground plane can be used for all GND connections, simplifying PCB layout. Each supply pin should be bypassed to GND with a 0.1µF ceramic capacitor positioned as close to the pins as possible.

Suggested Connections



Package Dimensions



	Dimensions (Typical)	
	Inches	Millimeters
A	0.389”	9.88
B	0.154”	3.91
C	0.236”	5.99
D	0.100”	2.50
E	0.008”	0.20
F	0.025”	0.64
G	0.050”	1.27
H	0.017”	0.42
J	0.011”	0.27
K	0.170”	4.32
L	0.033”	0.83

Note: Dimension “A” does not include mold flash, protrusions, or gate burrs.

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