AL1402G
ADAT® Optical Decoder
Lead Free – Complies with RoHS Directive

OptoRec ™ ADAT Optical Decoder AL1402G

General Description

The AL1402G OptoRec interface decodes a single datastream of the industry-standard ADAT Optical protocol (U.S. patent number 5,297,181) and produces four stereo pairs (8 channels) of digital audio suitable for DACs or further processing.

With an internal PLL to generate all needed clock signals, the AL1402G requires no external clocks in master mode, and only wordclock (Fs) for proper operation in slave mode.

A companion encoder, the AL1401A OptoGen™, is also available.

Use of the ADAT Optical interface (including the OptoGen and OptoRec) requires a license agreement (generally royalty-free) between the manufacturer and Wavefront Semiconductor. Details and agreement information are available upon request from Wavefront directly, or on our web site.

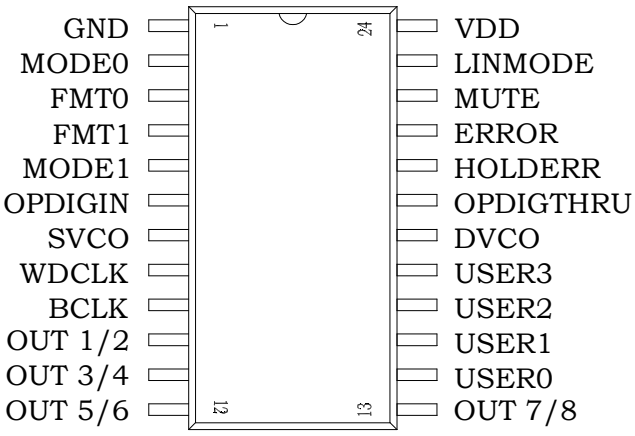
Features

- Compatible with ADAT Type I and II formats
- 4 stereo pairs as inputs using standard ADC formats
- 4 user bit outputs to receive time-code, MIDI data, etc.
- Internal PLL generates all required clocks from optical data or wordclock
- Wordclock input to synchronize outputs to user's system
- **Lead Free – Complies with RoHS Directive**

Applications

- Digital Mixing Boards
- Signal Processors
- Digital Effects Boxes
- Digital Recorders
- Computer Sound Boards
- Sound Reinforcement Products

Package



24 pin SOIC
300 mils wide

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Table of Contents

Pin Descriptions

Pin#	Name	Pin Type	Description
1	GND	Ground	Ground connection.
2	MODE0	In	Mode 0, sets mode.
3	FMT0	In	Format 0, sets data format.
4	FMT1	In	Format 1, sets data format.
5	MODE1	In	Mode 1, sets mode.
6	OPDIGIN	In	Input to optical receiver.
7	SVCO	Out	Master mode: DVCO-derived clock (nominal 12.288MHz, 256*Fs), Slave mode: WDCLK-derived clock.
8	WDCLK	I/O	Wordclock input/output (nominal 48kHz, Fs).
9	BCLK	Out	Bitclock output (nominal 3.072MHz, 64*Fs).
10	OUT 1/2	Out	Channels 1&2 data output.
11	OUT 3/4	Out	Channels 3&4 data output.
12	OUT 5/6	Out	Channels 5&6 data output.
13	OUT 7/8	Out	Channels 7&8 data output.
14	USER0	Out	User 0 data bit output. Used to receive timecode.
15	USER1	Out	User 1 data bit output. Used to receive MIDI data.
16	USER2	Out	User 2 data bit output. Used to receive S/Mux indicator.
17	USER3	Out	User 3 data bit output. Reserved.
18	DVCO	Out	Recovered clock from datastream (nominal 12.288MHz, 256*Fs).
19	OPDIGTHRU	Out	Regenerated OPDIGIN for daisy-chaining.
20	HOLDERR	In	If high, ERROR pin stays high until cause of error removed AND HOLDERR goes low.
21	ERROR	Out	Indicates lack of input or failure to synchronize to datastream. If high, data outputs muted but not clock outputs.
22	MUTE	In	Mute select: 1=Mute outputs, 0=No muting.
23	LINMODE	In	Tie high.
24	V_{DD}	Power	V_{DD} power pin.

Electrical Characteristics

Symbol	Description	Min	Typ	Max	Units
Recommended Operating Conditions					
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
$I_{DD-MSTR}$	Supply Current, Master		7.7		mA
$I_{DD-SLAV}$	Supply Current, Slave		5.4		mA
GND	Ground		0		V
Fs	Sample rate	30	48	55	kHz
Temp	Temperature	0	25	70	°C
Inputs (WDCLK, FMT0-1, OPDIGIN, MODE0-1 LINMODE, MUTE, HOLDERR)					
V_{IH}	Logical "1" input voltage	0.75 V_{DD}			V
V_{IL}	Logical "0" input voltage			0.25 V_{DD}	V
I_{IH}	Logical "1" input current			1	µA
I_{IL}	Logical "0" input current			1	µA
C_{IN}	Logic input capacitance		5		pF
Outputs (WDCLK, DVCO, OPDIGTHRU, SVCO, BCLK, ERROR)					
V_{OH}	Logical "1" output voltage	0.9 V_{DD}			V
V_{OL}	Logical "0" output voltage			0.1 V_{DD}	V
I_{OH}	Logical "1" output current			-8	mA
I_{OL}	Logical "0" output current			8	mA
Outputs (OUT1/2-7/8, USER0-3)					
V_{OH}	Logical "1" output voltage	0.9 V_{DD}			V
V_{OL}	Logical "0" output voltage			0.1 V_{DD}	V
I_{OH}	Logical "1" output current			-2	mA
I_{OL}	Logical "0" output current			2	mA

Architecture Details

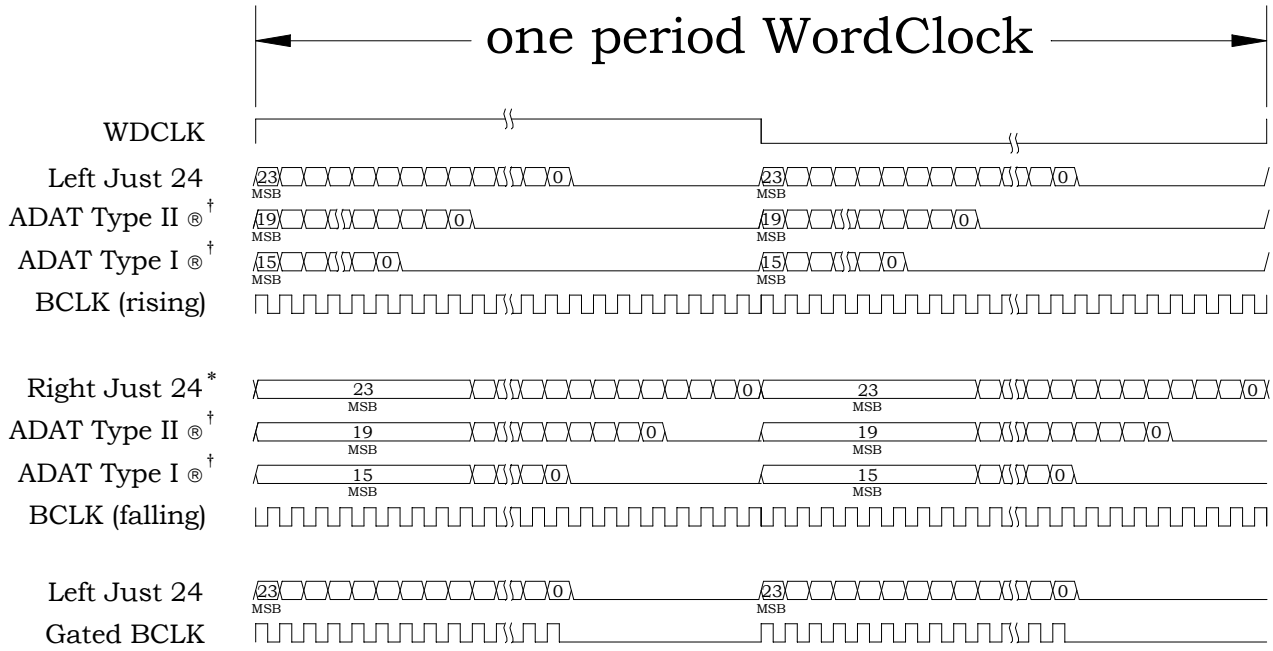
Serial Output Interface

The AL1402G OptoRec interface has been designed for ease of use and flexibility in systems designed to interface to the ADAT protocol. It supports both left and right justified data formats for ease of integration into existing devices as well as new devices. These formats allow it to operate in parallel with many standard ADCs. The specific output format to be used is selected by the format pins FMT1 and FMT0.

Serial Output Format Selection

FMT[1:0]	Format
00	Right justified, BCLK falls on WDCLK edge.
01	Left justified, BCLK rises on WDCLK edge.
10	Chip reset.
11	Gated BCLK, BCLK rises on WCLK edge.

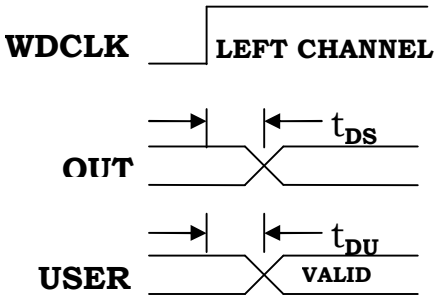
Serial Output Formats



*Note: The most significant bit is sign-extended to the left of the frame.

+Note: These diagrams represent how data would be framed from an ADAT Type I or Type II device. They are not actual modes of the OptoRec. The left justified mode is recommended for ADAT formats.

Serial Output Timing



Symbol	Description	Min	Typ	Max	Units
$t_{DS(Mstr)}$	OUT setup time relative to Master WDCLK output	-10	2	27	ns
$t_{DS(Slav)}$	OUT setup time relative to Slave WDCLK input	-7	5	30	ns
$t_{DU(Mstr)}$	USER setup time relative to Master WDCLK output	-10	0	25	ns
$t_{DU(Slav)}$	USER setup time relative to Slave WDCLK input	-8	2	27	ns

Note: Above specifications hold after 3900 WDCLK cycles of valid input at OPDIGIN.

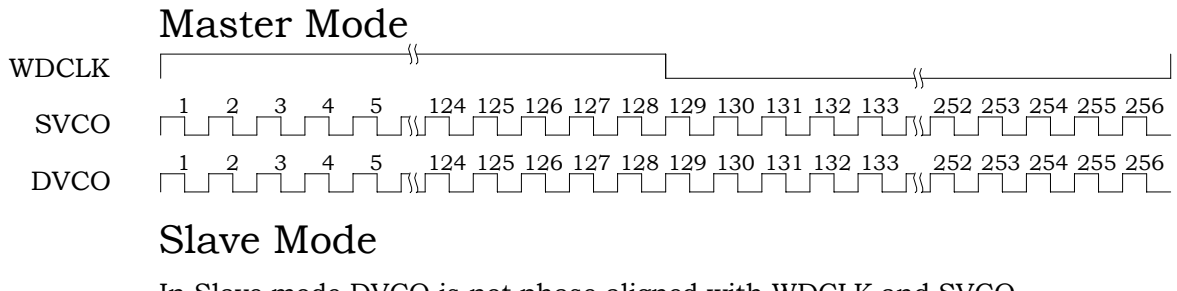
Wordclock Selection

With the use of the MODE inputs, the user may choose the source of the wordclock used to generate the output clocks for the OptoRec. When the OptoRec is in Master Mode, all outputs are derived from the input ADAT Optical datastream on the OPDIGIN pin, and WDCLK is an output. When the OptoRec is in Slave Mode, OUT1/2-7/8, USER0-3, BCLK, and SVCO are synchronous to WDCLK, which is an input. While in Slave mode, WDCLK may be at an arbitrary phase with respect to the incoming samples of OPDIGIN, but if the two frequencies are not identical, samples will be dropped, repeated, or garbled. Generally, identical frequencies are achieved by either using DVCO as the source from which WDCLK is generated, or creating OPDIGIN from a source synchronized to WDCLK.

Wordclock Mode Selection

MODE[1:0]	Mode
00	Master Mode, WDCLK is an output.
01	Slave Mode, WDCLK is an input. WDCLK MUST be derived from the same clock supplying the source.
10	Reserved.
11	Reserved.

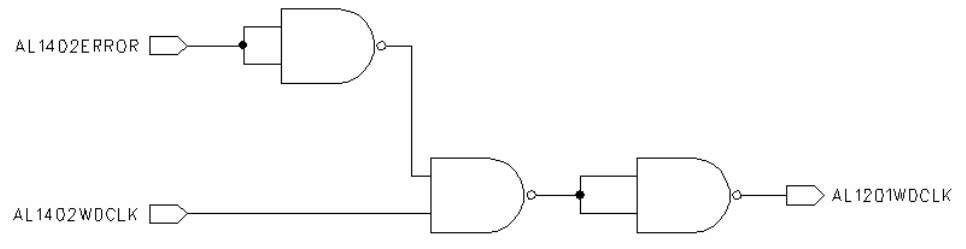
Wordclock Modes



In Slave mode DVCO is not phase aligned with WDCLK and SVCO.

Wordclock Muting

The OptoRec in Master Mode can produce clock outputs running at uncontrolled frequencies if the digital input becomes unstable after stable use, due mostly to poor connection of the optical cable to the optical connector. Care should be taken when running the OptoRec with the AL1201 DAC as the AL1201 DAC will output noise if the OptoRec WDCLK is at an uncontrolled VCO frequency beyond the AL1201's maximum. An external AND gate implementation may be used to correct this. The inverted ERROR pin and the desired OptoRec output clock are inputs to the AND gate and the desired mutable clock is the output, and the AND function will mute the selected OptoRec clock when the ERROR pin is high (i.e. when unstable input is present at OPDIGIN). In place of this circuit, the ERROR pin may be used as a mute select for any audio output stage muting circuitry that is present in the system.



ADAT Optical Datastream

The AL1402G provides support for both the ADAT Type I format (16-bit) and the ADAT Type II format (20-bit). Data lengths of up to 24 bits are supported. USER0 is used to receive the ADAT format 32-bit timecode, USER1 is used to receive MIDI data, USER2 is used to receive the S/Mux data indicator, and USER3 is reserved and should be tied low.

Reset Circuitry

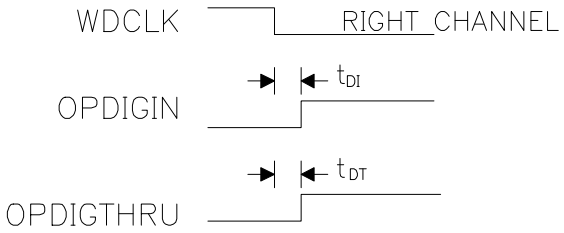
An OptoRec reset, initiated by setting FMT[1:0]=10, is synchronous, and a minimum duration of 1 DVCO clock period is required. At a nominal 12.288MHz, this translates to 82ns. A safety margin is advised, and a pulse width of 100ns would be sufficient to reset the chip. This will reset all internal counters and state registers to their initial state and disrupt the outputs. However, PLL lock to OPDIGIN will not be disturbed.

The clock and data outputs of the OptoRec are undefined after power-up until a proper datastream is well established on OPDIGIN. The clock outputs may be running at an uncontrolled frequency during that time. In this case, the ERROR pin will be high, indicating that the outputs are invalid. This may be prevented by using the FMT pins to reset the OptoRec on power-up, thus stopping the VCO clocks and muting the data output. The FMT pins may then be set to the value required in your system. Nevertheless the OptoRec will synchronize and produce proper outputs when proper and valid inputs are provided, whether this reset procedure is used or not.

Clock Generator and PLL

The OptoRec contains an internal PLL that locks to the embedded clock in the ADAT Optical datastream and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming datastream. Receiving 8 channels of ADAT Optical data on OPDIGIN, the jitter was measured to be 1.5ns typical on WDCLK.

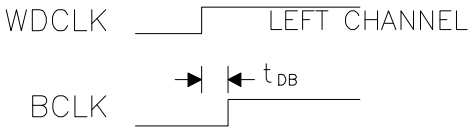
Using the extracted clock, the PLL generates the DVCO output. The datastream is also reconstructed using this PLL and outputted on OPDIGTHRU (clocked on the rising edge of DVCO), and thus the OPDIGTHRU datastream is synchronized to the PLL's wordclock, as well as to OPDIGIN.



Symbol	Description	Min	Typ	Max	Units
t_{DI}	OPDIGIN setup time relative to Master WDCLK output	-34	-53	-72	ns
t_{DT}	OPDIGTHRU setup time relative to Master WDCLK output	-20	-4	5	ns

The OptoRec contains a duplicate PLL that locks to the incoming clock signal on WDCLK when in slave mode. Receiving 8 channels of ADAT Optical data on OPDIGIN, the jitter was measured to be 1.26ns typical on BCLK.

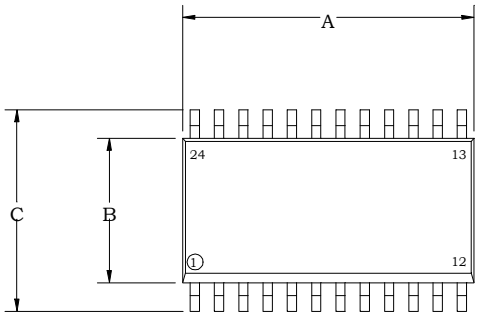
The second PLL locks onto the wordclock selected by the user via the Master/Slave Mode selection. In Master Mode, the selected wordclock comes from the first PLL, and SVCO, BCLK, and WDCLK are all synchronized to it. In Slave Mode, WDCLK is an input, and is what SVCO and BCLK are locked to.



Symbol	Description	Min	Typ	Max	Units
t_{DB}	BCLK setup time relative to Slave WDCLK output	0	9	30	ns

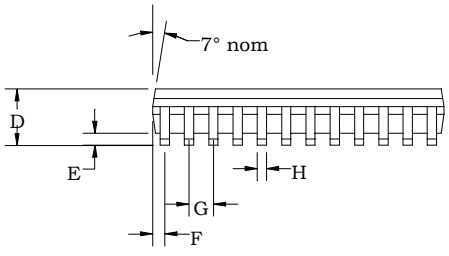
The PLL allows a simplified user interface and eliminates the need of running high frequency clocks to the part on PCB traces. This reduces unwanted RF noise and coupling problems that can occur when such clock signals are required on input pins for a device.

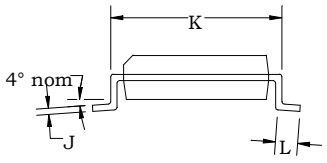
Package Dimensions



Dimensions (Typical)	Inches	Millimeters
A	0.606”	15.40
B	0.295”	7.50
C	0.406”	10.30
D	0.100”	2.50
E	0.008”	0.20
F	0.025”	0.64
G	0.050”	1.27
H	0.017”	0.42
J	0.011”	0.27
K	0.352”	8.94
L	0.033”	0.83

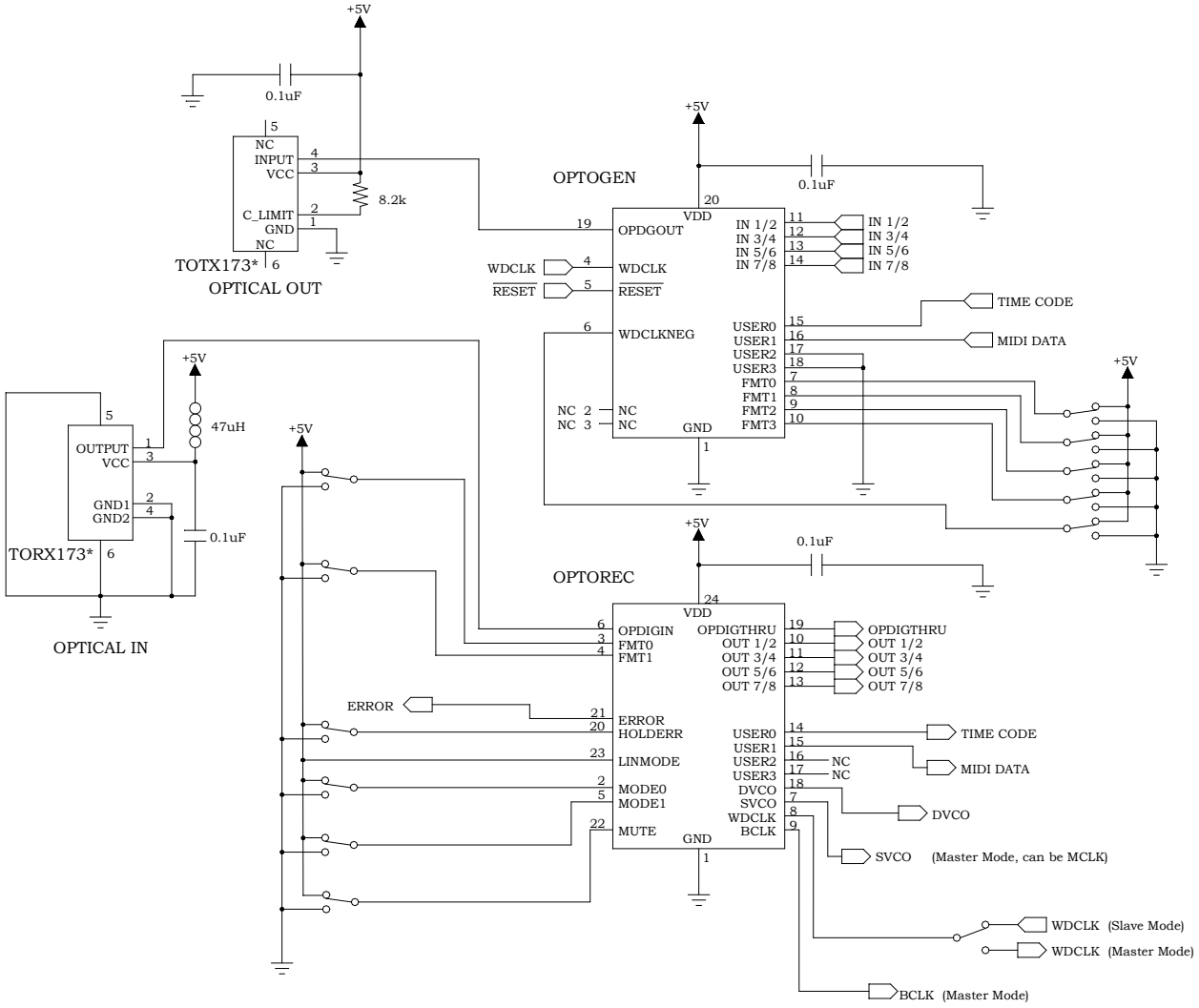
Note: Dimension “A” does not include mold flash, protrusions, or gate burrs.



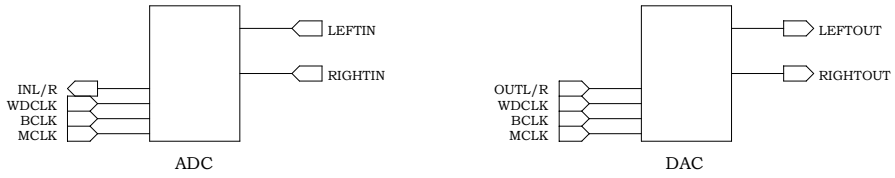


Sample Application Schematic

The following schematic shows the OptoGen and OptoRec in a typical application. The OptoGen accepts input from an ADC, then outputs data in the ADAT Optical format on the optical transmitters. The OptoRec receives ADAT Optical data on the optical receivers, then outputs data to a DAC.



* Optical I/O parts shown are Toshiba parts. The Sharp GP1F33RT or equivalent is also compatible.



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