ELPIDA

DATA SHEET

4GB Unbuffered DDR3 SDRAM DIMM

EBJ41UF8BCF0 (512M words × 64 bits, 2 Ranks)

Specifications

- Density: 4GB
- Organization
  - 512M words × 64 bits, 2 ranks
- Mounting 16 pieces of 2G bits DDR3 SDRAM sealed in FBGA
- Package: 240-pin socket type dual in line memory module (DIMM)
  - PCB height: 30.0mm
  - Lead pitch: 1.0mm
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD = 1.5V ± 0.075V
- Data rate: 1600Mbps/1333Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9, 10, 11
- /CAS write latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    7.8µs at 0°C ≤ TC ≤ +85°C
    3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
- Programmable Output driver impedance control

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Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBJ41UF8BCF0-GN-F	1600	DDR3-1600K (11-11-11)	240-pin DIMM (lead-free and halogen-free)	Gold	EDJ2108BCSE-GN-F
EBJ41UF8BCF0-DJ-F	1333	DDR3-1333H (9-9-9)			EDJ2108BCSE-GN-F EDJ2108BCSE-DJ-F

Detailed Information

For detailed electrical specifications and further information, please refer to the component DDR3 SDRAM datasheet EDJ2104BCSE, EDJ2108BCSE (E1677E).

Pin Configurations

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	121	VSS
2	VSS	122	DQ4
3	DQ0	123	DQ5
4	DQ1	124	VSS
5	VSS	125	DM0
6	/DQS0	126	NC
7	DQS0	127	VSS
8	VSS	128	DQ6
9	DQ2	129	DQ7
10	DQ3	130	VSS
11	VSS	131	DQ12
12	DQ8	132	DQ13
13	DQ9	133	VSS
14	VSS	134	DM1
15	/DQS1	135	NC
16	DQS1	136	VSS
17	VSS	137	DQ14
18	DQ10	138	DQ15
19	DQ11	139	VSS
20	VSS	140	DQ20
21	DQ16	141	DQ21
22	DQ17	142	VSS
23	VSS	143	DM2
24	/DQS2	144	NC
25	DQS2	145	VSS
26	VSS	146	DQ22
27	DQ18	147	DQ23
28	DQ19	148	VSS
29	VSS	149	DQ28
30	DQ24	150	DQ29
31	DQ25	151	VSS
32	VSS	152	DM3
33	/DQS3	153	NC
34	DQS3	154	VSS
35	VSS	155	DQ30
36	DQ26	156	DQ31
37	DQ27	157	VSS
38	VSS	158	NC
39	NC	159	NC
40	NC	160	VSS
41	VSS	161	NC

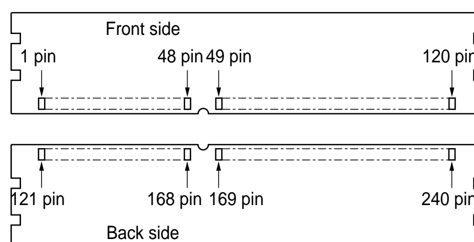
Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
42	NC	162	NC
43	NC	163	VSS
44	VSS	164	NC
45	NC	165	NC
46	NC	166	VSS
47	VSS	167	NC
48	NC	168	/RESET
KEY			
49	NC	169	CKE1
50	CKE0	170	VDD
51	VDD	171	NC
52	BA2	172	A14
53	NC	173	VDD
54	VDD	174	A12
55	A11	175	A9
56	A7	176	VDD
57	VDD	177	A8
58	A5	178	A6
59	A4	179	VDD
60	VDD	180	A3
61	A2	181	A1
62	VDD	182	VDD
63	CK1	183	VDD
64	/CK1	184	CK0
65	VDD	185	/CK0
66	VDD	186	VDD
67	VREFCA	187	NC
68	NC	188	A0
69	VDD	189	VDD
70	A10(AP)	190	BA1
71	BA0	191	VDD
72	VDD	192	/RAS
73	/WE	193	/CS0
74	/CAS	194	VDD
75	VDD	195	ODT0
76	/CS1	196	A13
77	ODT1	197	VDD
78	VDD	198	NC
79	NC	199	VSS
80	VSS	200	DQ36
81	DQ32	201	DQ37

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
82	DQ33	202	VSS
83	VSS	203	DM4
84	/DQS4	204	NC
85	DQS4	205	VSS
86	VSS	206	DQ38
87	DQ34	207	DQ39
88	DQ35	208	VSS
89	VSS	209	DQ44
90	DQ40	210	DQ45
91	DQ41	211	VSS
92	VSS	212	DM5
93	/DQS5	213	NC
94	DQS5	214	VSS
95	VSS	215	DQ46
96	DQ42	216	DQ47
97	DQ43	217	VSS
98	VSS	218	DQ52
99	DQ48	219	DQ53
100	DQ49	220	VSS
101	VSS	221	DM6
102	/DQS6	222	NC
103	DQS6	223	VSS
104	VSS	224	DQ54
105	DQ50	225	DQ55
106	DQ51	226	VSS
107	VSS	227	DQ60
108	DQ56	228	DQ61
109	DQ57	229	VSS
110	VSS	230	DM7
111	/DQS7	231	NC
112	DQS7	232	VSS
113	VSS	233	DQ62
114	DQ58	234	DQ63
115	DQ59	235	VSS
116	VSS	236	VDDSPD
117	SA0	237	SA1
118	SCL	238	SDA
119	SA2	239	VSS
120	VTT	240	VTT

Pin Description

Pin name	Function
A0 to A14	Address input Row address A0 to A14 Column address A0 to A9
A10 (AP)	Auto precharge
A12 (/BC)	Burst chop
BA0, BA1, BA2	Bank select address
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
/CS0, /CS1	Chip select
CKE0, CKE1	Clock enable
CK0, CK1	Clock input
/CK0, /CK1	Differential clock input
ODT0, ODT1	ODT control
DQ0 to DQ63	Data input/output
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1, SA2	Address input for serial PD
VDD*1	Power for internal circuit
VDDSPD	Power for serial PD
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VSS	Ground
VTT	I/O termination supply for SDRAM
/RESET	Set DRAM to a known state
NC	No connection

Note: 1. The VDD and VDDQ pins are tied common to a single power-plane on these designs.

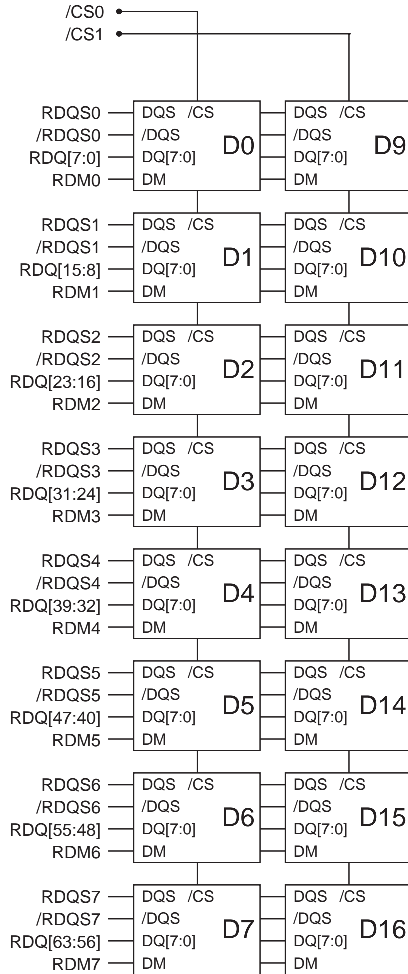


Serial PD Matrix

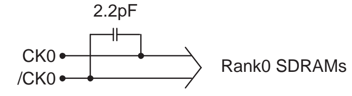
		-DJ		-GN	
Byte No.	Function described	Hex	Comments	Hex	Comments
0	Number of serial PD bytes written/SPD device size/CRC coverage	92h	176/256/0-116	92h	176/256/0-116
1	SPD revision	10h	Rev.1.0	10h	Rev.1.0
2	Key byte/DRAM device type	0Bh	DDR3 SDRAM	0Bh	DDR3 SDRAM
3	Key byte/module type	02h	UDIMM	02h	UDIMM
4	SDRAM density and banks	03h	2G bits, 8 banks	03h	2G bits, 8 banks
5	SDRAM addressing	19h	15 rows, 10 columns	19h	15 rows, 10 columns
6	Module nominal voltage, VDD	00h	1.5V	00h	1.5V
7	Module organization	09h	2 ranks/×8 bits	09h	2 ranks/×8 bits
8	Module memory bus width	03h	64 bits/non-ECC	03h	64 bits/non-ECC
9	Fine timebase (FTB) dividend/divisor	52h	5/2	52h	5/2
10	Medium timebase (MTB) dividend	01h	1	01h	1
11	Medium timebase (MTB) divisor	08h	8	08h	8
12	SDRAM minimum cycle time (tCK (min.))	0Ch	1.5ns	0Ah	1.25ns
13	Reserved	00h	—	00h	—
14	SDRAM CAS latencies supported, LSB	7Ch	6, 7, 8, 9, 10	FCh	6, 7, 8, 9, 10, 11
15	SDRAM CAS latencies supported, MSB	00h	—	00h	—
16	SDRAM minimum CAS latencies time (tAA (min.))	69h	13.125ns	69h	13.125ns
17	SDRAM minimum write recovery time (tWR (min.))	78h	15ns	78h	15ns
18	SDRAM minimum /RAS to /CAS delay (tRCD (min.))	69h	13.125ns	69h	13.125ns
19	SDRAM minimum row active to row active delay (tRRD (min.))	30h	6ns	30h	6ns
20	SDRAM minimum row precharge time (tRP (min.))	69h	13.125ns	69h	13.125ns
21	SDRAM upper nibbles for tRAS and tRC	11h	—	11h	—
22	SDRAM minimum active to precharge time (tRAS (min.)), LSB	20h	36ns	18h	35ns
23	SDRAM minimum active to active /auto-refresh time (tRC (min.)), LSB	89h	49.125ns	81h	48.125ns
24	SDRAM minimum refresh recovery time delay (tRFC (min.)), LSB	00h	160ns	00h	160ns
25	SDRAM minimum refresh recovery time delay (tRFC (min.)), MSB	05h	160ns	05h	160ns
26	SDRAM minimum internal write to read command delay (tWTR (min.))	3Ch	7.5ns	3Ch	7.5ns
27	SDRAM minimum internal read to precharge command delay (tRTP (min.))	3Ch	7.5ns	3Ch	7.5ns
28	Upper nibble for tFAW	00h	30ns	00h	30ns
29	Minimum four activate window delay time (tFAW (min.))	F0h	30ns	F0h	30ns
30	SDRAM optional features	83h	DLL-off, RZQ/6, 7	83h	DLL-off, RZQ/6, 7
31	SDRAM thermal and refresh options	81h	PASR/2X refresh at +85°C to +95°C	81h	PASR/2X refresh at +85°C to +95°C
32	Module thermal sensor	00h	Not incorporated	00h	Not incorporated
33	SDRAM device type	00h	Standard	00h	Standard
34 to 59	Reserved	00h	—	00h	—

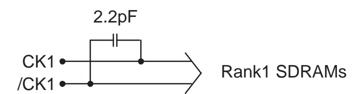
		-DJ		-GN	
Byte No.	Function described	Hex	Comments	Hex	Comments
60	Module nominal height	0Fh	29 < height ≤ 30mm	0Fh	29 < height ≤ 30mm
61	Module maximum thickness	11h	Dual sides	11h	Dual sides
62	Reference raw card used	21h	Raw Card B1	21h	Raw Card B1
63	Address mapping from edge connector to DRAM	01h	Mirrored	01h	Mirrored
64 to 116	Reserved	00h	—	00h	—
117	Module ID: manufacturer’s JEDEC ID code, LSB	02h	Elpida Memory	02h	Elpida Memory
118	Module ID: manufacturer’s JEDEC ID code, MSB	FEh	Elpida Memory	FEh	Elpida Memory
119	Module ID: manufacturing location	××	—	××	—
120	Module ID: manufacturing date	yy	Year code (BCD)	yy	Year code (BCD)
121	Module ID: manufacturing date	ww	Week code (BCD)	ww	Week code (BCD)
122 to 125	Module ID: module serial number	××	—	××	—
126	Cyclical redundancy code (CRC)	F1h	—	24h	—
127	Cyclical redundancy code (CRC)	96h	—	48h	—
128	Module part number	45h	E	45h	E
129	Module part number	42h	B	42h	B
130	Module part number	4Ah	J	4Ah	J
131	Module part number	34h	4	34h	4
132	Module part number	31h	1	31h	1
133	Module part number	55h	U	55h	U
134	Module part number	46h	F	46h	F
135	Module part number	38h	8	38h	8
136	Module part number	42h	B	42h	B
137	Module part number	43h	C	43h	C
138	Module part number	46h	F	46h	F
139	Module part number	30h	0	30h	0
140	Module part number	2Dh	—	2Dh	—
141	Module part number	44h	D	47h	G
142	Module part number	4Ah	J	4Eh	N
143	Module part number	2Dh	—	2Dh	—
144	Module part number	46h	F	46h	F
145	Module part number	20h	(Space)	20h	(Space)
146	Module revision code	30h	Initial	30h	Initial
147	Module revision code	20h	(Space)	20h	(Space)
148	SDRAM manufacturer’s JEDEC ID code, LSB	02h	Elpida Memory	02h	Elpida Memory
149	SDRAM manufacturer’s JEDEC ID code, MSB	FEh	Elpida Memory	FEh	Elpida Memory
150 to 175	Manufacturer's specific data				
176 to 255	Open for customer use	00h	—	00h	—

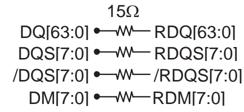
Block Diagram

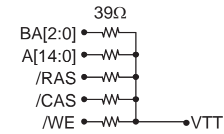


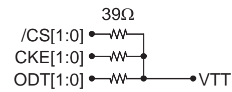
/CS0 — Rank0 SDRAMs
/CS1 — Rank1 SDRAMs
CKE0 — Rank0 SDRAMs
CKE1 — Rank1 SDRAMs
ODT0 — Rank0 SDRAMs
ODT1 — Rank1 SDRAMs
BA[2:0] — All SDRAMs
A[14:0] — All SDRAMs
/RAS — All SDRAMs
/CAS — All SDRAMs
/WE — All SDRAMs
/RESET — All SDRAMs

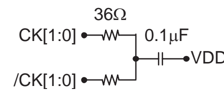


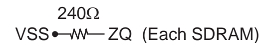


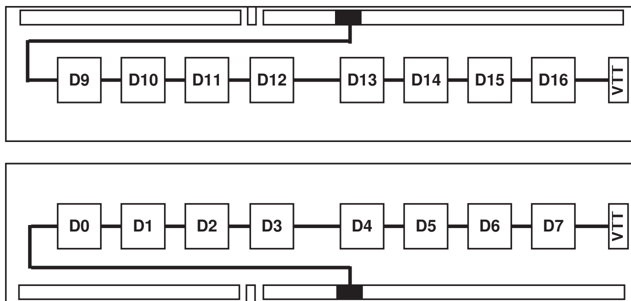


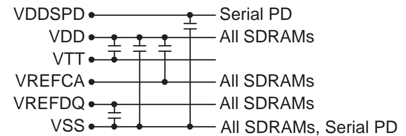




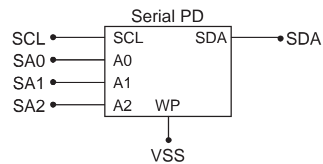








Address, command and control line



Note :
1. DQ wiring may be changed within a byte.

Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Power supply voltage	VDD	–0.4 to +1.975	V	1, 3, 4
Input voltage	VIN	–0.4 to +1.975	V	1, 4
Output voltage	VOUT	–0.4 to +1.975	V	1, 4
Reference voltage	VREFCA	–0.4 to 0.6 × VDD	V	3, 4
Reference voltage for DQ	VREFDQ	–0.4 to 0.6 × VDDQ	V	3, 4
Storage temperature	Tstg	–55 to +100	°C	1, 2, 4
Power dissipation	PD	8	W	
Short circuit output current	IOUT	50	mA	1, 4

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. DDR3 SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)
   - b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions (TC = 0°C to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.425	1.5	1.575	V	1, 2, 3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input reference voltage for address, command inputs	VREFCA (DC)	0.49 × VDD	—	0.51 × VDD	V	1, 4, 5
Input reference voltage for DQ, DM inputs	VREFDQ (DC)	0.49 × VDD	—	0.51 × VDD	V	1, 4, 5

Notes: 1. DDR3 SDRAM component specification.

2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
4. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx ±15 mV).
5. For reference: approx. VDD/2 ±15 mV.

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V, VSS = 0V)

Data rate (Mbps)		1600	1333		
Parameter	Symbol	max.	max.	Unit	Notes
Operating current (ACT-PRE) (Another rank is in IDD2P1)	IDD0	856	800	mA	
Operating current (ACT-PRE) (Another rank is in IDD3N)	IDD0	1080	1000	mA	
Operating current (ACT-READ-PRE) (Another rank is in IDD2P1)	IDD1	976	920	mA	
Operating current (ACT-READ-PRE) (Another rank is in IDD3N)	IDD1	1200	1120	mA	
Precharge power-down standby current	IDD2P1	592	560	mA	Fast PD Exit
	IDD2P0	240	240	mA	Slow PD Exit
Precharge standby current	IDD2N	800	720	mA	
Precharge standby ODT current	IDD2NT	800	720	mA	
Precharge quiet standby current	IDD2Q	800	720	mA	
Active power-down current (Always fast exit)	IDD3P	624	592	mA	
Active standby current	IDD3N	1040	960	mA	
Operating current (Burst read operating) (Another rank is in IDD2P1)	IDD4R	1576	1400	mA	
Operating current (Burst read operating) (Another rank is in IDD3N)	IDD4R	1800	1600	mA	
Operating current (Burst write operating) (Another rank is in IDD2P1)	IDD4W	1616	1440	mA	
Operating current (Burst write operating) (Another rank is in IDD3N)	IDD4W	1840	1640	mA	
Burst refresh current (Another rank is in IDD2P1)	IDD5B	2296	2200	mA	
Burst refresh current (Another rank is in IDD3N)	IDD5B	2520	2400	mA	
All bank interleave read current (Another rank is in IDD2P1)	IDD7	2376	2280	mA	
All bank interleave read current (Another rank is in IDD3N)	IDD7	2600	2480	mA	
RESET low current	IDD8	272	272	mA	

Self-Refresh Current (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V)

Parameter	Symbol	max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	272	mA	
Self-refresh current extended temperature range	IDD6ET	352	mA	
Auto self-refresh current (optional)	IDD6TC	—	mA	

Timings used for IDD and IDDQ Measurement-Loop Patterns

	DDR3-1600	DDR3-1333	
Parameter	11-11-11	9-9-9	Unit
CL	11	9	nCK
tCK min.	1.25	1.5	ns
nRCD min.	11	9	nCK
nRC min.	39	33	nCK
nRAS min.	28	24	nCK
nRP min.	11	9	nCK
nFAW	24	20	nCK
nRRD	5	4	nCK
nRFC	128	107	nCK

Pin Functions

CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pins)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A14 (input pins)

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

[Address Pins Table]

Address (A0 to A14)		Notes
Row address (RA)	Column address (CA)	
AX0 to AX14	AY0 to AY9	

A10(AP) (input pin)

A10 is sampled during read/write commands to determine whether auto-precharge should be performed to the accessed bank after the read/write operation. (high: auto-precharge; low: no auto-precharge)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

A12 (/BC) (input pin)

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.)

BA0 to BA2 (input pins)

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine if a mode register is to be accessed during a MRS cycle.

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pins)

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DQ (input and output pins)

Bi-directional data bus.

DQS and /DQS (input and output pins)

Output with read data, input with write data. Edge-aligned with read data, centered in write data.
The data strobe DQS is paired with differential signals /DQS to provide differential pair signaling to the system during READs and WRITEs.

ODT (input pins)

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

DM (input pins)

DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.

VDD (power supply pins)

1.5V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)

3.3V is applied (For serial EEPROM).

VSS (power supply pins)

Ground is connected.

VTT (power supply pins)

I/O termination supply for SDRAM.

VREFDQ (power supply pin)

Reference voltage for DQ.

VREFCA (power supply pin)

Reference voltage for CA.

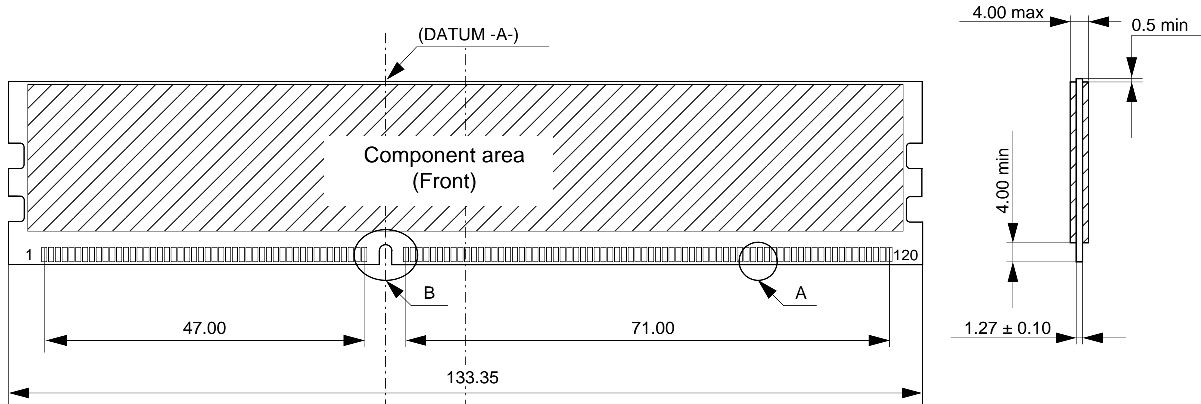
/RESET (input pin)

/RESET is negative active signal (active low) and is referred to VSS.

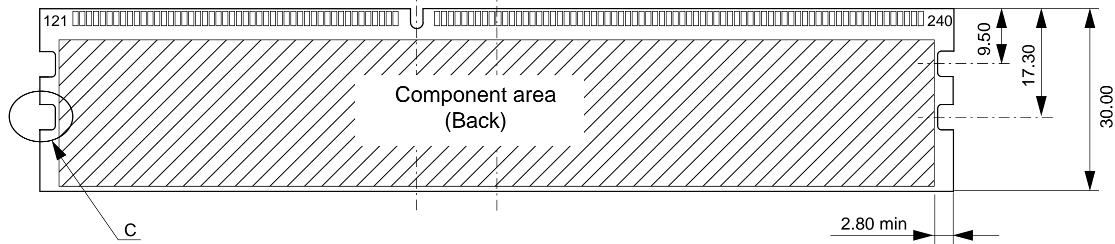
Physical Outline

Unit: mm

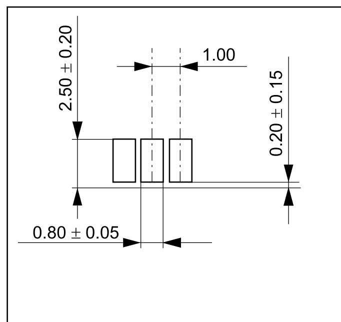
Front side



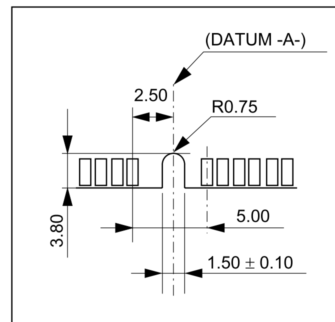
Back side



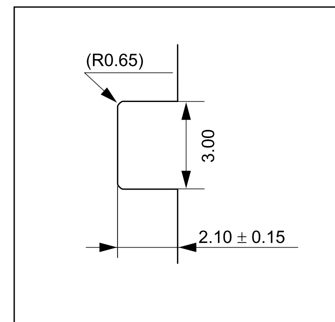
Detail A



Detail B



Detail C



ECA-TS2-0192-03

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Usage environment]
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Accordingly, our company assumes no responsibility for loss of a customer or a third party when used in environments with the special characteristics listed below.

Example:

1) Usage in liquids, including water, oils, chemicals and organic solvents.
2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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