PRELIMINARY DATA SHEET

ELPIDA

MOS INTEGRATED CIRCUIT

MC-45D16CD641KS

16 M-WORD BY 64-BIT DDR SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-45D16CD641KS is a 16,777,216 words by 64 bits DDR synchronous dynamic RAM module on which 8 pieces of 128M DDR SDRAM: μPD45D128164 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 16,777,216 words by 64 bits organization
- Clock frequency

Part number	/CAS latency	Clock frequency (MAX.)	Module type
MC-45D16CD641KS-C75	CL = 2.5	133 MHz	DDR SDRAM
	CL = 2	100 MHz	SO DIMM
MC-45D16CD641KS-C80	CL = 2.5	125 MHz	Design specification
	CL = 2	100 MHz	Rev.1.0 compliant

- Fully Synchronous Dynamic RAM with all signals except DM, DQS and DQ referenced to a positive clock edge
- Double Data Rate interface
  Differential CLK (/CLK) input
  Data inputs and DM are synchronized with both edges of DQS
  Data outputs and DQS are synchronized with a cross point of CLK and /CLK
- Quad internal banks operation
- Possible to assert random column address in every clock cycle
- Programmable Mode register set
  /CAS latency (2, 2.5)
  Burst length (2, 4, 8)
  Wrap sequence (Sequential / Interleave)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- 2.5 V $\pm$ 0.2 V Power supply for V_{DD}
- 2.5 V $\pm$ 0.2 V Power supply for $V_{DD}Q$
- SSTL_2 compatible with all signals
- 4,096 refresh cycles / 64 ms
- Burst termination by Precharge command and Burst stop command
- 200-pin dual in-line memory module (Pin pitch = 0.6 mm)
- Unbuffered type
- Serial PD

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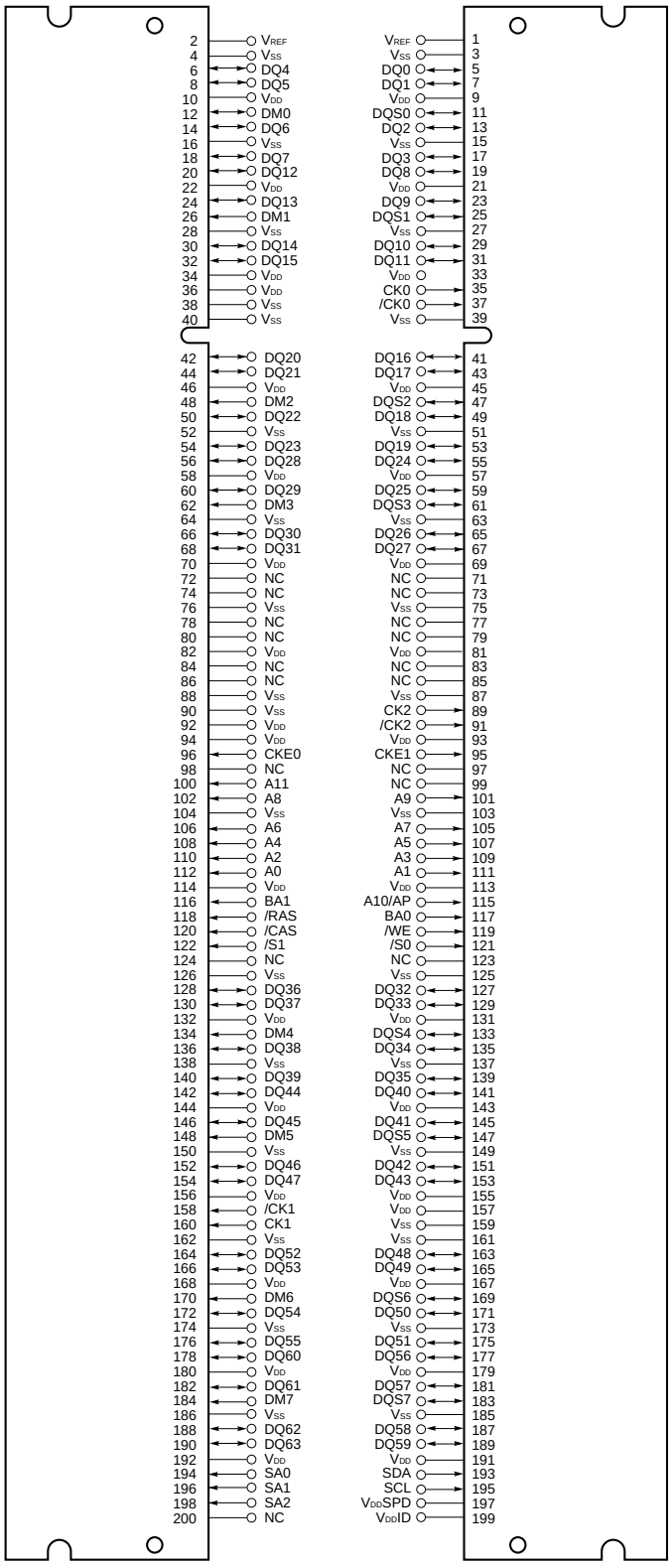
Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

Ordering Information

Part number	Clock frequency (MAX.)	Package	Mounted devices
MC-45D16CD641KS-C75	133 MHz	200-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plated 31.75 mm height	8 pieces of μPD45D128164G5 (Rev. K) (10.16 mm (400) TSOP (II))
MC-45D16CD641KS-C80	125 MHz		

Pin Configuration

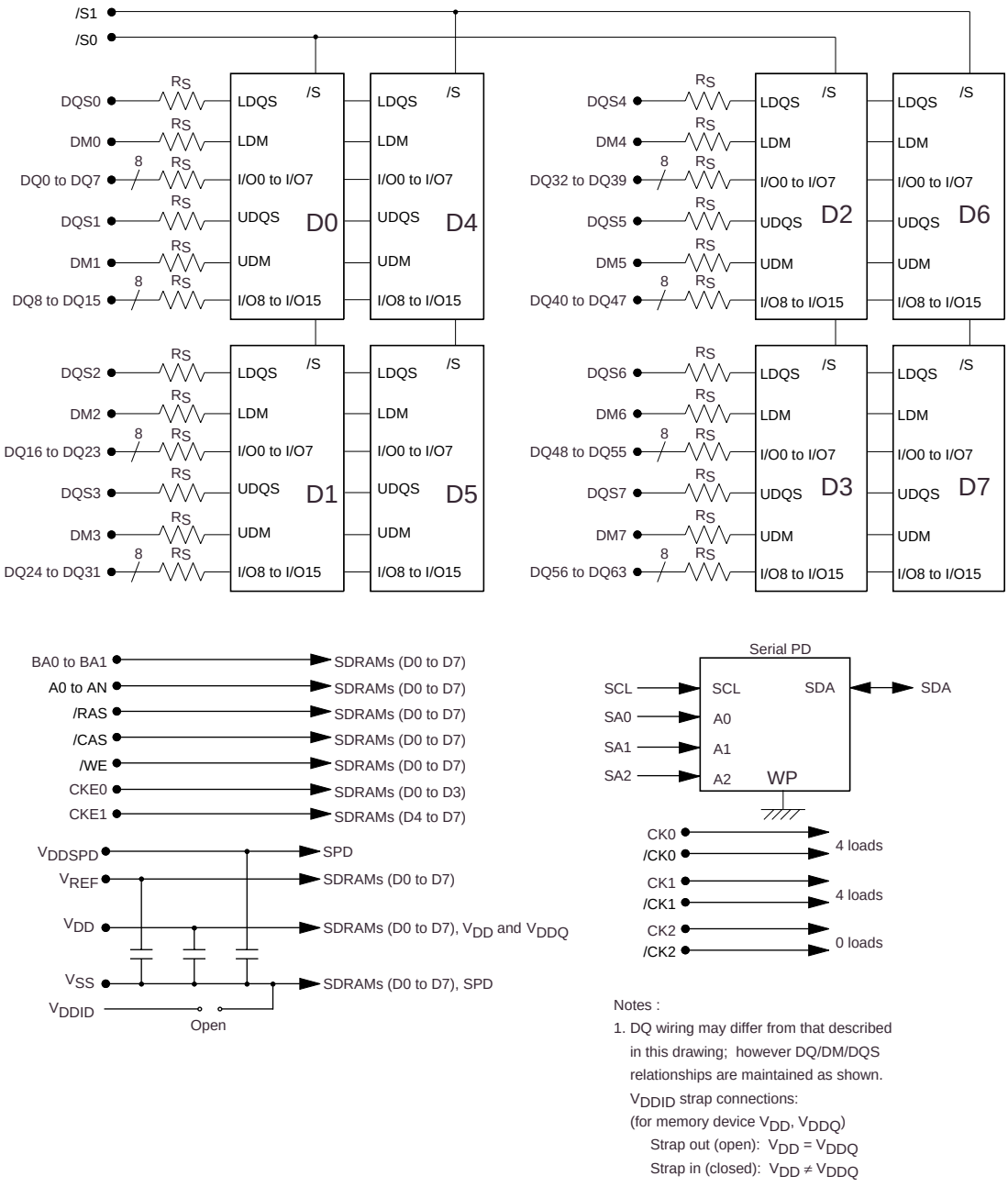
200-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

A0 - A11	:	Address Inputs
[Row: A0 - A11, Column: A0 - A9]		
BA0, BA1	:	SDRAM Bank Select
DQ0 - DQ63	:	Data Inputs/Outputs
CK0 - CK2	:	Clock Input
(positive line of differential pair)		
/CK0 - /CK2	:	Clock Input
(negative line of differential pair)		
CKE0	:	Clock Enable Input
/S0, /S1	:	Chip Select Input
/RAS	:	Row Address Strobe
/CAS	:	Column Address Strobe
/WE	:	Write Enable
DQS0 - DQS7	:	Low Data Strobe
DM(0 - 7) / DQS(9 - 16)	:	Low Data Masks / High Data Strobe
SA0 - SA2	:	Address Input for EEPROM
SDA	:	Serial Data I/O for PD
SCL	:	Clock Input for PD
V_{DD}	:	Power Supply
V_{SS}	:	Ground
V_{DD}ID	:	V_{DD} Identification Flag
V_{DD}Q	:	Power Supply for DQ and DQS
V_{REF}	:	Input Reference
V_{DD}SPD	:	Power supply for EEPROM
NC	:	No Connection
/RESET	:	Reset Input

Block Diagram



Notes :

1. DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
   V_{DDID} strap connections:
   (for memory device V_{DD}, V_{DDQ})
   Strap out (open): $V_{DD} = V_{DDQ}$
   Strap in (closed): $V_{DD} \neq V_{DDQ}$

Remarks 1. The value of all resistors of DQs, DQSs, DM/DQSs is 22 Ω.± 5%

2. D0 – D7: μPD45D128164 (2M words × 16 bits × 4 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute **Power on sequence and CBR (Auto) refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to V_{SS}	V_{DD}, $V_{DD}Q$		–0.5 to +3.6	V
Voltage on input pin relative to V_{SS}	V_T		–0.5 to +3.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		12	W
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.3	2.5	2.7	V
Supply voltage for DQ, DQS	$V_{DD}Q$		2.3	2.5	2.7	V
Input reference voltage	V_{REF}		$0.49 \times V_{DD}Q$		$0.51 \times V_{DD}Q$	V
Termination voltage	V_{TT}		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
High level dc input voltage	V_{IH} (DC)		$V_{REF} + 0.15$		$V_{DD} + 0.3$	V
Low level dc input voltage	V_{IL} (DC)		–0.3		$V_{REF} - 0.15$	V
Input differential voltage (CLK and /CLK)	V_{ID} (DC)		0.36		$V_{DD}Q + 0.6$	V
Input crossing point voltage (CLK and /CLK)	V_{IX}		$0.5 \times V_{DD}Q$–0.2		$0.5 \times V_{DD}Q$+0.2	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 100 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0, BA1, /RAS, /CAS, /WE	TBD		TBD	pF
	C_{I2}	CK0 - CK2, /CK0 - /CK2	TBD		TBD	
	C_{I3}	CKE0	TBD		TBD	
	C_{I4}	/S0, /S1	TBD		TBD	
Data input/output capacitance	$C_{I/O1}$	DM(0-7) / DQS(9-16), DQS0 - DQS7	TBD		TBD	pF
	$C_{I/O2}$	DQ0 - DQ63	TBD		TBD	

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	/CAS latency	Grade	MIN.	MAX.	Unit	Notes
Operating current (ACT-PRE)	I_{DD0}	t_{RC} = $t_{RC(MIN.)}$, t_{CK} = $t_{CK(MIN.)}$, One bank, Active-precharge, DQ, DM and DQS inputs changing twice per clock cycle, Address and control inputs changing once per clock cycle		-C75		920	mA	
				-C80		840		
Operating current (ACT-READ-PRE)	I_{DD1}	t_{RC} = $t_{RC(MIN.)}$, t_{CK} = $t_{CK(MIN.)}$, One bank, Active-read-precharge, I_O = 0 mA, Burst length = 2, Address and control inputs changing once per clock cycle	CL = 2	-C75		980	mA	1
				-C80		920		
			CL = 2.5	-C75		1020		
				-C80		960		
Precharge power down standby current	I_{DD2P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = $t_{CK(MIN.)}$, All banks idle, Power down mode				80	mA	
Idle standby current	I_{DD2N}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = $t_{CK(MIN.)}$, /CS ≥ $V_{IH(MIN.)}$, All banks idle, Address and other control inputs changing once per clock cycle				400	mA	
Active power down standby current	I_{DD3P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = $t_{CK(MIN.)}$, One bank active, Power down mode				400	mA	
Active standby current	I_{DD3N}	/CS ≥ $V_{IH(MIN.)}$, CKE ≥ $V_{IH(MIN.)}$, t_{CK} = $t_{CK(MIN.)}$, t_{RC} = $t_{RAS(MAX.)}$, One bank, Active-precharge, DQ, DM and DQS inputs changing twice per clock cycle, Address and other control inputs changing once per clock cycle				560	mA	
Operating current (Burst read)	I_{DD4R}	t_{CK} = $t_{CK(MIN.)}$, Continuous burst read, Burst length = 2, I_O = 0mA, One bank active, Address and control inputs changing once per clock cycle	CL = 2	-C75		1080	mA	2
				-C80		1080		
			CL = 2.5	-C75		1340		
				-C80		1280		
Operating current (Burst write)	I_{DD4W}	t_{CK} = $t_{CK(MIN.)}$, Continuous burst write, Burst length = 2, One bank active, Address and control inputs changing once per clock cycle	CL = 2	-C75		1040	mA	2
				-C80		1040		
			CL = 2.5	-C75		1300		
				-C80		1240		
CBR (Auto) refresh current	I_{DD5}	t_{RFC} = $t_{RFC(MIN.)}$		-C75		1360	mA	
				-C80		1280		
Self refresh current	I_{DD6}	CKE ≤ 0.2 V				16	mA	

Notes 1. I_{DD1} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{DD4R} and I_{DD4W} depend on output loading and cycle rates. Specified values are obtained with the output open.

DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, all other pins not under test = 0 V	–5	5	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to $V_{DD}Q$ + 0.3 V	–5	5	μA	
Output high current	I_{OH}	V_{OUT} = $V_{DD}Q$ – 0.43 V	–15.2		mA	
Output low current	I_{OL}	V_{OUT} = 0.35 V	15.2		mA	

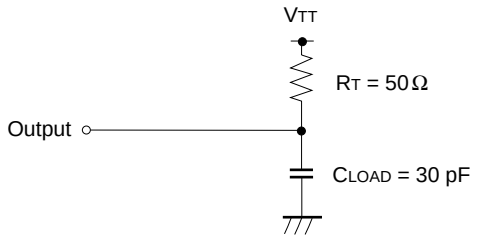
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

Parameter	Symbol	Value	Unit	Notes
Input Reference voltage (Input timing measurement reference level)	V_{REF}	$V_{DD}Q$ x 0.5	V	
Termination voltage (Output timing measurement reference level)	V_{TT}	V_{REF}	V	1
High level ac input voltage	V_{IH}(ac)	V_{REF} + 0.31	V	
Low level ac input voltage	V_{IL}(ac)	V_{REF} – 0.31	V	
Input differential voltage (CK0 - CK2 and /CK0 - /CK2)	V_{ID}(ac)	0.7	V	
Input signal slew rate	SLEW	1	V/ns	2

Notes 1. Output waveform timing is measured where the output signal crosses through the V_{TT} level.

2. Slew rate is to be maintained in the V_{IL} (ac) to V_{IH}(ac) range of the input signal swing. SLEW = (V_{IH}(ac)-V_{IL}(ac))/ Δt



Synchronous Characteristics

Parameter		Symbol	-C75 (PC266B)		-C80 (PC200)		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	CL = 2.5	t_{CK}	7.5	15	8	15	ns	
	CL = 2		10	15	10	15		
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
DQ output access time from CLK, /CLK		t_{AC}	–0.75	0.75	–0.8	0.8	ns	
DQS output access time from CLK, /CLK		t_{DQSCK}	–0.75	0.75	–0.8	0.8	ns	
DQS-DQ skew (for DQS and associated DQ signals)		t_{DQSQ}	–0.5	0.5	–0.6	0.6	ns	
DQS-DQ skew (for DQS and all DQ signals)		t_{DQSQA}	–0.5	0.5	–0.6	0.6	ns	
Data out low-impedance time from CLK, /CLK		t_{LZ}	–0.75	0.75	–0.8	0.8	ns	
Data out high-impedance time from CLK, /CLK		t_{HZ}	–0.75	0.75	–0.8	0.8	ns	
Half clock period		t_{HP}	t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns	
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} – 0.75		t_{HP} – 1		ns	
DQ and DM input setup time		t_{DS}	0.5		0.6		ns	
DQ and DM input hold time		t_{DH}	0.5		0.6		ns	
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		2		ns	
DQS write preamble setup time		t_{WPRES}	0		0		ns	
DQS write preamble		t_{WPRE}	0.25		0.25		t_{CK}	
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}	
DQS falling edge to CLK setup time		t_{DSS}	0.2		0.2		t_{CK}	
DQS falling edge hold time from CLK		t_{DSH}	0.2		0.2		t_{CK}	
Address and control input setup time		t_{IS}	0.9		1.1		ns	
Address and control input hold time		t_{IH}	0.9		1.1		ns	
Address and control input pulse width		t_{IPW}	2.2		2.5		ns	
Internal write to read command delay		t_{WTR}	1		1		t_{CK}	

Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics

Parameter	Symbol	-C75 (PC266B)		-C80 (PC200)		Unit
		MIN.	MAX.	MIN.	MAX.	
ACT to REF/ACT command period (operation)	t_{RC}	65		70		ns
REF to REF/ACT command period (refresh)	t_{RFC}	75		80		ns
ACT to PRE command period	t_{RAS}	45	120,000	50	120,000	ns
PRE to ACT command period	t_{RP}	20		20		ns
ACT to READ/WRITE delay	t_{RCD}	20		20		ns
ACT(one) to ACT(another) command period	t_{RRD}	15		15		ns
Write recovery time	t_{WR}	15		15		ns
Auto precharge write recovery time + precharge time	t_{DAL}	35		35		ns
Mode register set command cycle time	t_{MRD}	15		15		ns
Exit self refresh to command	t_{XSNR}	75		80		ns
Refresh time (4,096 refresh cycles)	t_{REF}		64		64	ms

Serial PD **(1/2)**

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		07H	0	0	0	0	0	1	1	1	DDR SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks		02H	0	0	0	0	0	0	1	0	2 banks
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		04H	0	0	0	0	0	1	0	0	SSTL_2
9	CL = 2.5 Cycle time	-C75	75H	0	1	1	1	0	1	0	1	7.5 ns
		-C80	80H	1	0	0	0	0	0	0	0	8 ns
10	CL = 2.5 Access time	-C75	75H	0	1	1	1	0	1	0	1	0.75 ns
		-C80	80H	1	0	0	0	0	0	0	0	0.8 ns
11	DIMM configuration type		00H	0	0	0	0	0	0	0	0	None
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		10H	0	0	0	1	0	0	0	0	x8
14	Error checking SDRAM width		00H	0	0	0	0	0	0	0	0	None
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		0EH	0	0	0	0	1	1	1	0	2, 4, 8
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		0CH	0	0	0	0	1	1	0	0	2, 2.5
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		02H	0	0	0	0	0	0	1	0	1
21	SDRAM module attributes		20H	0	0	1	0	0	0	0	0	Differential Clock
22	SDRAM device attributes : General		00H	0	0	0	0	0	0	0	0	$V_{DD} \pm 0.2$ V
23	CL = 2 Cycle time	-C75	A0H	1	0	1	0	0	0	0	0	10 ns
		-C80	A0H	1	0	1	0	0	0	0	0	10 ns
24	CL = 2 Access time	-C75	75H	0	1	1	1	0	1	0	1	0.75 ns
		-C80	80H	1	0	0	0	0	0	0	0	0.8 ns
25-26												
27	$t_{RP(MIN.)}$	-C75	50H	0	1	0	1	0	0	0	0	20 ns
		-C80	50H	0	1	0	1	0	0	0	0	20 ns
28	$t_{RRD(MIN.)}$	-C75	3CH	0	0	1	1	1	1	0	0	15 ns
		-C80	3CH	0	0	1	1	1	1	0	0	15 ns
29	$t_{RCD(MIN.)}$	-C75	50H	0	1	0	1	0	0	0	0	20 ns
		-C80	50H	0	1	0	1	0	0	0	0	20 ns
30	$t_{RAS(MIN.)}$	-C75	2DH	0	0	1	0	1	1	0	1	45 ns
		-C80	32H	0	0	1	1	0	0	1	0	50 ns
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes

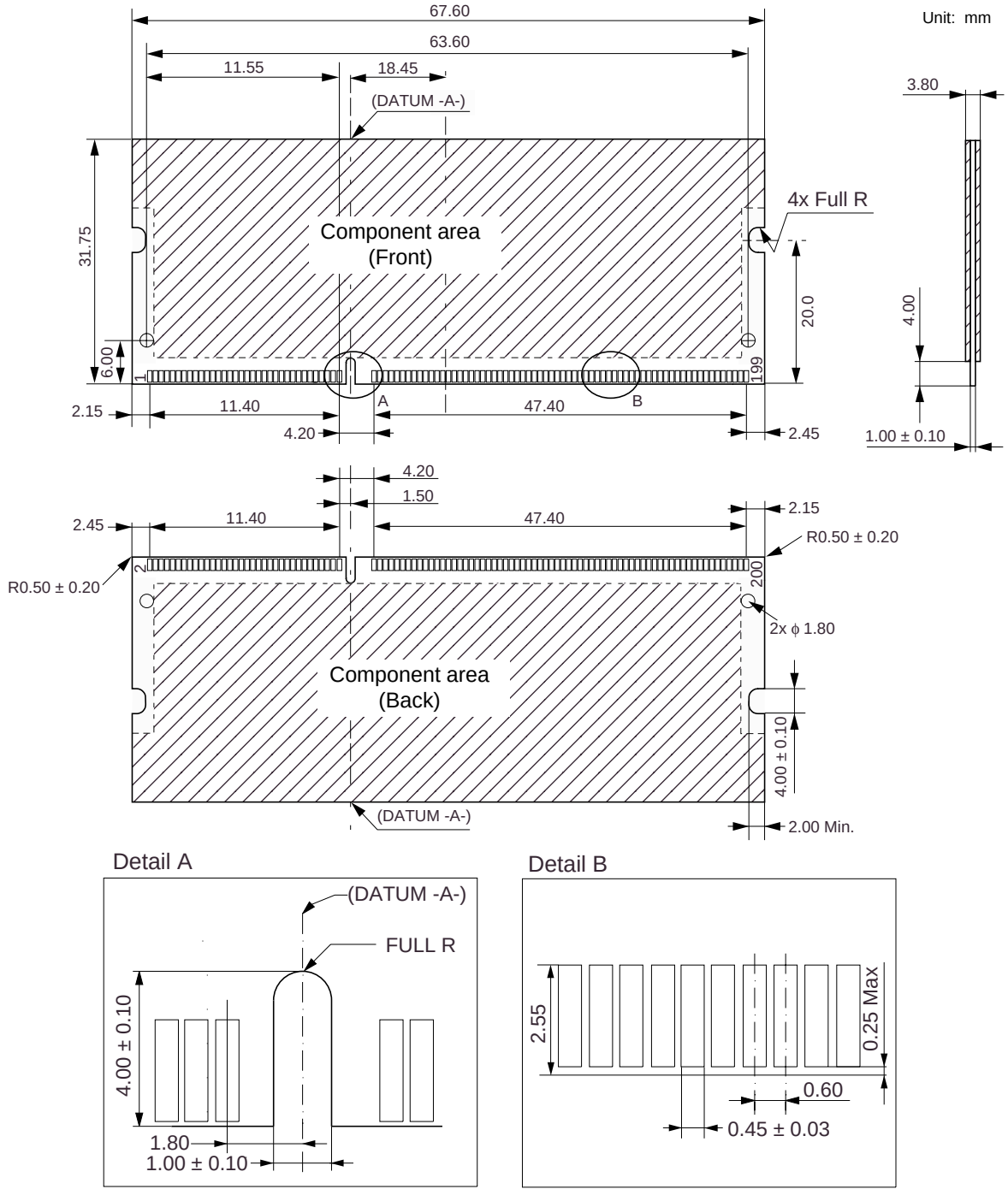
(2/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal	-C75	90H	1	0	0	1	0	0	0	0	0.9 ns
	input setup time	-C80	B0H	1	0	1	1	0	0	0	0	1.1 ns
33	Command and address	-C75	90H	1	0	0	1	0	0	0	0	0.9 ns
	signal input hold time	-C80	B0H	1	0	1	1	0	0	0	0	1.1 ns
34	Data signal input setup time	-C75	50H	0	1	0	1	0	0	0	0	0.5 ns
		-C80	60H	0	1	1	0	0	0	0	0	0.6 ns
35	Data signal input hold time	-C75	50H	0	1	0	1	0	0	0	0	0.5 ns
		-C80	60H	0	1	1	0	0	0	0	0	0.6 ns
36-61												
62	SPD revision		00H	0	0	0	0	0	0	0	0	
63	Checksum for bytes 0 - 62	-C75	94H	1	0	0	1	0	1	0	0	
		-C80	1AH	0	0	0	1	1	0	1	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-99	Assembly serial number											
100-127	Mfg specific		00H	0	0	0	0	0	0	0	0	

Timing Chart

Refer to the μPD45D128442, 45D128842, 45D128164 Data sheet (E0030N).

Package Drawing



CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0107

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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