

**16M-WORD BY 64-BIT  
VirtualChannel™ DYNAMIC RAM MODULE (SO DIMM)****Description**

The MC-45V16AD642KS is a 16,777,216 words by 64 bits VirtualChannel dynamic RAM module (small outline DIMM) on which 8 pieces of 128M VirtualChannel DRAM :  $\mu$ PD45V128161 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

**Features**

- 16,777,216 words by 64 bits organization
- Clock frequency and access time from CLK

Part number	Read latency	Clock frequency MHz (MAX.)	Access time from CLK ns (MAX.)	Maximum supply current mA				
				Operating			Refresh	
				Prefetch	Restore	Channel read / write (Burst)	Auto	Self
MC-45V16AD642KS-A75	2	133	5.4	720		420	1,040	16

- Fully Standard Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Programmable wrap sequence (interleave)
- Programmable burst length (4)
- Read latency (2)
- Prefetch read latency (4)
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V  $\pm$  0.3 V power supply
- Interface: LVTTL
- Refresh cycle: 4K cycles/64 ms
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

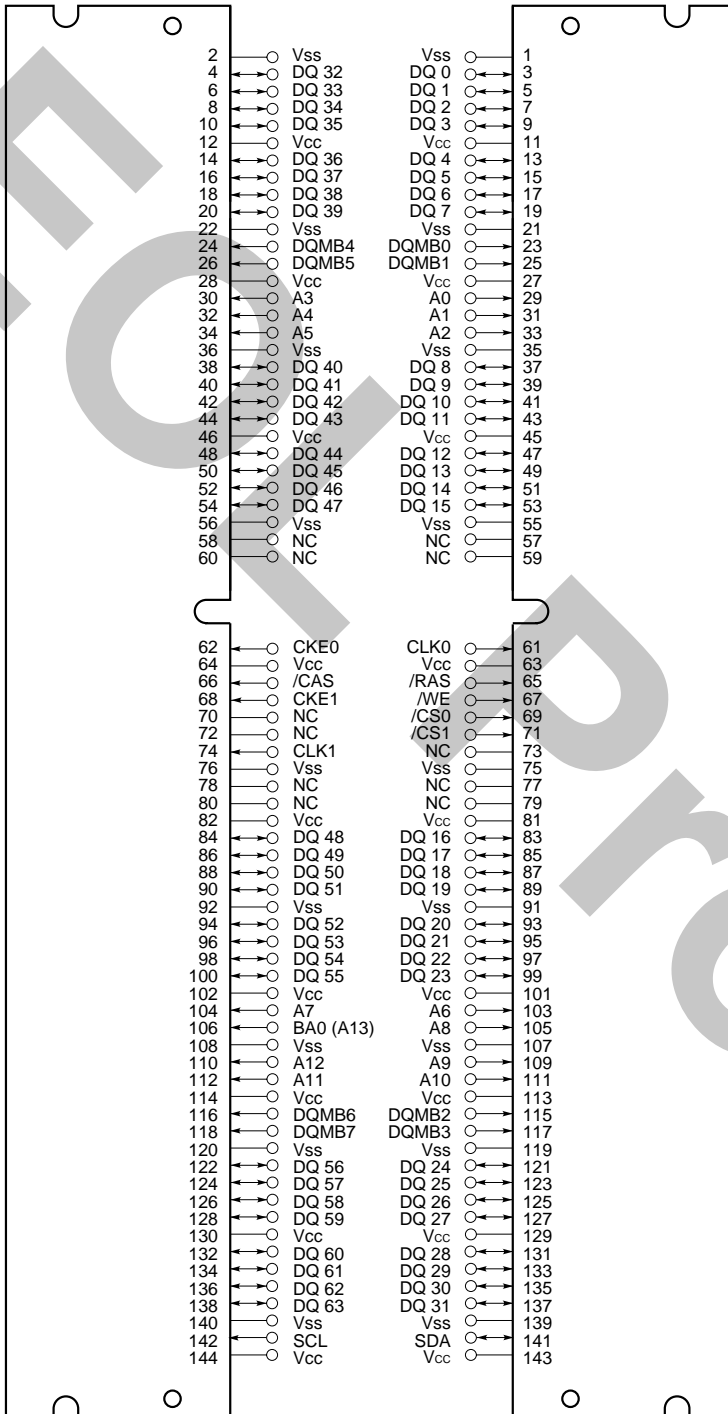
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Not all devices/types available in every country. Please check with local Elpida Memory, Inc. for availability and additional information.

**Ordering Information**

Part number	Clock frequency MHz (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
MC-45V16AD642KS-A75	133	2	4	144-pin Small Outline DIMM (Socket Type) Edge connector : Gold plated 31.75 mm height	8 pieces of $\mu$ PD45V128161G5 (10.16 mm (400) TSOP (II))

Pin Configuration

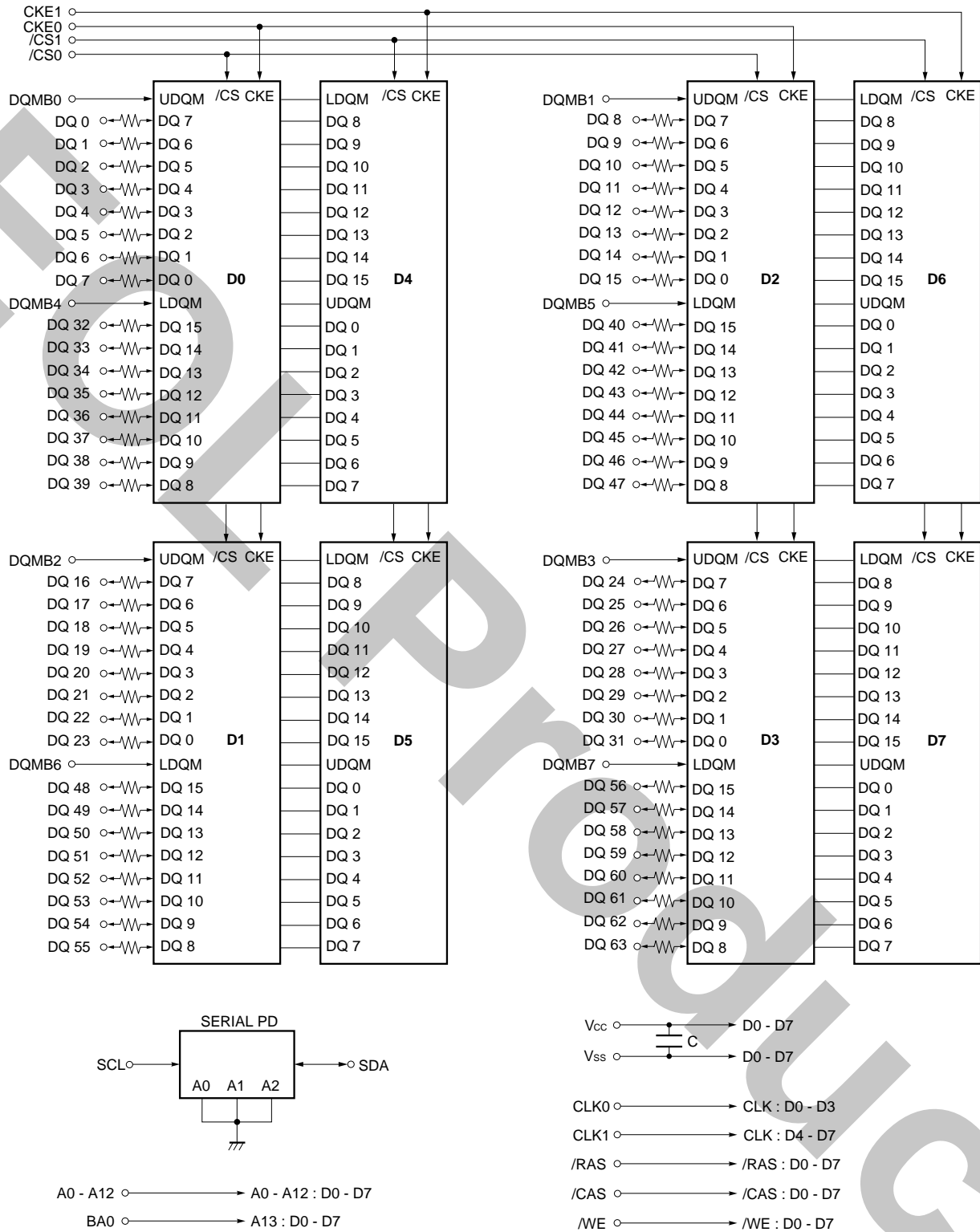
144-pin Small Outline Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

- A0 - A12 : Address Inputs  
[Row: A0 - A12, Column: A0 - A6]
- BA0 (A13) : VirtualChannel DRAM Bank Select
- DQ0 - DQ63 : Data Inputs/Outputs
- CLK0, CLK1 : Clock Input
- CKE0, CKE1 : Clock Enable Input
- /CS0, /CS1 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- NC : No Connection

Block Diagram



**Remark** D0 - D7:  $\mu$ PD45V128161 (4M words  $\times$  16 bits  $\times$  2 banks)

**Electrical Specifications**

- All voltages are referenced to V<sub>SS</sub> (GND).
- After power up, wait more than 100  $\mu$ s and then, execute power on sequence and auto refresh before proper device operation is achieved.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V <sub>CC</sub>		-0.5 to +4.6	V
Voltage on input pin relative to GND	V <sub>T</sub>		-0.5 to +4.6	V
Short circuit output current	I <sub>O</sub>		50	mA
Power dissipation	P <sub>D</sub>		8	W
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>sig</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I1</sub>	A0 - A12, BA0 (A13), /RAS, /CAS, /WE	30		60	pF
	C <sub>I2</sub>	CLK0, CLK1	23		37	
	C <sub>I3</sub>	CKE0, CKE1	18		30	
	C <sub>I4</sub>	/CS0, /CS1	18		30	
	C <sub>I5</sub>	DQMB0 - DQMB7	7		14	
Data input/output capacitance	C <sub>I/O</sub>	DQ0 - DQ63	7		18	pF

## DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

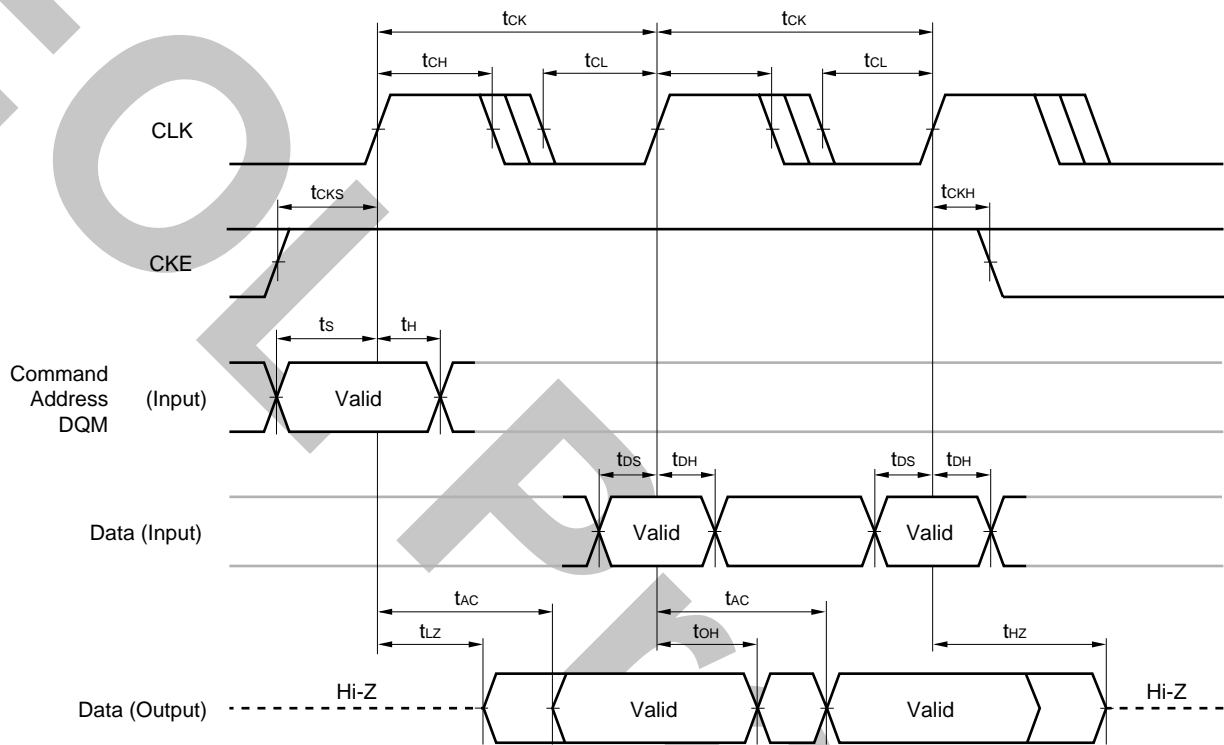
Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	I <sub>CC1P</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub> Prefetch is executed one time during t <sub>RC</sub> .	-A75		720	mA	1
Operating current (Restore mode at one bank active)	I <sub>CC1R</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	-A75		720	mA	1
Precharge standby current in power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns			9.6	mA	
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞			9.6		
Precharge standby current in non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.			160	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.			80		
Active standby current in power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns			48	mA	
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞			48		
Active standby current in non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.			240	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.			160		
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK (MIN.)</sub> , I <sub>O</sub> = 0 mA Background : precharge standby	-A75		420	mA	2
Auto Refresh current	I <sub>CC5</sub>	t <sub>RCF</sub> ≥ t <sub>RCF (MIN.)</sub>	-A75		1,040	mA	3
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2 V	-A75		16	mA	
Input leakage current	I <sub>I (L)</sub>	V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V		-8	+8	μA	
Output leakage current	I <sub>O (L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -4.0 mA		2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +4.0 mA			0.4	V	

- Notes**
1. I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  2. I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  3. I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

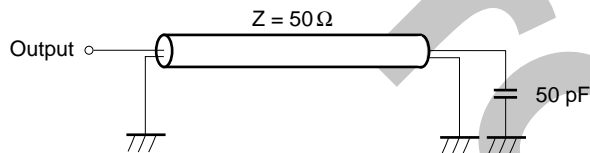
- AC measurements assume  $t_r = 1$  ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- If  $t_r$  is longer than 1 ns, reference level for measuring timing of input signals is  $V_{IH(MIN.)}$  and  $V_{IL(MAX.)}$ .
- An access time is measured at 1.4 V.



AC characteristics

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
Clock cycle time	t <sub>CK2</sub>	7.5	–	ns	
Access time from CLK	t <sub>AC2</sub>	–	5.4	ns	1
CLK high level width	t <sub>CH</sub>	2.5	–	ns	
CLK low level width	t <sub>CL</sub>	2.5	–	ns	
Data-out hold time	t <sub>OH</sub>	2.7	–	ns	1
Data-out low-impedance time	t <sub>LZ</sub>	0	–	ns	
Data-out high-impedance time	t <sub>HZ2</sub>	2.5	5.4	ns	
Data-in setup time	t <sub>DS</sub>	1.5	–	ns	
Data-in hold time	t <sub>DH</sub>	0.8	–	ns	
Address, Command, DQM setup time	t <sub>S</sub>	1.5	–	ns	
Address, Command, DQM hold time	t <sub>H</sub>	0.8	–	ns	
CKE setup time	t <sub>CKS</sub>	1.5	–	ns	
CKE hold time	t <sub>CKH</sub>	0.8	–	ns	
CKE setup time (Power down exit)	t <sub>CKSP</sub>	1.5	–	ns	
Transition time	t <sub>T</sub>	0.5	30	ns	
Refresh time (4,096 refresh cycle)	t <sub>REF</sub>	–	64	ms	
Mode register set cycle time	t <sub>RSC</sub>	2	–	CLK	

Note 1. Output load.



**AC characteristics (Background to Background operation)**

Parameter	Symbol	-A75		Unit	Notes
		MIN.	MAX.		
<b>Same Bank Operation</b>					
ACT to ACT/REF Command period	t <sub>RC</sub>	67.5	–	ns	
REF to REF / ACT Command period	t <sub>RCF</sub>	67.5	–	ns	
ACT to PRE Command period	t <sub>RAS</sub>	52.5	120,000	ns	
PRE to ACT / REF Command period	t <sub>RP</sub>	20	–	ns	
ACT to PFC/PFCA Command delay time	t <sub>APD</sub>	15	–	ns	
ACT to PFR Command delay time (Prefetch Read Operation)	t <sub>APRD</sub>	15	–	ns	
PFC to PRE Command delay time	t <sub>PPL</sub>	22.5	–	ns	
PFCA / PFR to ACT/REF Command delay time	t <sub>PAL</sub>	45	–	ns	
RST / RSTA to ACT(R) <sup>Note1</sup> Command delay time	t <sub>RAD</sub>	7.5	30	ns	2
<b>Same, Other Bank Operation</b>					
ACT(R) <sup>Note1</sup> to PFC/PFCA/PFR Command delay time	t <sub>RPD</sub>	37.5	–	ns	
PFC to PFC / PFCA Command delay time	t <sub>PPD</sub>	22.5	–	ns	
<b>Other Bank Operation</b>					
ACT to ACT/ACT(R) or ACT(R) to ACT Command delay time	t <sub>RRD</sub>	15	–	ns	
ACT(R) to ACT(R) Command delay time	t <sub>RRDR</sub>	30	–	ns	
PFC /PFCA to RST /RSTA Command delay time	t <sub>PRD</sub>	22.5	–	ns	

**Notes** 1. ACT (R) command is ACT command after RST command.

2. The another background operation and same channel foreground operation are illegal while t<sub>RAD</sub> period.

**AC characteristics (Foreground to Foreground operation)**

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
READ/WRITE to READ/WRITE Command delay time	t <sub>CCD</sub>	7.5	–	ns	

**AC characteristics (Background to Foreground operation)  
(after same channel Prefetch/Restore)**

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
PFC/PFCA to READ/WRITE Command delay time	t <sub>PCD</sub>	15	–	ns	
ACT(R) to READ/WRITE Command delay time	t <sub>RCD</sub>	30	–	ns	1

**Note 1.** ACT (R) command is ACT command after RST command.

Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	08H	0	0	0	0	1	0	0	0	VC DRAM	
3	Number of row addresses	0DH	0	0	0	0	1	1	0	1	13 rows	
4	Number of column addresses	07H	0	0	0	0	0	1	1	1	7 columns	
5	Number of banks	02H	0	0	0	0	0	0	1	0	2 banks	
6	Data width	40H	0	1	0	0	0	0	0	0	64 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface standard	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	Read latency (/CAS latency) = 2 cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	Read latency (/CAS latency) = 2 access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type	00H	0	0	0	0	0	0	0	0	0	None
12	Refresh rate / type	80H	1	0	0	0	0	0	0	0	0	Normal
13	VC DRAM width	10H	0	0	0	1	0	0	0	0	0	×16
14	Error checking DRAM width	00H	0	0	0	0	0	0	0	0	0	None
15	Minimum clock delay	01H	0	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported	04H	0	0	0	0	0	1	0	0	0	4
17	Number of banks on each VC DRAM	02H	0	0	0	0	0	0	1	0	0	2 banks
18	Read latency (/CAS latency) supported	02H	0	0	0	0	0	0	1	0	0	2
19	/CS latency supported	01H	0	0	0	0	0	0	0	0	1	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	0	1	0
21	VC DRAM module attributes	00H	0	0	0	0	0	0	0	0	0	
22	VC DRAM device attributes : general	0EH	0	0	0	0	1	1	1	1	0	
23-26		00H	0	0	0	0	0	0	0	0	0	
27	t <sub>RP</sub> (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
28	t <sub>RRD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	t <sub>APD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
30	t <sub>RAS</sub> (MIN.)	-A75	34H	0	0	1	1	0	1	0	0	52.5 ns

(2/2)

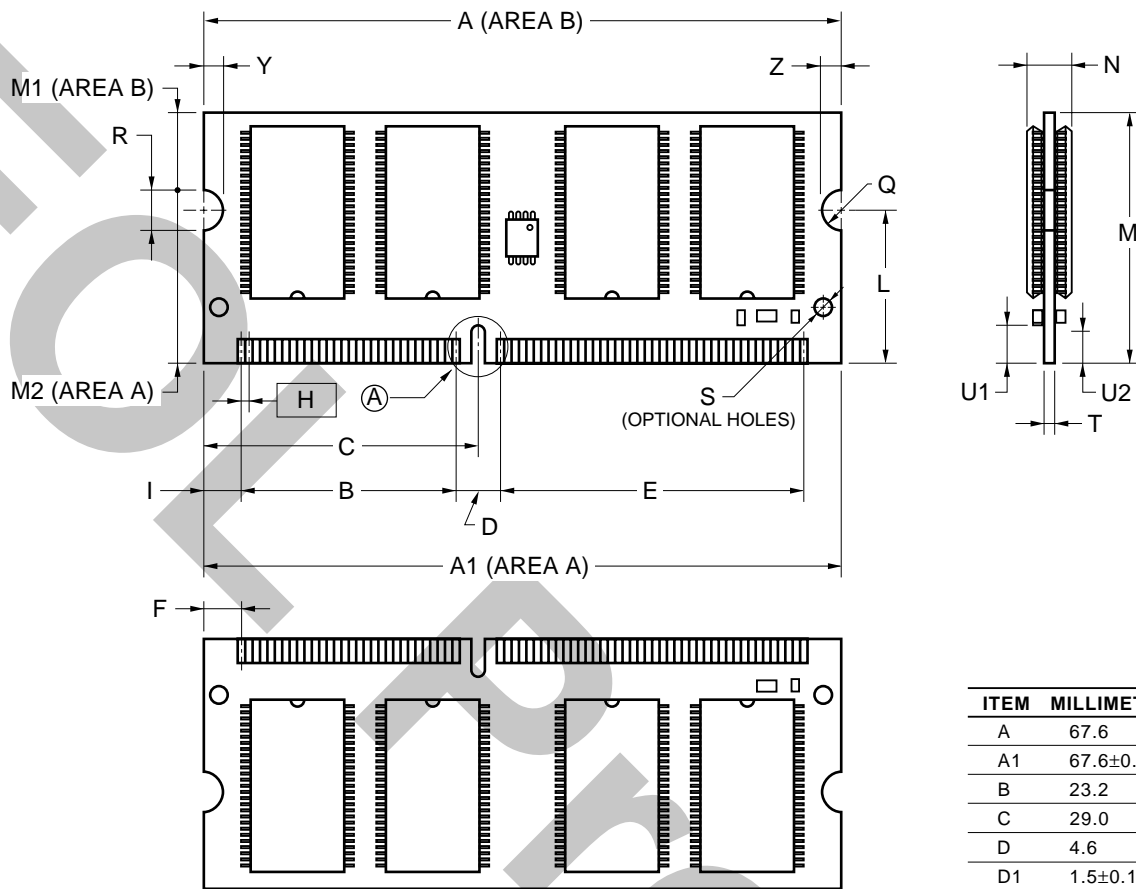
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes
32	Address and command signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Address and command signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
36	Prefetch read latency	-A75	04H	0	0	0	0	0	1	0	0	4 clocks
37	t <sub>PCD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
38	Number of segment addresses		02H	0	0	0	0	0	0	1	0	2 bits
39	Number of channels		04H	0	0	0	0	0	1	0	0	16
40	Depth of channels		07H	0	0	0	0	0	1	1	1	128 bits
41-61												
62	SPD revision		02H	0	0	0	0	0	0	1	0	2.0
63	Checksum for bytes 0 - 62	-A75	2BH	0	0	1	0	1	0	1	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

**Timing Charts**

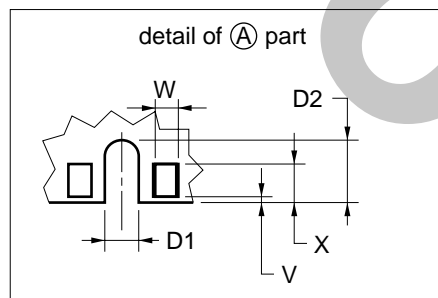
Please refer to the **μPD45V128421, 45V128821, 45V128161 Data sheet (E0025N)**.

Package Drawing

144-PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	67.6
A1	67.6±0.15
B	23.2
C	29.0
D	4.6
D1	1.5±0.10
D2	4.0
E	32.8
F	3.7
H	0.8 (T.P.)
I	3.3
L	20.0
M	31.75±0.15
M1	9.75
M2	22.0
N	3.8 MAX.
Q	R2.0
R	4.00±0.10
S	φ 1.8
T	1.0±0.1
U1	3.2 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	0.6±0.05
X	2.55 MIN.
Y	2.0 MIN.
Z	2.0 MIN.



**Revision History**

Edition / Date	Page		Description	
	This edition	Previous edition	Type of edition	Location
NEC Corporation (M15240E)				
1st edition / Dec.2000	-	-	-	-
Elpida Memory, Inc. (E0029N)				
1st edition / Jan. 2001	-	-	-	Republished by Elpida Memory, Inc.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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### CAUTION FOR HANDLING MEMORY MODULES

**When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.**

**When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.**

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