

16M-WORD BY 64-BIT

SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

#### Description

The MC-4516CD642XS is 16,777,216 words by 64 bits synchronous dynamic RAM module (Small Outline DIMM) on which 8 pieces of 128M SDRAM:  $\mu$ PD45128163 are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

#### Features

- 16,777,216 words by 64 bits organization
- Clock frequency and access time from CLK

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
MC-4516CD642XS-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6 ns
MC-4516CD642XS-A75L	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0, BA1 (Bank Select)
- Programmable burst-length: 1, 2, 4, 8 and Full Page
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single 3.3 V  $\pm$  0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

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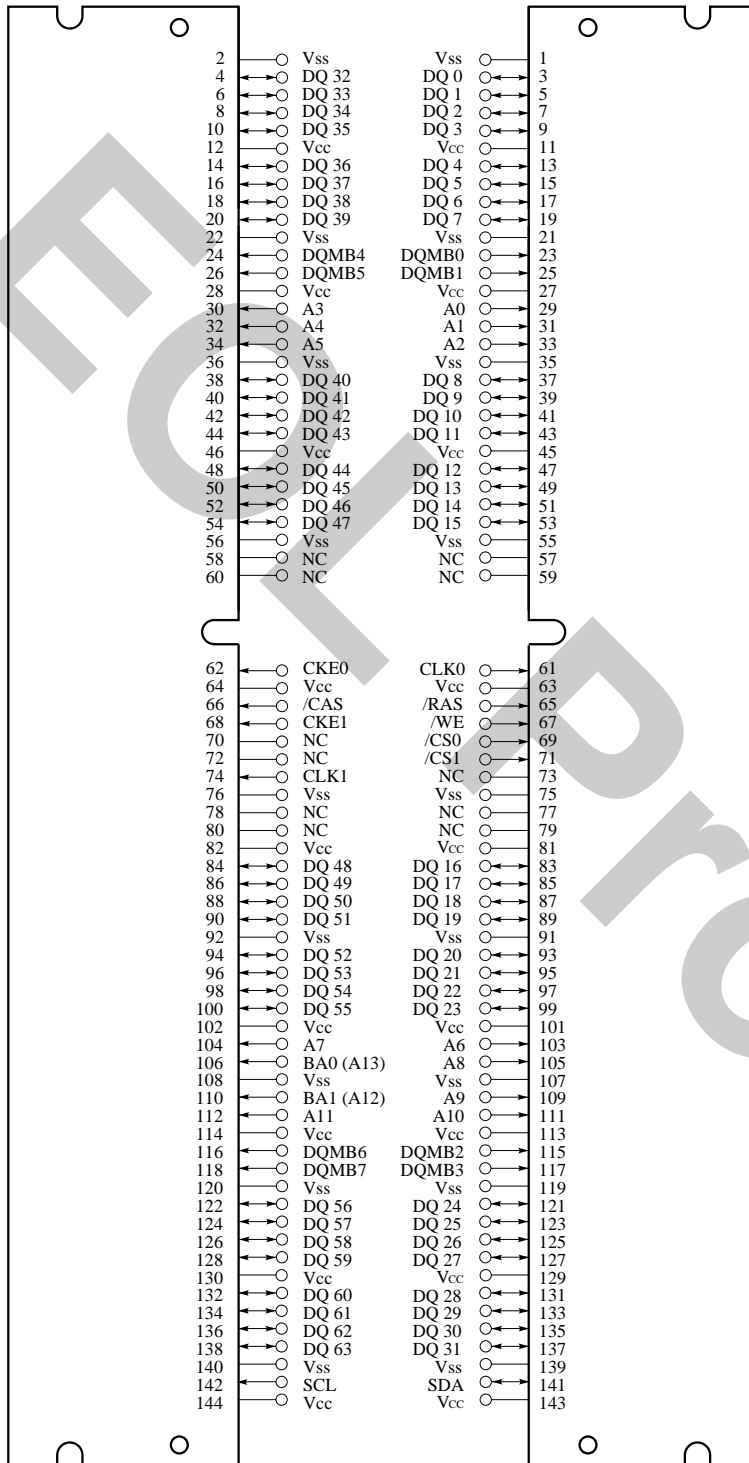
**Ordering Information**

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-4516CD642XS-A75	133 MHz	144-pin Small Outline DIMM (Socket Type)	8 pieces of $\mu$ PD45128163G5 (Rev. X) (10.16 mm (400) TSOP (II))
MC-4516CD642XS-A75L	133 MHz	Edge connector: Gold plated 31.75 mm height	

EOL Product

Pin Configuration

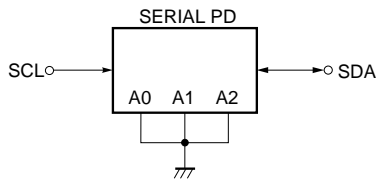
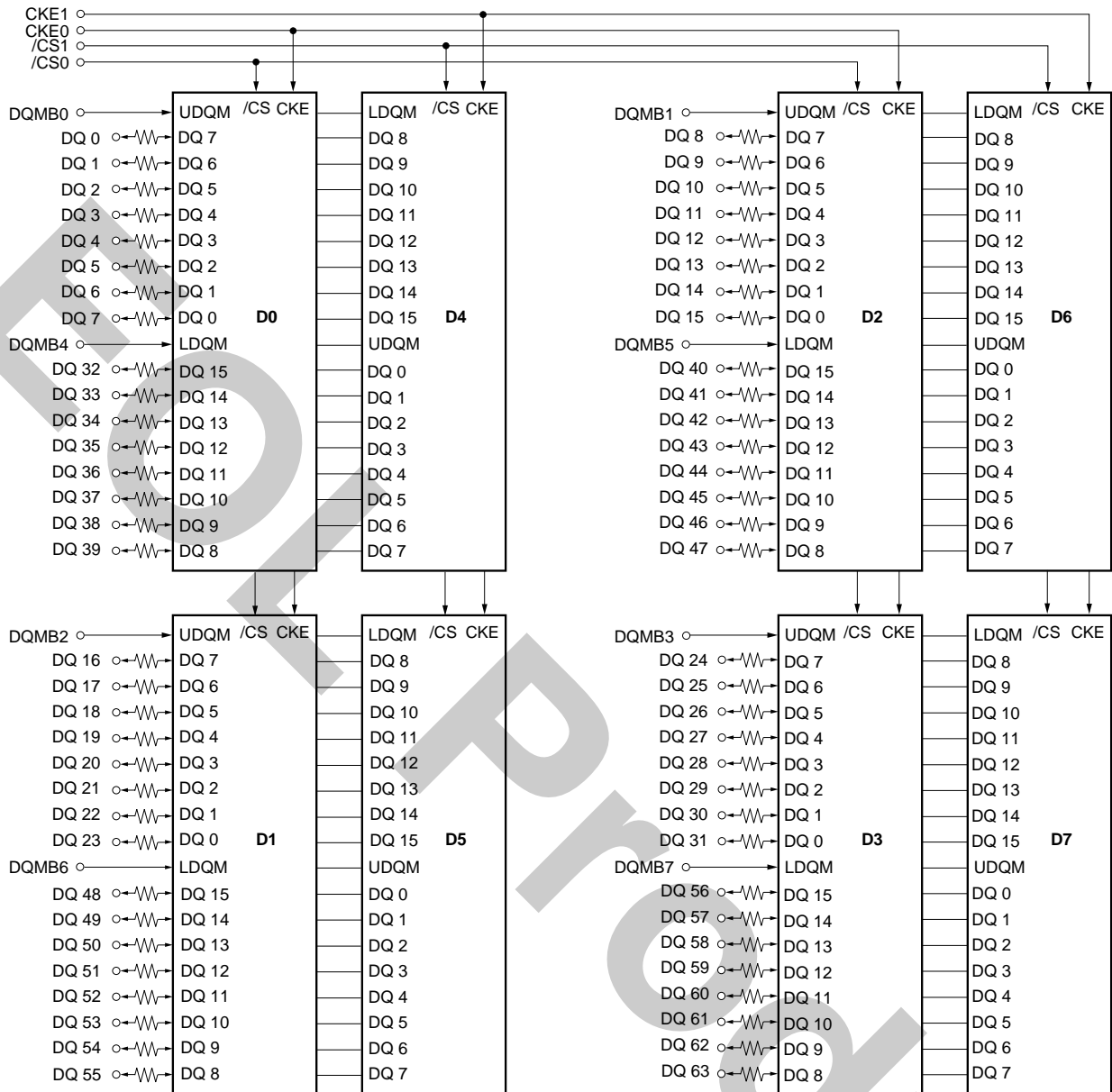
144-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

- A0 - A11 : Address Inputs  
[Row: A0 - A11, Column: A0 - A8]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0 - DQ63 : Data Inputs/Outputs
- CLK0, CLK1 : Clock Input
- CKE0, CKE1 : Clock Enable Input
- /CS0, /CS1 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- NC : No Connection

Block Diagram



A0 - A11 → A0 - A11 : D0 - D7  
 BA0 → A13 : D0 - D7  
 BA1 → A12 : D0 - D7

V<sub>CC</sub> → D0 - D7  
 V<sub>SS</sub> → D0 - D7  
 CLK0 → CLK : D0 - D3  
 CLK1 → CLK : D4 - D7  
 /RAS → /RAS : D0 - D7  
 /CAS → /CAS : D0 - D7  
 /WE → /WE : D0 - D7

**Remarks 1.** D0 - D7:  $\mu$ PD45128163 (2M words x 16 bits x 4 banks)

**2.** The value of all resistors is 10  $\Omega$ .

### Electrical Specifications

- All voltages are referenced to V<sub>SS</sub> (GND).
- After power up, wait more than 100  $\mu$ s and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V <sub>CC</sub>		-0.5 to +4.6	V
Voltage on input pin relative to GND	V <sub>T</sub>		-0.5 to +4.6	V
Short circuit output current	I <sub>O</sub>		50	mA
Power dissipation	P <sub>D</sub>		8	W
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

### Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I1</sub>	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	30		60	pF
	C <sub>I2</sub>	CLK0, CLK1	23		37	
	C <sub>I3</sub>	CKE0, CKE1	18		30	
	C <sub>I4</sub>	/CS0, /CS1	18		30	
	C <sub>I5</sub>	DQMB0 - DQMB7	7		14	
Data input/output capacitance	C <sub>I/O</sub>	DQ0 - DQ63	9		18	pF

## DC Characteristics (Recommended Operating Conditions unless otherwise noted)

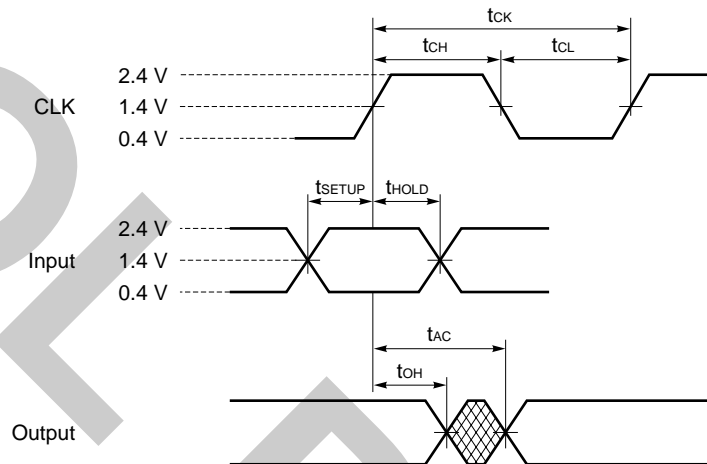
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I <sub>CC1</sub>	Burst length = 1, t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	/CAS latency = 2	560	mA	1
			/CAS latency = 3	580		
Precharge standby current in power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns		8	mA	
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞		8		
Precharge standby current in non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.		160	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.		64		
Active standby current in power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns		40	mA	
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞		32		
Active standby current in non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.		240	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.		160		
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK (MIN.)</sub> , I <sub>O</sub> = 0 mA	/CAS latency = 2	700	mA	2
			/CAS latency = 3	860		
CBR (Auto) refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	/CAS latency = 2	1,040	mA	3
			/CAS latency = 3	1,080		
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2 V	-**	16	mA	
			-**L	6.4		
Input leakage current	I <sub>I(L)</sub>	V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V	-8	+8	μA	
Output leakage current	I <sub>O(L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V	-3	+3	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -4.0 mA	2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +4.0 mA		0.4	V	

- Notes**
- I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

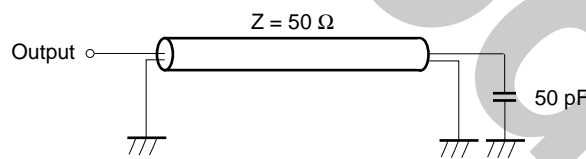
Parameter	Value	Unit
AC high level input voltage / low level input voltage	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Transition time (Input rise and fall time)	1	ns
Output timing measurement reference level	1.4	V



Synchronous Characteristics

Parameter		Symbol	-A75		Unit	Note
			MIN.	MAX.		
Clock cycle time	/CAS latency = 3	$t_{CK3}$	7.5	(133 MHz)	ns	
	/CAS latency = 2	$t_{CK2}$	10	(100 MHz)	ns	
Access time from CLK	/CAS latency = 3	$t_{AC3}$		5.4	ns	1
	/CAS latency = 2	$t_{AC2}$		6	ns	1
CLK high level width		$t_{CH}$	2.5		ns	
CLK low level width		$t_{CL}$	2.5		ns	
Data-out hold time	/CAS latency = 3	$t_{OH3}$	3		ns	1
	/CAS latency = 2	$t_{OH2}$	3		ns	1
Data-out low-impedance time		$t_{LZ}$	0		ns	
Data-out high-impedance time	/CAS latency = 3	$t_{HZ3}$	3	5.4	ns	
	/CAS latency = 2	$t_{HZ2}$	3	6	ns	
Data-in setup time		$t_{DS}$	1.5		ns	
Data-in hold time		$t_{DH}$	0.8		ns	
Address setup time		$t_{AS}$	1.5		ns	
Address hold time		$t_{AH}$	0.8		ns	
CKE setup time		$t_{CKS}$	1.5		ns	
CKE hold time		$t_{CKH}$	0.8		ns	
CKE setup time (Power down exit)		$t_{CKSP}$	1.5		ns	
Command (/CS0, /CS1, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		$t_{CMS}$	1.5		ns	
Command (/CS0, /CS1, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		$t_{CMH}$	0.8		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

## Asynchronous Characteristics

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
ACT to REF/ACT command period (Operation)	$t_{RC}$	67.5		ns	
REF to REF/ACT command period (Refresh)	$t_{RC1}$	67.5		ns	
ACT to PRE command period	$t_{RAS}$	45	120,000	ns	
PRE to ACT command period	$t_{RP}$	20		ns	
Delay time ACT to READ/WRITE command	$t_{RCD}$	20		ns	
ACT (one) to ACT (another) command period	$t_{RRD}$	15		ns	
Data-in to PRE command period	/CAS latency = 3	$t_{DPL3}$	8	ns	
	/CAS latency = 2	$t_{DPL2}$	8	ns	
Data-in to ACT (REF) command period (Auto precharge)	/CAS latency = 3	$t_{DAL3}$	1CLK+22.5	ns	1
	/CAS latency = 2	$t_{DAL2}$	1CLK+20	ns	
Mode register set cycle time	$t_{RSC}$	2		CLK	
Transition time	$t_T$	0.5	30	ns	
Refresh time (4,096 refresh cycles)	$t_{REF}$		64	ms	

**Note 1.** This device can satisfy the  $t_{DAL3}$  spec of 1CLK+20 ns for up to and including 125 MHz operation.

Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	09H	0	0	0	0	1	0	0	1	9 columns	
5	Number of banks	02H	0	0	0	0	0	0	1	0	2 bank	
6	Data width	40H	0	1	0	0	0	0	0	0	64 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	CL = 3 Access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type	00H	0	0	0	0	0	0	0	0	0	None
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	0	Normal
13	SDRAM width	10H	0	0	0	1	0	0	0	0	0	×16
14	Error checking SDRAM width	00H	0	0	0	0	0	0	0	0	0	None
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	0	4 banks
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	0	2, 3
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	0
21	SDRAM module attributes	00H	0	0	0	0	0	0	0	0	0	
22	SDRAM device attributes: General	0EH	0	0	0	0	1	1	1	1	0	
23	CL = 2 Cycle time	-A75	A0H	1	0	1	0	0	0	0	0	10 ns
24	CL = 2 Access time	-A75	60H	0	1	1	0	0	0	0	0	6 ns
25-26		00H	0	0	0	0	0	0	0	0	0	
27	t <sub>RP</sub> (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
28	t <sub>RRD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	t <sub>RCD</sub> (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
30	t <sub>RAS</sub> (MIN.)	-A75	2DH	0	0	1	0	1	1	0	0	45 ns
31	Module bank density	10H	0	0	0	1	0	0	0	0	0	64M bytes

(2/2)

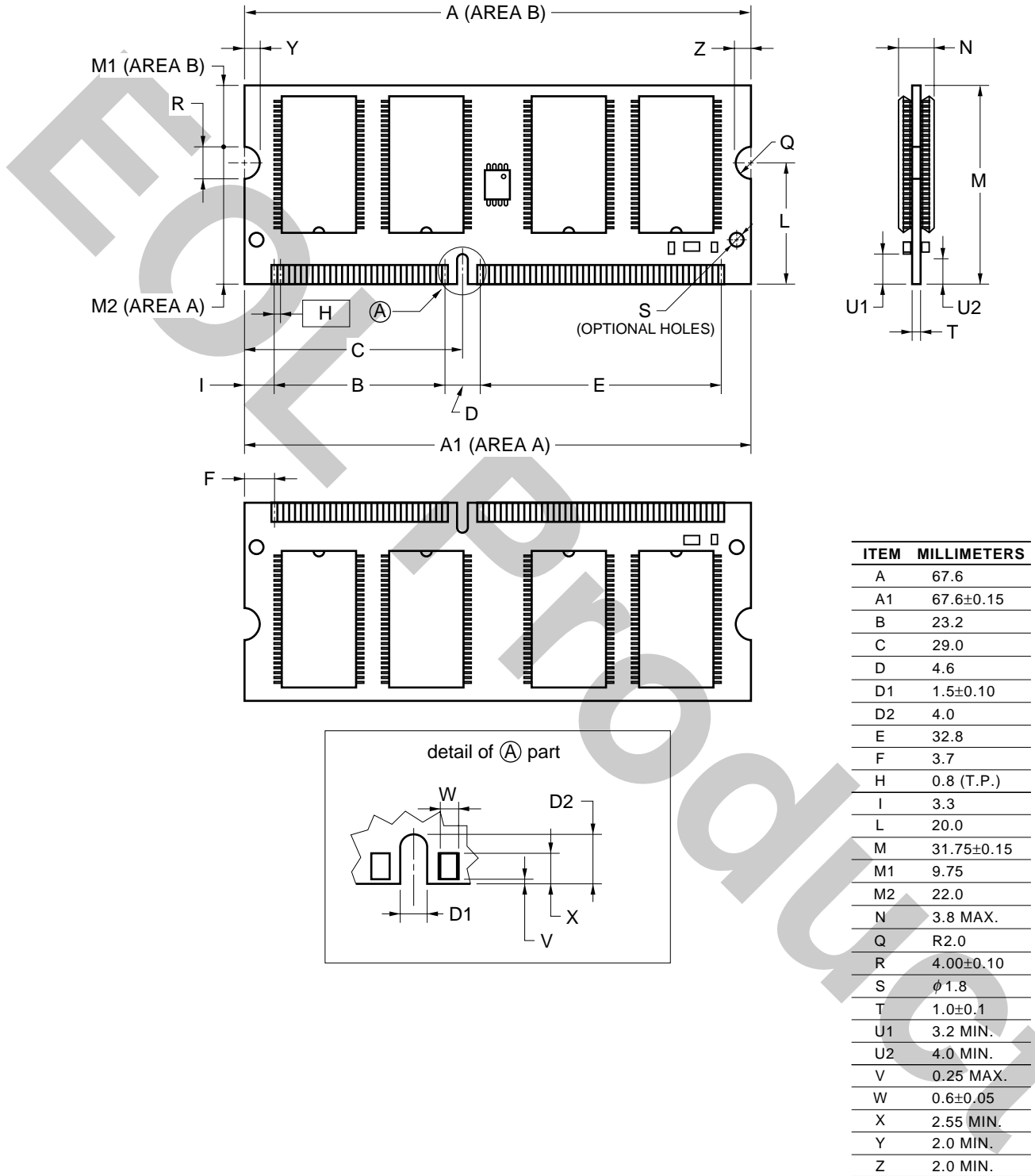
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
32	Command and address signal setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
36-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision	-A75	12H	0	0	0	1	0	0	1	0	1.2 A
63	Checksum for bytes 0 - 62	-A75	A7H	1	0	1	0	0	1	1	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	-A75	64H	0	1	1	0	0	1	0	0	
127	Intel specification /CAS latency support	-A75	C7H	1	1	0	0	0	1	1	1	

### Timing Chart

Refer to the [μPD45128441](#), [45128841](#), [45128163 Data sheet](#) (E0031N).

Package Drawing

144-PIN DUAL IN-LINE MODULE (SOCKET TYPE)



**CAUTION FOR HANDLING MEMORY MODULES**

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0107

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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