ELPIDA

DATA SHEET

256MB Unbuffered SDRAM DIMM

HB52F328EM-75B (32M words × 64 bits, 1 bank)
HB52F329EM-75B (32M words × 72 bits, 1 bank)

Description

The HB52F328EM and HB52F329EM belong to 8-byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 8-byte processor applications. They are synchronous Dynamic RAM Module, mounted 256M bits SDRAMs (HM5225805BTT) sealed in TSOP package, and 1 piece of serial EEPROM (2k bits) for Presence Detect (PD). The HB52F328EM is organized 32M × 64 × 1 bank mounted 8 pieces of 256M bits SDRAM. The HB52F329EM is organized 32M × 72 × 1 bank mounted 9 pieces of 256M bits SDRAM. Therefore, they make high density mounting possible without surface mount technology. They provide common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- Fully compatible with: JEDEC standard outline 8-byte DIMM
- 168-pin socket type package (dual lead out)
  - Outline: 133.37mm (Length) × 34.925mm (Height) × 4.00mm (Thickness)
  - Lead pitch: 1.27mm
- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Data bus width : × 64 Non parity (HB52F328EM)
  : × 72 ECC (HB52F329EM)
- Single pulsed /RAS
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8
- 2 variations of burst sequence
  - Sequential
  - Interleave
- Programmable /CE latency (CL) : 3 (133MHz)
  : 2 (100MHz)
- Byte control by DQMB
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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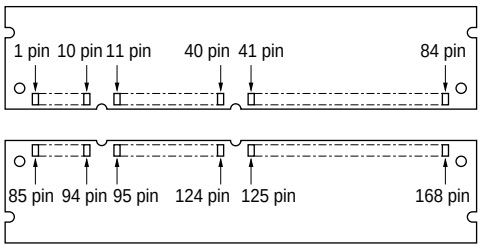
Ordering Information

Part number	Clock frequency MHz (max.)	/CE latency	Package	Contact pad
HB52F328EM-75B*	133	3	168-pin dual lead out socket type	Gold
HB52F329EM-75B*	133	3		

Note: 100MHz operation at /CE latency = 2.

Pin Configurations



[HB52F328EM]

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	NC	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	/W	69	DQ24	111	/CE	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	NC	156	DQ59
31	NC	73	VCC	115	/RE	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CK1	167	SA2
42	CK0	84	VCC	126	A12	168	VCC

[HB52F329EM]

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	NC	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
27	/W	69	DQ24	111	/CE	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	NC	156	DQ59
31	NC	73	VCC	115	/RE	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CK1	167	SA2
42	CK0	84	VCC	126	A12	168	VCC

Pin Description

[HB52F328EM]

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/S0, /S2	Chip select input
/RE	Row enable (/RAS) input
/CE	Column enable (/CAS) input
/W	Write enable input
DQMB0 to DQMB7	Byte data mask
CK0, CK2	Clock input
CKE0	Clock enable input
WP	Write protect for serial PD
SDA	Data input/output for serial PD
SCL	Clock input for serial PD
SA0 to SA2	Serial address input
VCC	Primary positive power supply
VSS	Ground
NC	No connection

[HB52F329EM]

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/S0, /S2	Chip select input
/RE	Row enable (/RAS) input
/CE	Column enable (/CAS) input
/W	Write enable input
DQMB0 to DQMB7	Byte data mask
CK0, CK2	Clock input
CKE0	Clock enable input
WP	Write protect for serial PD
SDA	Data input/output for serial PD
SCL	Clock input for serial PD
SA0 to SA2	Serial address input
VCC	Primary positive power supply
VSS	Ground
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	1	0D	13
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width (HB52F328EM)	0	1	0	0	0	0	0	0	40	64 bit
	(HB52F329EM)	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest /CE latency) 7.5ns	0	1	1	1	0	1	0	1	75	CL = 3
10	SDRAM access from Clock (highest /CE latency) 5.4ns	0	1	0	1	0	1	0	0	54	
11	Module configuration type (HB52F328EM)	0	0	0	0	0	0	0	0	00	Non parity
	(HB52F329EM)	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	Normal (7.8125 µs) Self refresh
13	SDRAM width	0	0	0	0	1	0	0	0	08	32M × 8
14	Error checking SDRAM width (HB52F328EM)	0	0	0	0	0	0	0	0	00	—
	(HB52F329EM)	0	0	0	0	1	0	0	0	08	× 8
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	0	0	0	0	1	1	1	1	0F	1, 2, 4, 8
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: /CE latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: /S latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: /W latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM device attributes	0	0	0	0	0	0	0	0	00	Non buffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	VCC ± 10%
23	SDRAM cycle time (2nd highest /CE latency) 10ns	1	0	1	0	0	0	0	0	A0	CL = 2
24	SDRAM access from Clock (2nd highest /CE latency) 6ns	0	1	1	0	0	0	0	0	60	
25	SDRAM cycle time (3rd highest /CE latency) Undefined	0	0	0	0	0	0	0	0	00	

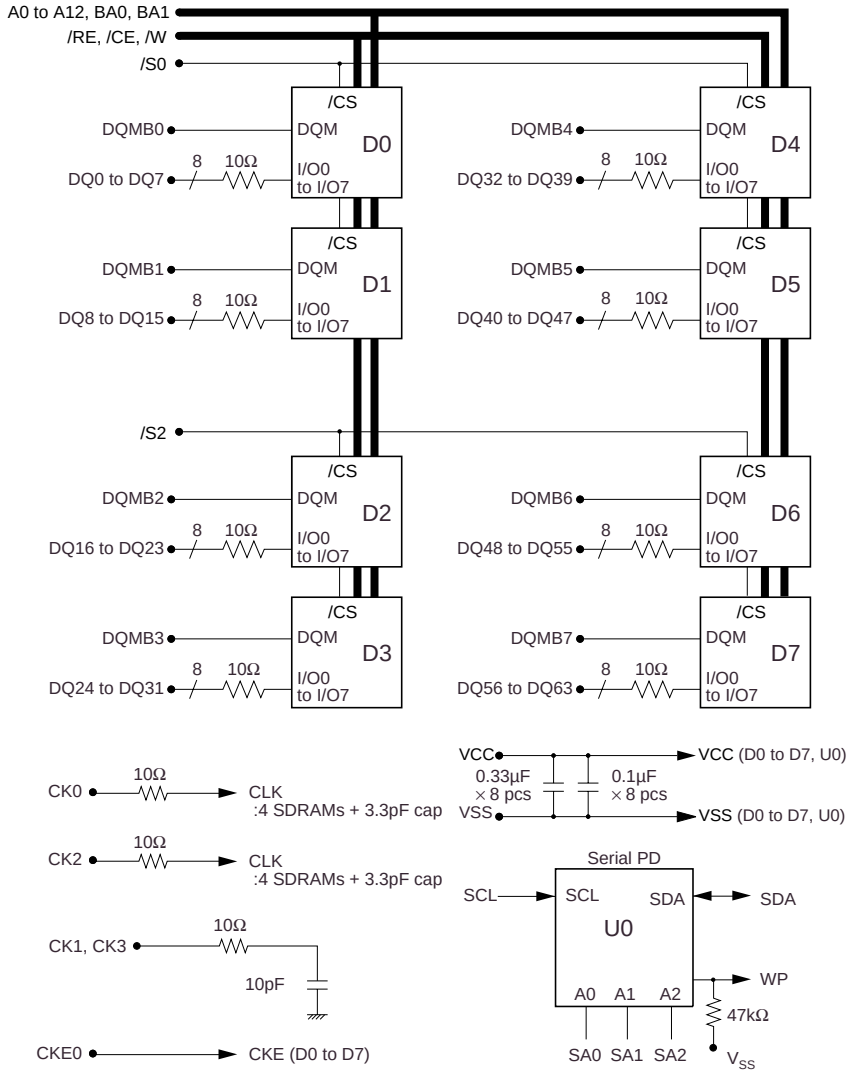
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
26	SDRAM access from Clock (3rd highest /CE latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20ns
28	Row active to row active min	0	0	0	0	1	1	1	1	0F	15ns
29	/RE to /CE delay min	0	0	0	1	0	1	0	0	14	20ns
30	Minimum /RE pulse width	0	0	1	0	1	1	0	1	2D	45ns
31	Density of each bank on module	0	1	0	0	0	0	0	0	40	1 bank 256M byte
32	Address and command signal input setup time	0	0	0	1	0	1	0	1	15	1.5ns
33	Address and command signal input hold time	0	0	0	0	1	0	0	0	08	0.8ns
34	Data signal input setup time	0	0	0	1	0	1	0	1	15	1.5ns
35	Data signal input hold time	0	0	0	0	1	0	0	0	08	0.8ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	0	0	0	1	0	02	JEDEC2
63	Checksum for bytes 0 to 62 (HB52F328EM))	0	1	0	0	0	0	1	0	42	66
	(HB52F329EM)	0	1	0	1	0	1	0	0	54	84
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	1	0	0	0	1	1	0	46	F
78	Manufacturer's part number	0	0	1	1	0	0	1	1	33	3
79	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
80	Manufacturer's part (HB52F328EM)	0	0	1	1	1	0	0	0	38	8
	(HB52F329EM)	0	0	1	1	1	0	0	1	39	9
81	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
82	Manufacturer's part number	0	1	0	0	1	1	0	1	4D	M
83	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
84	Manufacturer's part number	0	0	1	1	0	1	1	1	37	7
85	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
86	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
87	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Assembly serial number	*3									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*4
126	Reserved (Intel specification frequency)	0	1	1	0	0	1	0	0	64	
127	Reserved (Intel specification /CE# latency support)	1	0	1	0	1	1	1	1	AF	

Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High”.

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 125 are not defined (“1” or “0”).

Block Diagram (HB52F328EM)

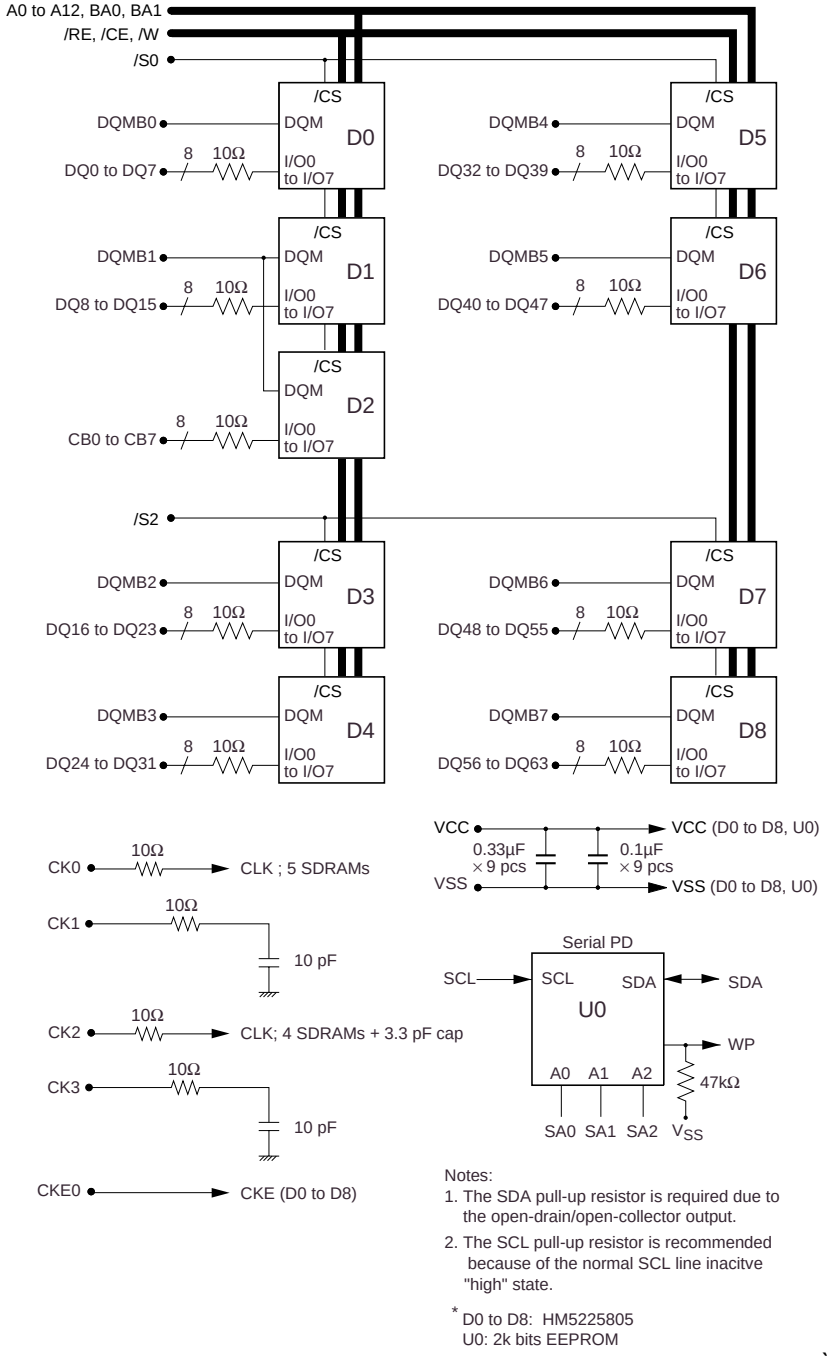


Notes :

1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D7: HM5225805
U0: 2k bits EEPROM

Block Diagram (HB52F329EM)



Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D8: HM5225805
U0: 2k bits EEPROM

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to VCC + 0.5 (≤ 4.6 (max.))	V	1
Supply voltage relative to VSS	VCC	–0.5 to +4.6	V	1
Short circuit output current	IOUT	50	mA	
Power dissipation (HB52F328EM)	PT	8.0	W	
Power dissipation (HB52F329EM)	PT	9.0	W	
Operating temperature	Topr	0 to +65	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. Respect to VSS.

DC Operating Conditions (TA = 0 to +65°C)

Parameter	Symbol	min.	max.	Unit	Note
Supply voltage	VCC	3.0	3.6	V	1, 2
	VSS	0	0	V	3
Input high voltage	VIH	2.0	VCC + 0.3	V	1, 4
Input low voltage	VIL	–0.3	0.8	V	1, 5

Notes: 1. All voltage referred to VSS
2. The supply voltage with all VCC pins must be on the same level.
3. The supply voltage with all VSS pins must be on the same level.
4. VIH (max.) = VCC + 2.0V for pulse width ≤ 3ns at VCC.
5. VIL (min.) = VSS − 2.0V for pulse width ≤ 3ns at VSS.

DC Characteristics (TA = 0 to 65°C, VCC = 3.3V ± 0.3V, VSS = 0V)

Parameter			HB52F328EM	HB52F329EM			
/CE latency	Symbol	Grade	max.	max.	Unit	Test condition	Notes
Operating current (CL = 2)	ICC1	PC100	880	990	mA	Burst length = 1 tRC = min.	1, 2, 3
(CL = 3)	ICC1	PC133	880	990	mA		
Standby current in power down	ICC2P		24	27	mA	CKE = VIL, tCK = 12ns	6
Standby current in power down (input signal stable)	ICC2PS		16	18	mA	CKE = VIL, tCK = ∞	7
Standby current in non power down	ICC2N		160	180	mA	CKE, /S = VIH, tCK = 12ns	4
Active standby current in power down	ICC3P		32	36	mA	CKE = VIL, tCK = 12ns	1, 2, 6
Active standby current in non power down	ICC3N		240	270	mA	CKE, /S = VIH, tCK = 12ns	1, 2, 4
Burst operating current (CL = 2)	ICC4	PC100	800	900	mA	tCK = min., BL = 4	1, 2, 5
(CL = 3)	ICC4	PC133	1080	1215	mA		
Refresh current	ICC5		1760	1980	mA	tRC = min.	3
Self refresh current	ICC6		24	27	mA	VIH ≥ VCC – 0.2 V VIL ≤ 0.2 V	8

Notes: 1. ICC depends on output load condition when the device is selected. ICC (max.) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK operating current.
7. After power down mode, no CK operating current.
8. After self refresh mode set, self refresh current.

DC Characteristics2 (TA = 0 to 65°C, VCC = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–10	10	µA	0 ≤ VIN ≤ VCC	
Output leakage current	ILO	–10	10	µA	0 ≤ VOUT ≤ VCC DQ = disable	
Output high voltage	VOH	2.4	—	V	IOH = –4mA	
Output low voltage	VOL	—	0.4	V	IOL = 4mA	

Pin Capacitance (TA = 25°C, VCC = 3.3V ± 0.3V) (HB52F328EM)

Parameter	Symbol	Pin	max.	Unit	Notes
Input capacitance	CI1	Address	70	pF	1, 2, 4
	CI2	/RE, /CE, /W	63	pF	1, 2, 4
	CI3	CKE	68	pF	1, 2, 4
	CI4	/S	34	pF	1, 2, 4
	CI5	CK	50	pF	1, 2, 4
	CI6	DQMB	16	pF	1, 2, 4
Input/Output capacitance	CI/O1	DQ	14	pF	1, 2, 3, 4

Pin Capacitance (TA = 25°C, VCC = 3.3V ± 0.3V) (HB52F329EM)

Parameter	Symbol	Pin	max.	Unit	Notes
Input capacitance	CI1	Address	72	pF	1, 2, 4
	CI2	/RE, /CE, /W	66	pF	1, 2, 4
	CI3	CKE	70	pF	1, 2, 4
	CI4	/S	39	pF	1, 2, 4
	CI5	CK	50	pF	1, 2, 4
	CI6	DQMB	21	pF	1, 2, 4
Input/Output capacitance	CI/O1	DQ	14	pF	1, 2, 3, 4

Notes: 1.Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. Measurement condition: f = 1MHz, 1.4Vbias, 200mV swing.
3. DQMB = VIH to disable Data-out.
4. This parameter is sampled and not 100% tested.

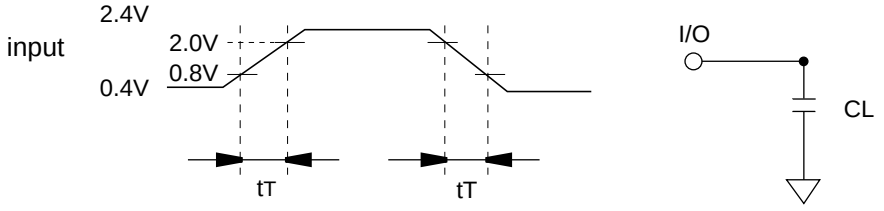
AC Characteristics (TA = 0 to 65°C,VCC = 3.3V ± 0.3V, VSS = 0V)

			PC133 CL = 3		PC100 CL = 2			
Parameter	Symbol	PC100 Symbol	min.	max.	min.	max.	Unit	Notes
System clock cycle time	tCK	Tclk	7.5	—	10	—	ns	1
CK high pulse width	tCKH	Tch	2.5	—	3	—	ns	1
CK low pulse width	tCKL	Tcl	2.5	—	3	—	ns	1
Access time from CK	tAC	Tac	—	5.4	—	6	ns	1, 2
Data-out hold time	tOH	Toh	2.7	—	3	—	ns	1, 2
CK to Data-out low impedance	tLZ		2	—	2	—	ns	1, 2, 3
CK to Data-out high impedance	tHZ		—	5.4	—	6	ns	1, 4
Data-in setup time	tDS	Tsi	1.5	—	2	—	ns	1
Data in hold time	tDH	Thi	0.8	—	1	—	ns	1
Address setup time	tAS	Tsi	1.5	—	2	—	ns	1
Address hold time	tAH	Thi	0.8	—	1	—	ns	1
CKE setup time	tCES	Tsi	1.5	—	2	—	ns	1, 5
CKE setup time for power down exit	tCESP	Tpde	1.5	—	2	—	ns	1
CKE hold time	tCEH	Thi	0.8	—	1	—	ns	1
Command setup time	tCS	Tsi	1.5	—	2	—	ns	1
Command hold time	tCH	Thi	0.8	—	1	—	ns	1
Ref/Active to Ref/Active command period	tRC	Trc	67.5	—	70	—	ns	1
Active to precharge command period	tRAS	Tras	45	120000	50	120000	ns	1
Active command to column command (same bank)	tRCD	Trcd	20	—	20	—	ns	1
Precharge to active command period	tRP	Trp	20	—	20	—	ns	1
Write recovery or data-in to precharge lead time	tDPL	Tdpl	15	—	20	—	ns	1
Active (a) to Active (b) command period	tRRD	Trrd	15	—	20	—	ns	1
Transition time (rise and fall)	tT		1	5	1	5	ns	
Refresh period	tREF		—	64	—	64	ms	

Notes: 1. AC measurement assumes tT = 1ns. Reference level for timing of input signals is 1.5V.
2. Access time is measured at 1.5V. Load condition is C_L = 50pF.
3. tLZ (min.) defines the time at which the outputs achieves the low impedance state.
4. tHZ (max.) defines the time at which the outputs achieves the high impedance state.
5. tCES defines CKE setup time to CK rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.5V
- Input waveform and output load: See following figures



Output load

Relationship Between Frequency and Minimum Latency

Parameter			CL = 3	CL = 2	
Frequency (MHz)			133	100	
tCK (ns)	Symbol	PC100 Symbol	7.5	10	Notes
Active command to column command (same bank)	IRCD		3	2	1
Active command to active command (same bank)	IRC		9	7	= [IRAS + IRP] 1
Active command to precharge command (same bank)	IRAS		6	5	1
Precharge command to active command (same bank)	IRP		3	2	1
Write recovery or data-in to precharge command (same bank)	IDPL	Tdpl	2	2	1
Active command to active command (different bank)	IRRD		2	2	1
Self refresh exit time	ISREX	Tsrx	1	1	2
Last data in to active command (Auto precharge, same bank)	IAPW	Tdal	5	4	= [IDPL + IRP]
Self refresh exit to command input	ISEC		9	7	= [IRC] 3
Precharge command to high impedance	IHZP	Troh	3	2	
Last data out to active command (Auto precharge, same bank)	IAPR		1	1	
Last data out to precharge (early precharge)	IEP		–2	–1	
Column command to column command	ICCD	Tccd	1	1	
Write command to data in latency	IWCD	Tdwd	0	0	
DQMB to data in	IDID	Tdqm	0	0	
DQMB to data out	IDOD	Tdqz	2	2	
CKE to CK disable	ICLE	Tcke	1	1	
Register set to active command	IRSA	Tmrd	1	1	
/S to command disable	ICDD		0	0	
Power down exit to command input	IPEC		1	1	

Notes: 1. IRCD to IRRD are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Pin Functions

CK0, CK2 (input pin): CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

/S0, /S2 (input pin): When /S is Low, the command input cycle becomes valid. When /S is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RE, /CE and /W (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9) is determined by A0 to A9 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0, BA1 (BA) is precharged.

BA0, BA1 (input pin): BA0, BA1 are bank select signal (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 is Low and BA0 is Low, bank 0 is selected. If BA1 is High and BA0 is Low, bank 1 is selected. If BA1 is Low and BA0 is High, bank 2 is selected. If BA1 is High and BA0 is High, bank 3 is selected.

CKE0 (input pin): This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63, CB0 to CB7 (input/output pins): Data is input to and output from these pins.

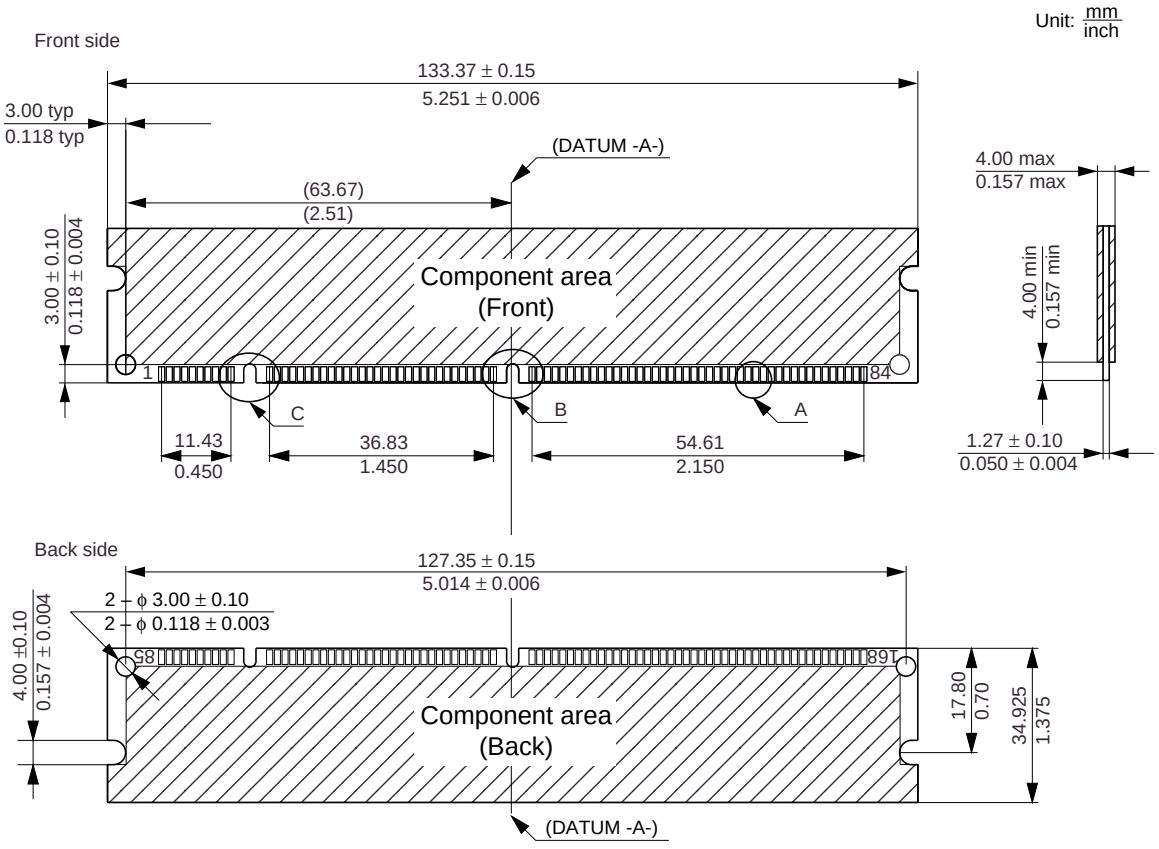
VCC (power supply pins): 3.3V is applied.

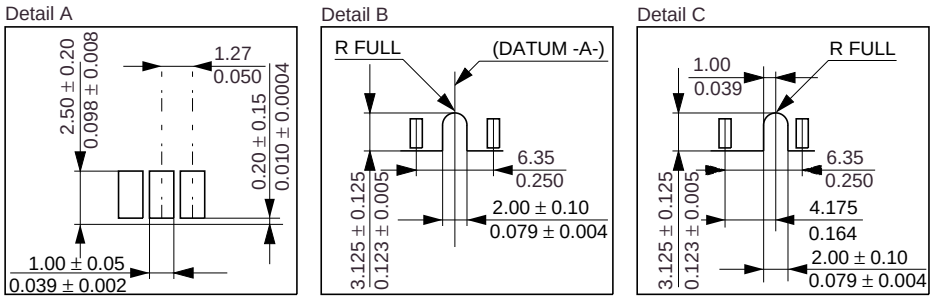
VSS (power supply pins): Ground is connected.

Detailed Operation Part

Refer to the HM5225165B/HM5225805B/HM5225405B-75/A6/B6 datasheet (E0082H).

Physical Outline





Note: Tolerance on all dimensions ± 0.15/0.006 unless otherwise specified.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.