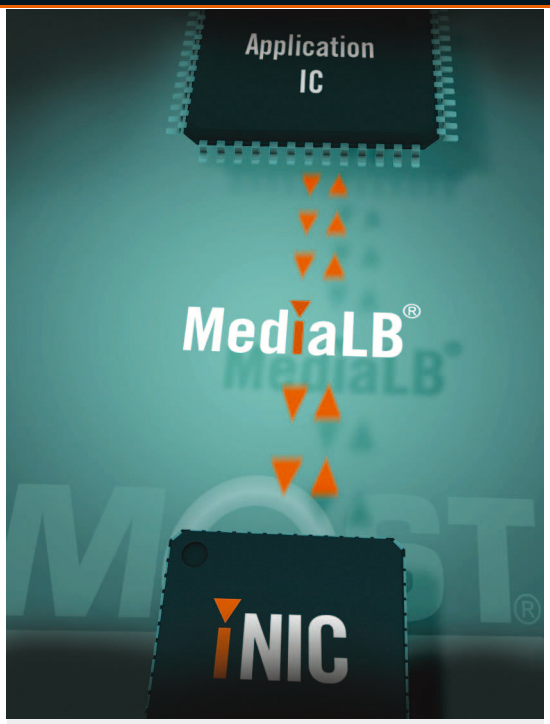
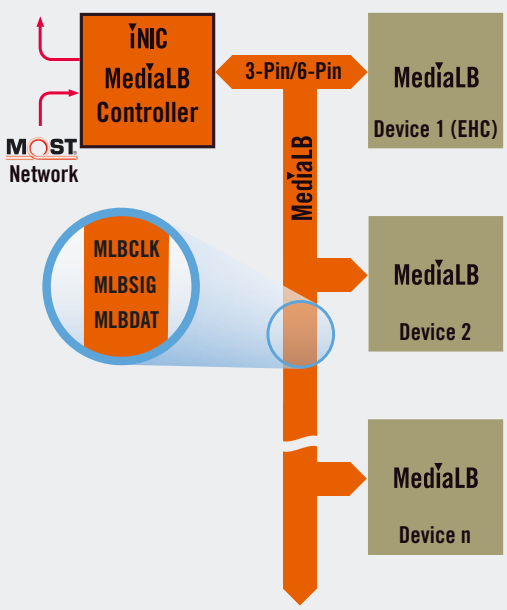
MediaLB

MediaLB® (Media Local Bus): The Standardized on-PCB, Inter-Chip Communication Bus for MOST Based Devices



Features

- Synchronous and serial on-PCB bus
- Synchronous to the MOST® network
- Local de-multiplexed version of MOST network data
- Supports all MOST network data types: control, asynchronous, synchronous and isochronous[1]
- Flexible and scalable implementation designed for all MOST network (MOST25/50/150) system configurations
- Supports a single-ended 3-Pin and a differential 6-Pin physical layer
- Speed modes for MediaLB 3-Pin:
  - 256Fs (12.3 Mbits/s[2])
  - 512Fs (24.6 Mbits/s[2])
  - 1024Fs (49.2 Mbits/s[2])
- Speed modes for MediaLB 6-Pin:
  - 2048Fs (89.1 Mbits/s[2])
  - 3072Fs (133.6 Mbits/s[2])
  - 4096Fs (179.7 Mbits/s[2])
  - 6144Fs (247.3 Mbits/s[2])
  - 8192Fs (330.2 Mbits/s[2])



Benefits

- Simplifies hardware and software application development of MOST network components
- Enhances reusability of hardware and software applications
- Established standard for accessing MOST
- MediaLB device interface implementation is available through a royalty-free SMSC license agreement
- Provides low-cost and low-pin count interface
- Data transfer from a single MediaLB controller to multiple MediaLB devices
- Supports inter-MediaLB device data transfer
- Full support in developing and testing MediaLB products with SMSC's IP and tool solutions

1. Supported on MOST150 networks
2. At 48 kHz

SMSC's MediaLB Support

MediaLB Training & Workshops

Several MediaLB Training modules are offered to provide the knowledge required to effectively use MediaLB tools:

- Information about hardware and software is taught according to the participants skill level - from "Overview" to "Expert" level.
- Customer-specific project support (i.e., implementing a MediaLB device interface) is provided in Workshops.

Joint preparation in advance of the training ensures maximum efficiency and benefit.

MediaLB Device Implementations

Different grades of MediaLB device implementations are available as VHDL™ source code to support your development:

- **MediaLB Device Core** implements the lower layers of the MediaLB interface. The device core performs serial to parallel and parallel to serial data transformation of MediaLB 3-Pin data.
- **MediaLB SRAM Interface** is a complete MediaLB device implementation for FPGAs. It is provided as VHDL source code to develop a MediaLB SRAM converter chip and to connect a standard application controller via an SRAM interface to MediaLB 3-Pin. The VHDL code is implemented and tested for a specific FPGA, but can be easily ported to other types of FPGAs.
- **MediaLB Device Interface Macro OS62420** represents Intellectual Property (IP) used to integrate a fully functional MediaLB device into a system-on-chip (SoC). The IP is provided as VHDL source code and supports MediaLB 3-Pin as well as MediaLB 6-Pin interfaces. It also features an Advanced Microcontroller Bus Architecture (AMBA®)-compliant user interface for integration into the system architecture.

MediaLB Tools

MediaLB tools enable analysis of data transfer on MediaLB interfaces and testing of MediaLB device implementations:

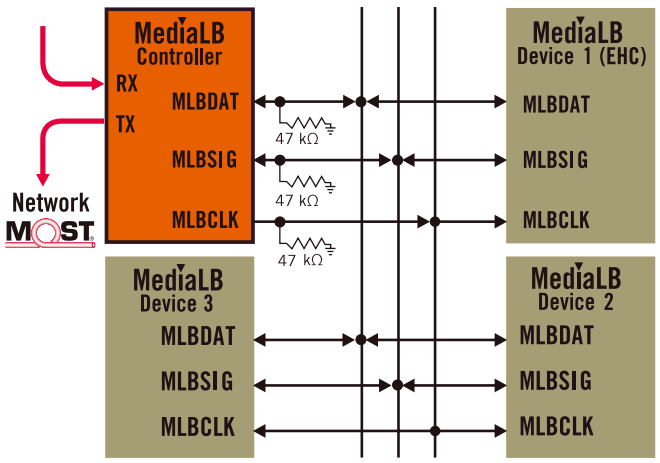
- **MediaLB Analyzer** is a combination of hardware and software components which allow observation and visualization of MediaLB data in a user-friendly manner. It consists of the MediaLB analysis software and a MediaLB Monitor. Several Active-Pods are available to support analysis of MediaLB 3-Pin and MediaLB 6-Pin data transfer. A Viewer depicts MediaLB data for analysis, and disassembled INIC Port Messages can be displayed since necessary syntax trees are included in the tool. This enables to focus on special events occurring on MediaLB.
- **MediaLB Interface Test Bench (MITB)** facilitates the testing of the physical and link layers of MediaLB 3-Pin interface implementations. The test bench incorporates hardware, firmware and a data checker software for testing control, asynchronous and synchronous data transport. Predefined tests are delivered to verify MediaLB interface implementations. A Graphical User Interface (GUI) is provided to display errors and to configure the generated test patterns. INIC Explorer and OSS Flasher are available to flash and configure the test bench.

MediaLB Operation

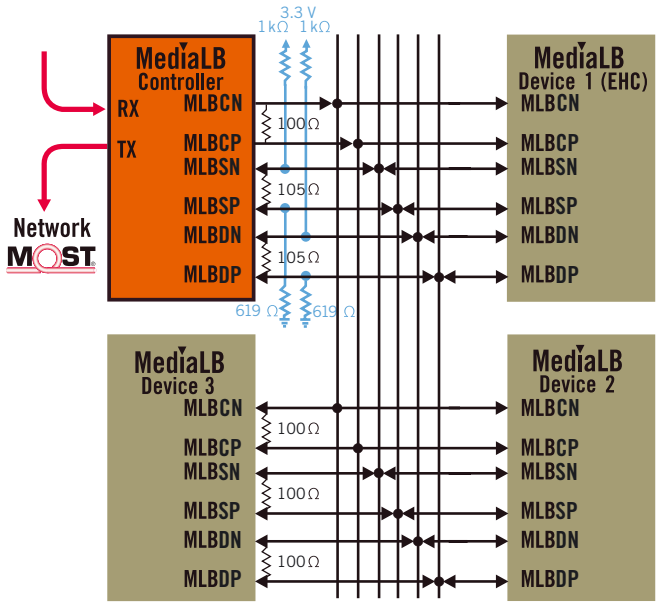
A MediaLB system consists of several MediaLB devices and one MediaLB controller (typically an INIC chip). The INIC serves as a transceiver for the MOST network and as a controller for MediaLB, which assures synchronization to the MOST network.

MediaLB Characteristics

- The MediaLB controller functions as the timing master and generates the clock signal and MediaLB frames
- MediaLB is synchronized to the MOST network
- MediaLB includes the definition of a single-ended 3-Pin and a differential 6-Pin physical layer interface
- MediaLB consists of the following signals:
  - MLBCLK - provides timing for the entire MediaLB system
  - MLBSIG - carries signaling information
  - MLBDAT - carries data
- MLBCLK supports multiple data rates:
  - MediaLB 3-Pin: 256Fs, 512Fs, 1024Fs
  - MediaLB 6-Pin: 2048Fs, 3072Fs, 4096Fs, 6144Fs, 8192Fs
- Frames are divided in 4 byte blocks (quadlets)
- The unique FRAMESYNC pattern transmitted by the MediaLB controller defines the frame boundary (between each MediaLB frame)



MediaLB 3-Pin Connection Diagram



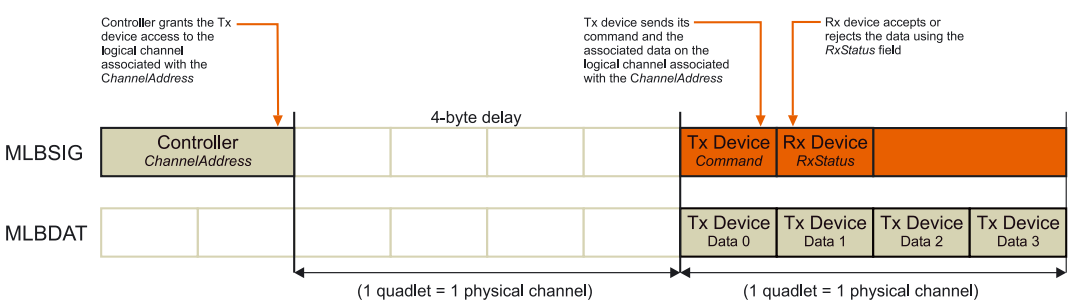
MediaLB 6-Pin Connection Diagram

Note: These drawings are abstracts from the MediaLB specification available at: www.smsc-ais.com/medialb.

MediaLB 3-Pin Data Structure

ChannelAddress: arbitrates bandwidth

Command: provides control information
RxStatus: used for hardware handshake and flow control
Data Quadlet: carries transferred data



Training & Workshops to Develop MediaLB on-PCB Communications

Training and Project Support

Modular training and customer-specific workshops provide the knowledge for your MediaLB projects.

During training, you learn how MediaLB works and how to use device implementations. Training is provided with lessons, presentations and hands-on sections. If you require specific project assistance, please advise your trainer.

MediaLB Training (1 Day)

MediaLB Training provides a comprehensive overview of all MediaLB hardware, communication mechanisms and protocols. Topics range from the MediaLB data and frame structure via the five types of logical channels to the configuration of ChannelAddresses. Different implementation options for MediaLB are explained.

Presentations and hands-on sections demonstrate the usage of the INIC Evaluation Platform, INIC Explorer and MediaLB Analyzer.

Locations

Training and workshop locations include:

- Karlsruhe, Germany
- Detroit, USA
- Göteborg, Sweden
- Yokohama, Japan

Training and workshops are available in German and English. Swedish and Japanese are available on request.

Your MediaLB Workshop

SMSC's workshops provide direct support for your MediaLB project. This can greatly shorten development time and help speed time-to-market for your products.

While the training modules have predefined content, workshops are setup as discussions with SMSC experts about design or debug issues.

To organize a workshop, SMSC recommends a single contact person from your company to handle all questions related to the workshop.

MediaLB workshop topics examples:

- Network interface hardware design and review
- MediaLB implementation
- MediaLB verification
- Video (e.g., MPEG and DTCP) data transport

Customized for Individual Needs

SMSC's workshop and training environment is designed to directly address your MediaLB project needs. The advantages of SMSC workshops include:

- Discussion with SMSC experts on customer-specific issues
- Expert review of customer-specific applications
- Maximum of six participants
- Detailed documentation provided, if required

Special preparation is needed to ensure the success of your workshop. Arrangements are made three months in advance of workshops. For details and scheduling, please contact us.

Typically duration is one to three days, according to your needs.

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MediaLB Device Core—(Complimentary)[1]

The MediaLB Device Core is a VHDL reference implementation for MediaLB 3-Pin, which can be easily integrated in an application-specific circuit or programmable logic device (representing the lowest level of the MediaLB interface[2]).

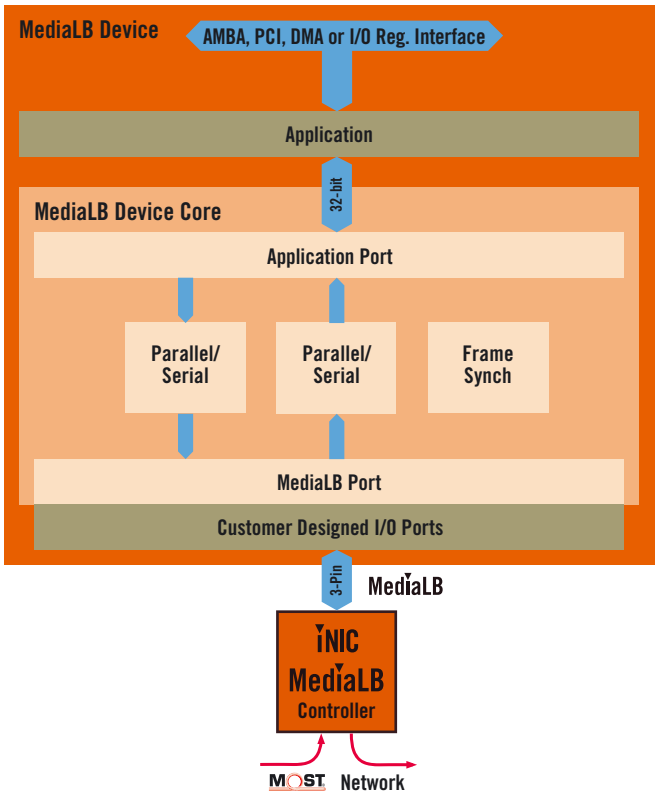
The MediaLB Device Core provides a MediaLB port for all MediaLB-relevant signals to access MediaLB data bytes and protocol information as well as signals required for controlling MediaLB Device Core functionality. The functionality of the application depends on the requirements of the device to be implemented. It can handle a single MediaLB ChannelAddress or multiple ChannelAddresses. It is also suitable for a single data type or all kinds of data types like control, asynchronous, synchronous and isochronous data.

The MediaLB application can work as an interface to various back-end interfaces e.g., AMBA, PCI, DMA or an I/O register interface.

In addition to the available VHDL source code of the core, a VHDL MediaLB host module is included. This module features an I/O interface, and can be used as a MediaLB controller and generic MediaLB pattern generator for device simulation and design verification.

Features

- Fully synchronous VHDL reference design
- Support for MediaLB 3-Pin interfaces
- Generic application interface for implementation of a variety of back-end applications
- Support for control, asynchronous, synchronous and isochronous data transfer
- core_frame_sync signal provision for user application synchronization
- Concurrent data transmission and reception
- Low gate-count
- Test bench for simulation included



Ordering Information

The MediaLB Device Core includes:

- VHDL source code
- VHDL test bench source code
- Scripts for Mentor Graphics® ModelSim® VHDL simulator
- MediaLB specification
- Manual
- Master license agreement

(Complimentary) Order No. B10168

1. Subject to license agreement
2. MediaLB Device Core implementation is up to the customer to meet application-related requirements.

Device Implementation: MediaLB SRAM Interface

MediaLB SRAM Interface

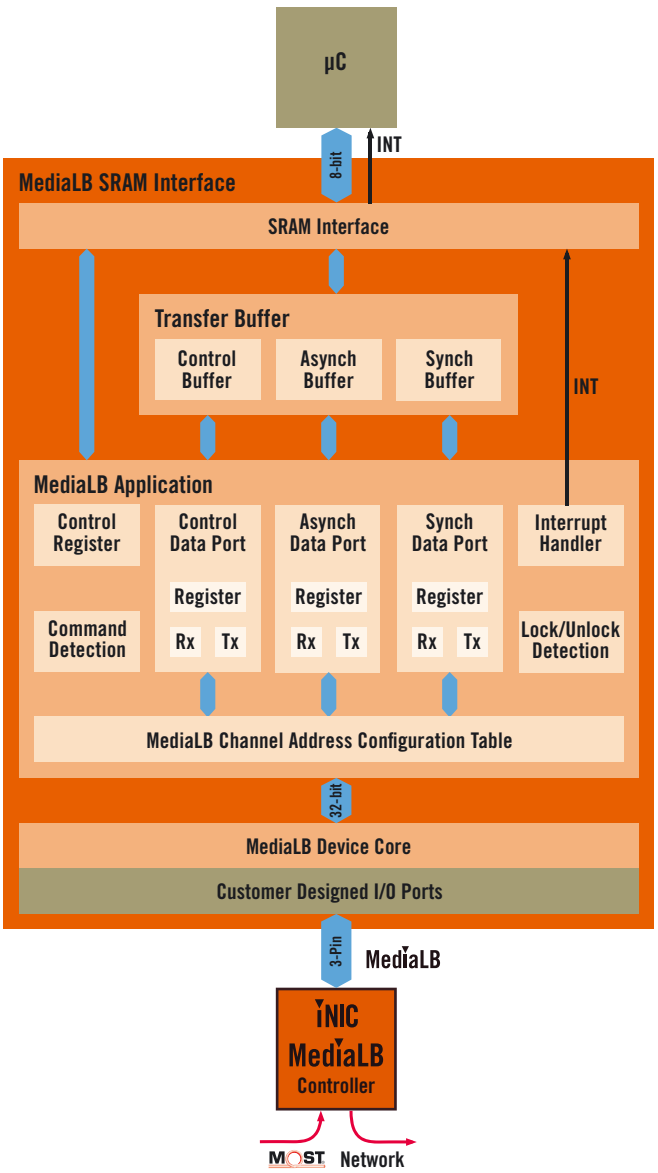
The MediaLB SRAM interface is a complete VHDL design for an FPGA[1]. It incorporates all state machines necessary for transferring control, asynchronous and synchronous data on MediaLB 3-Pin. It serves as an interface between the MediaLB port of an INIC and an 8-bit SRAM port of a standard microcontroller.

The MediaLB SRAM interface provides data ports for:

- Control data
- Asynchronous data
- Synchronous data

The transfer buffer for different data types is part of the design. By configuring control registers, the functionality of the interface can be defined. Control registers and data buffers are accessible via the SRAM interface port.

The design of the MediaLB SRAM interface is intended for implementation in a XILINX® Spartan® II XC2S200 FPGA. With adaptations, it can be easily ported to other types of FPGAs.



Features

- Implements MediaLB link layer requirements
- Supports MediaLB 3-Pin interfaces
- Selectable MediaLB clock rate: 256Fs or 512Fs
- Implements MediaLB lock detection
- 8-bit SRAM interface
- Supports control, asynchronous and synchronous data
- Supports single or double buffers for control and asynchronous Rx/Tx packet transfer
- Includes double buffers for synchronous Rx/Tx data transfer
- Adjustable sizes for all buffers
- Flexible interrupt rate for synchronous data transfer
- Supports Big-Endian and Little-Endian data format
- Provides hardware loop-back test mode

Ordering Information

The MediaLB SRAM CD-ROM includes:

- VHDL source code for the MediaLB SRAM interface
- VHDL source code for the simulation test bench including test patterns
- Scripts for Mentor Graphics ModelSim VHDL simulator
- Simulation templates
- MediaLB specification and manual
- Master license agreement

Order No. B10169

1. Subject to license agreement

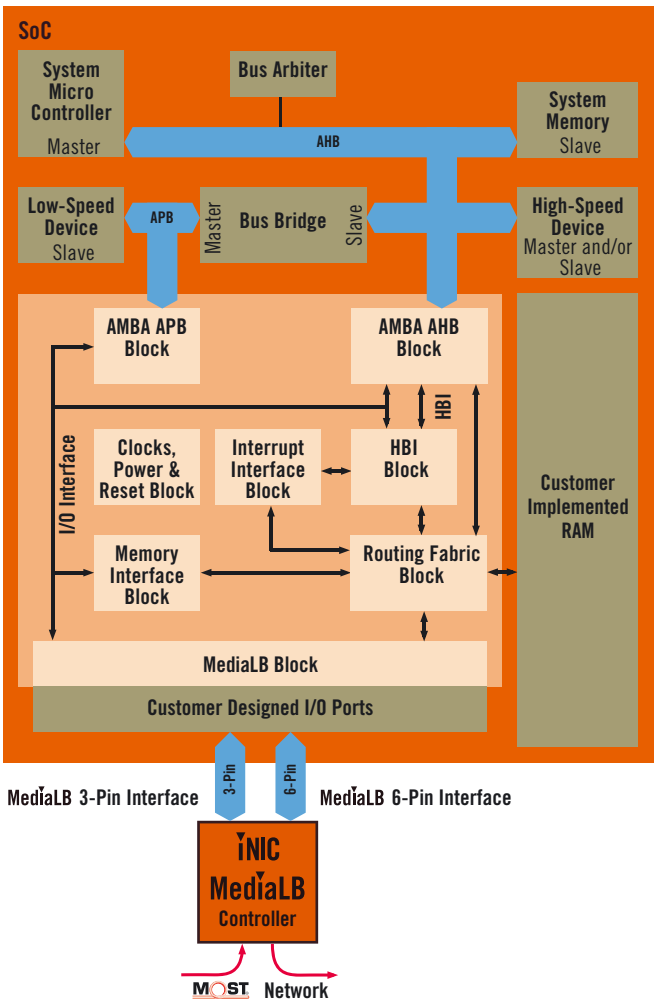
MediaLB Device Interface Macro OS62420

The MediaLB Device Interface Macro OS62420 is an IP provided as VHDL source code that implements the functionality of a MediaLB 3-Pin/6-Pin device. Its logic serves as an interface between MediaLB and a customer SoC.

The OS62420 can be configured to support either a MediaLB 3-Pin interface (single-ended) or a MediaLB 6-Pin interface (differential). The MediaLB interface is fully scalable with various speed modes to support a range of applications. Data rates range from 256Fs to 8192Fs (12.3 Mbits/s up to and including 330.2 Mbits/s at Fs = 48 kHz).

63 logical MediaLB channels are supported by the OS62420. These logical channels are software configurable and can be any combination of channel type (e.g., control, asynchronous, synchronous or isochronous) and direction (transmit or receive).

For seamless system integration, the OS62420 features an Advanced High-performance Bus (AHB™)-compliant, burst-capable DMA master interface and a slave Advanced Peripheral Bus (APB™) interface. The AHB interface is used for data transfer to/from the system memory and the APB interface provides the option to configure the IP. A customer implemented RAM is supported for channel data buffering.



Features

- MediaLB interface
  - Implements MediaLB Specification-compliant link layer requirements
  - Single-ended MediaLB 3-Pin interface (up to 1024Fs)
  - Differential MediaLB 6-Pin interface (up to 8192Fs)
  - Supports all MediaLB data types
  - Supports 63 logical channels, configurable for any channel type and direction
- AMBA high-performance bus
  - AMBA Specification Revision 2.0 AHB-compliant bus master interface for data transfer to/from system memory
  - Supports burst-capable DMA mode
  - 32-bit fixed data width
  - Supports customer implemented RAM used for channel data buffering
- AMBA peripheral bus
  - AMBA Specification Revision 2.0 APB-compliant slave interface for configuration
  - 32-bit fixed data width
  - 8-bit fixed address width

Ordering Information

The deliverables of the MediaLB Device Interface Macro depend upon the license agreement and include a subset of:

- VHDL source code for the MediaLB Device Interface Macro
- VHDL/Cadence® Incisive®-based test bench to simulate data flow
- Test plan and simulation suite
- Scripts to compile models, run tests and check results
- Synthesis reference script
- Data sheet

MediaLB Device Interface Macro OS62420 Order No. B10287

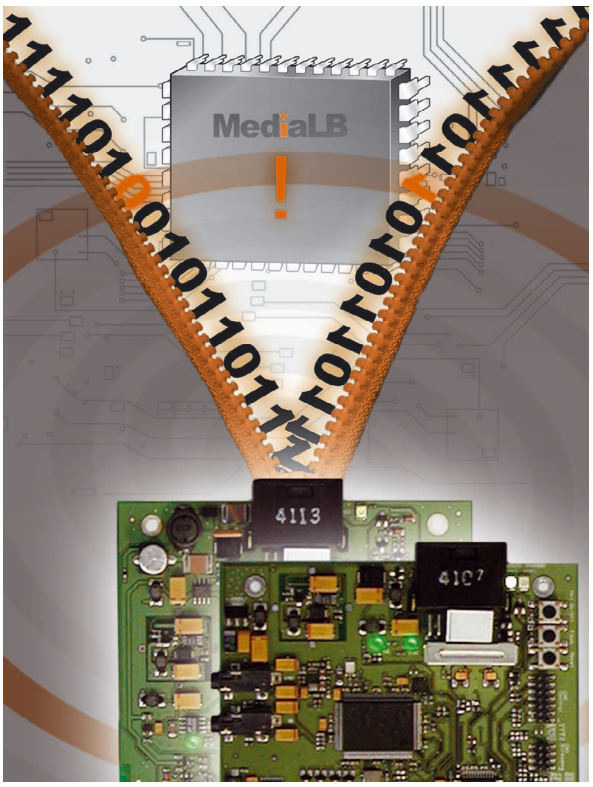
Tool: MediaLB Interface Testbench

MediaLB Interface Test Bench

The MediaLB Interface Test Bench (MITB) is a hardware test setup used for verification of both the physical layer of a MediaLB interface and the link layer implementation of a MediaLB device[1]. The test setup is based on the loop-back functionality of the MediaLB Device Under Test (DUT) and incorporates data checker software for test pattern generation and verification.

When performing a test, the MediaLB DUT must be connected via its MediaLB port to the test bench, which generates and transmits test patterns. These patterns are received on the MediaLB port of the DUT. To confirm correct data flow, the DUT performs a loop-back function, which allows the retransmission of the test patterns. The retransmitted patterns are received by the test bench and verified against the transmitted patterns.

The MediaLB Interface Test Bench provides a USB interface to the host PC. By means of the GUI, various test cases can be defined to verify different MediaLB port configurations according to the MediaLB interface mode, clock speed, channel allocation and transferred data type. Also, test results are displayed on the GUI.



Features

- Test setup for verification of the physical layer of a MediaLB interface
- Test setup for verification of the link layer implementation of a MediaLB device
- Supports MediaLB 3-Pin interfaces
- Supports 256Fs, 512Fs, and 1024Fs MediaLB clock rates
- Supports test pattern generation and verification of the following data types:
  - Control data
  - Asynchronous data
  - Synchronous data
  - Combinations of the above listed data types
- USB-compatible interface to the host PC
- GUI for test pattern configuration
- GUI for test status visualization
- Hardware error trigger outputs

1. Subject to license agreement

Testing MediaLB Interfaces

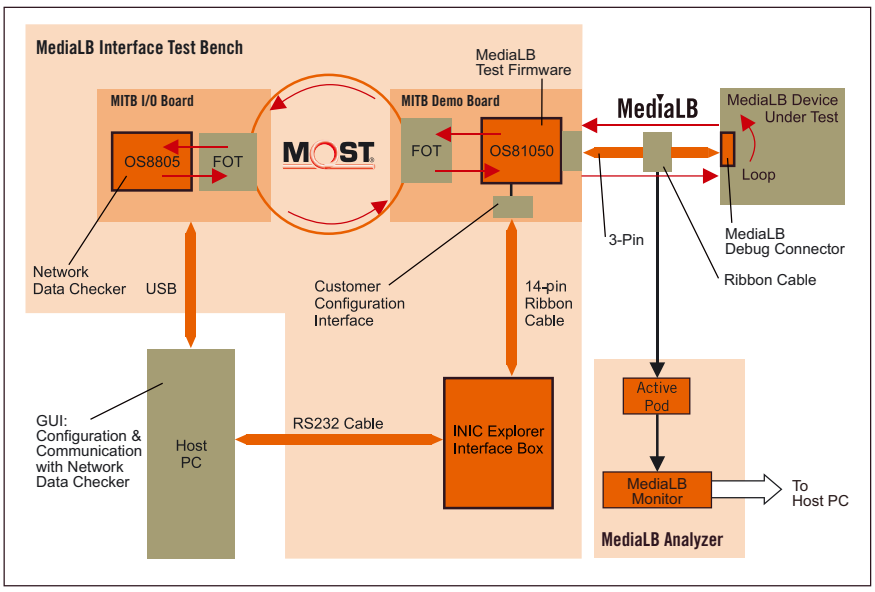
The MediaLB Interface Test Bench can be setup in two different ways[1].

MediaLB Device Setup

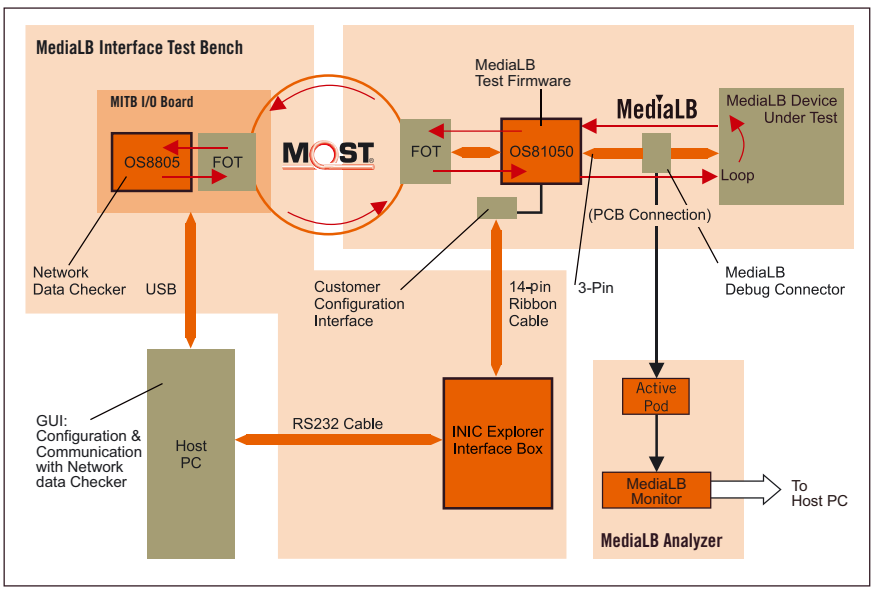
The MediaLB port of a MediaLB DUT is directly connected to the MediaLB port of the test bench. In most cases, fly-wires or ribbon cables are required to facilitate the connection.

MOST Device Setup

The MediaLB Interface Test Bench is connected to the MediaLB DUT via a MOST network connection. This requires that the DUT is part of a MOST device incorporating an OS81050 and an optical MOST interface. The DUT is connected to the OS81050 via MediaLB. In this case, the MediaLB connection is achieved on the PCB of the MOST device.



MediaLB Device Setup



MOST Device Setup

Ordering Information

The MediaLB Interface Test Bench includes:

- MITB I/O Board
- MITB Demo Board
- Plastic optical fiber set and USB connection cable
- MediaLB ribbon cable for MediaLB 3-Pin interface
- Software:
  - Network data checker GUI
    (Test pattern generator and checker)
  - Test firmware for different test cases
  - USB drivers
- Manuals

Note: A 12 V power supply is not included.

Order No. B10184

Additional Mandatory Products

To setup a complete MediaLB Interface Test Bench, the following products must be obtained:

- INIC Explorer and
- OSS Flasher (free download)

For details see last page.

Additional Recommended Products

To receive additional information on the DUT's MediaLB behavior:

- MediaLB Analyzer
- Oscilloscope

1. Subject to license agreement

Tool: MediaLB Analyzer

Features

- MediaLB analysis software
  - On and offline visualization of MediaLB RAW data
  - Composition of MediaLB RAW data to INIC Port Messages
  - Disassembly of INIC Port Messages
  - Integrated INIC Port Message syntax trees
  - Predefined and fully-customizable filter and trigger definitions provided
  - Storage of captured MediaLB data
  - Frame highlighting
  - Easy navigation with bookmarks and “go-to” actions
  - MediaLB lock detection
  - MediaLB speed detection
  - MediaLB frame and physical channel counter
  - MediaLB link layer protocol check
- MediaLB Monitor
  - Streaming-enabled USB 2.0 Hi-Speed interface
  - MediaLB clock activity, speed and lock detection
  - 256 MByte RAM for data buffering
  - Robust housing
- Active-Pod MediaLB 3-Pin LS and Active-Pod MediaLB 3-Pin HS
  - Support for MediaLB 3-Pin up to and including 1024Fs
  - Support for MediaLB 3-Pin low-speed debug header and MediaLB 3-Pin high-speed debug header
- Active-Pod MediaLB 6-Pin HS
  - Support for MediaLB 6-Pin up to and including 8192Fs
  - Support for MediaLB 6-Pin high-speed debug header

Ordering Information

The MediaLB Analyzer includes:

- MediaLB analysis software
- MediaLB Monitor
- Power supply
- Manuals

Order No. B10216

Note: This package does not include Active-Pods.
Mandatory: PC/laptop to install and run the MediaLB analysis software.

The MediaLB Monitor USB includes:

- MediaLB Monitor
- Power supply
- Manuals

Order No. B10288

Active-Pod MediaLB 3-Pin LS

Order No. B10297

Active-Pod MediaLB 3-Pin HS

Order No. B10293

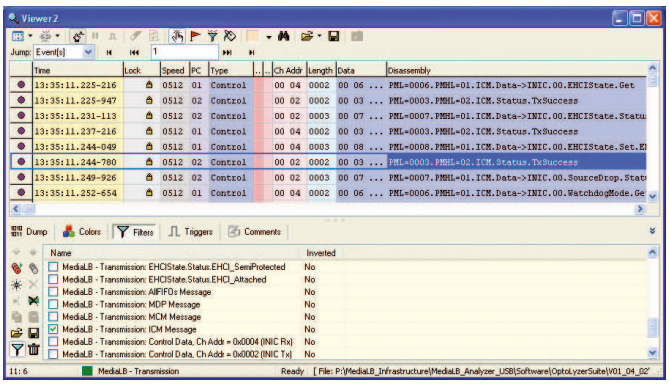
Active-Pod MediaLB 6-Pin HS

Order No. B10294

Description

The MediaLB Analyzer is a combination of hardware and software which allows observation and visualization of MediaLB data in a user-friendly manner[1]. It consists of three main modules:

- MediaLB analysis software—running on a HOST PC/ laptop and used to depict MediaLB data for analysis
- MediaLB Monitor hardware—used to format, process and buffer the incoming serial data before it is transferred via USB to the Host PC/laptop
- Active-Pod hardware—supports connection to the MediaLB interface on the DUT

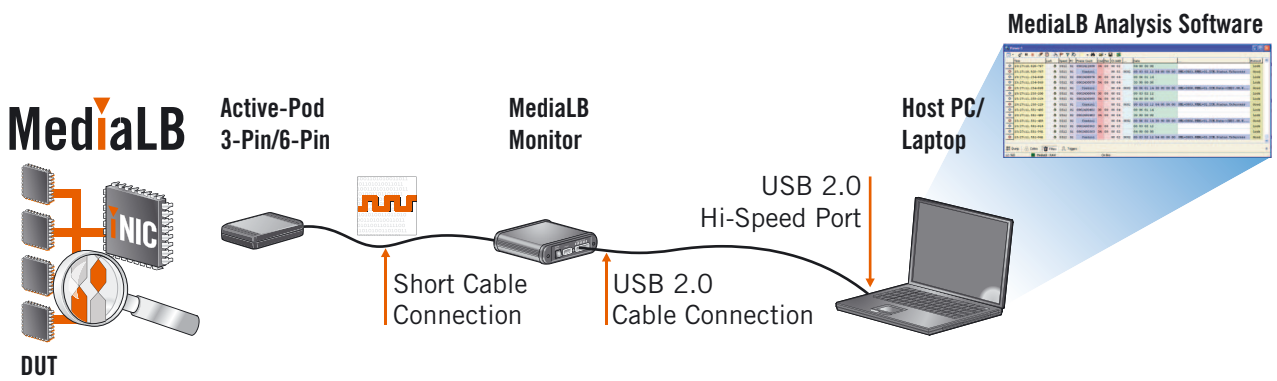


MediaLB Analysis Software: Viewer

MediaLB data analysis allows you to focus on special events occurring on the Media Local Bus. To capture these events, the MediaLB analysis software includes various filter and trigger capabilities. For the most common use cases, predefined filters and triggers help with starting the analysis. Customizable filters and triggers allow you to focus on each desired event.

A Viewer depicts the MediaLB data for analysis. Disassembled INIC Port Messages can be displayed since the MediaLB Analyzer includes the necessary syntax trees.

A detailed online help provides greater understanding of the capabilities of the MediaLB Analyzer and offers various examples on how to define filters and triggers.



System Requirements

- Intel® Pentium® IV Class PC supporting Hyper-Threading Technology (HTT) or a dual-core processor with 2.66 GHz
- 2 GByte RAM
- 1 GByte free disk space
- USB 2.0 Hi-Speed
- Microsoft® Windows® XP (SP2 or SP3) or Windows 2000 (SP4) operating system

1. Subject to license agreement

Tool: INIC Explorer and OSS Flasher for the MediaLB Interface Test

INIC Explorer

The INIC Explorer consists of software and a hardware interface box including power supply and connection cables[1]. This platform supports evaluating and debugging an INIC in a target platform.

For the MITB, the INIC Explorer Interface Box, in combination with the OSS Flasher software, is used for flashing the INIC chip part of the test bench. For flashing the INIC, the interface box needs to be connected to the customer configuration interface of the MITB. Through the USB cable, the INIC Explorer Interface Box must be connected to a host PC.

Ordering Information

The INIC Explorer includes:

- INIC Explorer Interface Box
- 12 V power supply
- USB to RS232 adapter cable
- 14-pin ribbon cable
- CD with INIC Explorer Software
- Manual

Order No. B10144

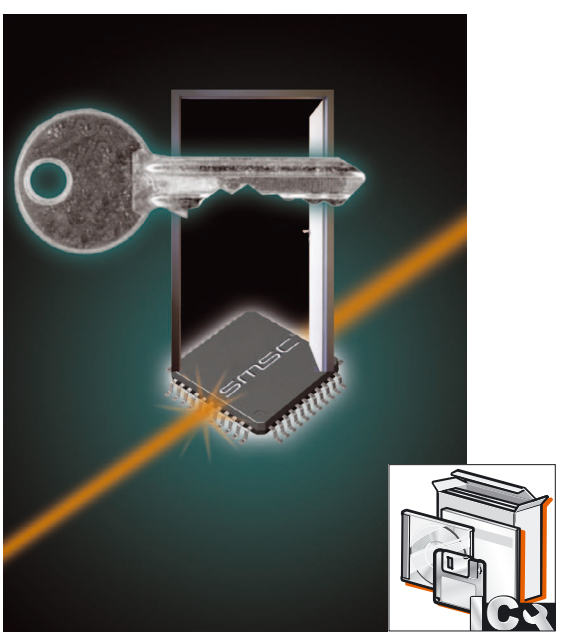
OSS Flasher

The OSS Flasher is a tool to update flash-based ICs[1].

With the MITB, the OSS Flasher is used to flash the MITB's INIC via the INIC Explorer Interface Box with the firmware for a certain test situation.

The OSS Flasher can be downloaded at no charge from the following SMSC link:

http://www.smsc-ais.com/ossflasher



1. Subject to license agreement

WEEE-Reg.-No. DE55114090

PFL_MediaLB_DevImpl_V01_00_XX-6.fm

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