**Product data sheet** 

## 1. Product profile

#### 1.1 General description

The BF1208 is a combination of two dual gate MOSFET amplifiers with shared source and gate2 leads and an integrated switch. The integrated switch is operated by the gate1 bias of amplifier B.

The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during Automatic Gain Control (AGC). Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT666 micro-miniature plastic package.

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

#### 1.2 Features and benefits

- Two low noise gain controlled amplifiers in a single package. One with a fully integrated bias and one with a partly integrated bias
- Internal switch to save external components
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio

#### 1.3 Applications

- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage
  - digital and analog television tuners
  - professional communication equipment



## **Dual N-channel dual gate MOSFET**

## 1.4 Quick reference data

**Table 1. Quick reference data**Per MOSFET unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage (DC)			-	-	6	V
I <sub>D</sub>	drain current (DC)			-	-	30	mA
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> ≤ 109 °C	[1]	-	-	180	mW
y <sub>fs</sub>	forward transfer admittance	f = 1 MHz					
		amplifier A; I <sub>D</sub> = 19 mA		26	31	41	mS
		amplifier B; I <sub>D</sub> = 13 mA		28	33	43	mS
C <sub>iss(G1)</sub>	input capacitance at gate1	f = 1 MHz					
		amplifier A		-	2.2	2.7	pF
		amplifier B		-	2.0	2.5	pF
C <sub>rss</sub>	reverse transfer capacitance	f = 1 MHz		-	20	-	fF
NF	noise figure	amplifier A; f = 400 MHz		-	1.3	1.9	dB
		amplifier B; f = 800 MHz		-	1.4	2.1	dB
Xmod	cross-modulation	input level for k = 1 % at 40 dB AGC					
		amplifier A		100	105	-	$dB\mu V$
		amplifier B		100	103	-	$dB\mu V$
Tj	junction temperature			-	-	150	°C

<sup>[1]</sup>  $T_{sp}$  is the temperature at the soldering point of the source lead.

# 2. Pinning information

Table 2. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate1 (AMP A)		
2	gate2	6 5 4	AMP A
3	gate1 (AMP B)		G1A DA
4	drain (AMP B)		
5	source	1 2 3	G2 + S
6	drain (AMP A)	1 2 3	G1B AMP B sym089

## **Dual N-channel dual gate MOSFET**

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BF1208	-	plastic surface mounted package; 6 leads	SOT666

# 4. Marking

Table 4. Marking codes

Type number	Marking code
BF1208	2L

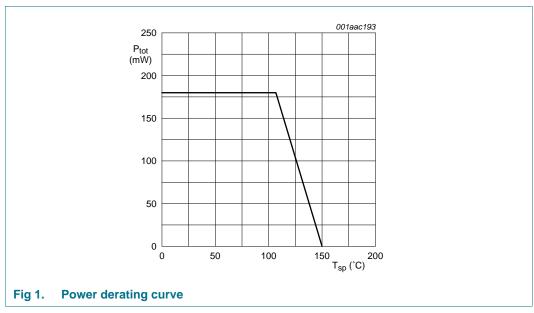
# 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per MOSFI	ET				
$V_{DS}$	drain-source voltage (DC)		-	6	V
$I_D$	drain current (DC)		-	30	mA
I <sub>G1</sub>	gate1 current		-	±10	mA
$I_{G2}$	gate2 current		-	±10	mA
P <sub>tot</sub>	total power dissipation	$T_{sp} \le 109  ^{\circ}C$	<u>[1]</u> _	180	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C

<sup>[1]</sup>  $T_{sp}$  is the temperature at the soldering point of the source lead.



## **Dual N-channel dual gate MOSFET**

## 6. Thermal characteristics

#### Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

# 7. Static characteristics

Table 7. Static characteristics

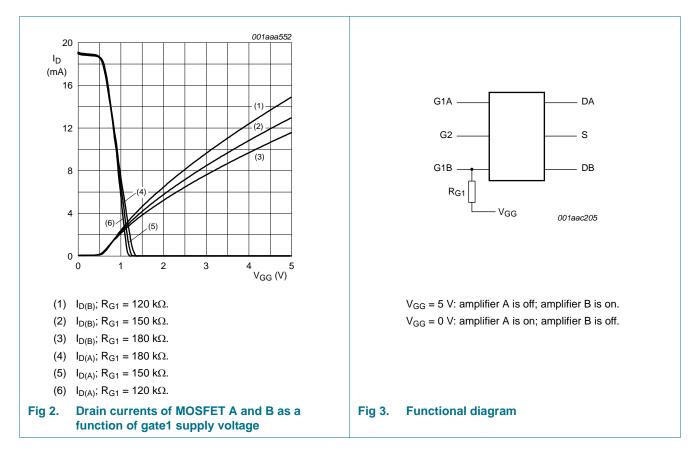
 $T_i = 25$  °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per MOSFE	T; unless otherwise specified						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0 \text{ V}; I_D = 10 \mu\text{A}$					
		amplifier A		6	-	-	V
		amplifier B		6	-	-	V
$V_{(BR)G1-SS}$	gate1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0 \text{ V}; I_{G1-S} = 10 \text{ mA}$		6	-	10	V
$V_{(BR)G2-SS}$	gate2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0 \text{ V}; I_{G2-S} = 10 \text{ mA}$		6	-	10	V
$V_{F(S-G1)}$	forward source-gate1 voltage	$V_{G2-S} = V_{DS} = 0 \text{ V}; I_{S-G1} = 10 \text{ mA}$		0.5	-	1.5	V
$V_{F(S-G2)}$	forward source-gate2 voltage	$V_{G1-S} = V_{DS} = 0 \text{ V}; I_{S-G2} = 10 \text{ mA}$		0.5	-	1.5	V
$V_{G1-S(th)}$	gate1-source threshold voltage	$V_{DS} = 5 \text{ V}; V_{G2-S} = 4 \text{ V}; I_D = 100 \mu\text{A}$		0.3	-	1.0	V
$V_{G2-S(th)}$	gate2-source threshold voltage	$V_{DS} = 5 \text{ V}; V_{G1-S} = 5 \text{ V}; I_D = 100 \mu\text{A}$		0.4	-	1.0	V
I <sub>DSX</sub>	drain-source current	$V_{G2-S} = 4 \text{ V}; V_{DS(B)} = 5 \text{ V}; R_{G1} = 150 \text{ k}\Omega$					
		amplifier A; V <sub>DS(A)</sub> = 5 V	[1]	14	-	24	mΑ
		amplifier B; V <sub>DS(B)</sub> = 5 V	[2]	9	-	17	mΑ
I <sub>G1-S</sub>	gate1 cut-off current	$V_{G2-S} = V_{DS(A)} = 0 V$					
		amplifier A; $V_{G1-S(A)} = 5 \text{ V}$ ; $I_{D(B)} = 0 \text{ A}$		-	-	50	nA
		amplifier B; $V_{G1-S(B)} = 5 \text{ V}$ ; $V_{DS(B)} = 0 \text{ V}$		-	-	50	nA
I <sub>G2-S</sub>	gate2 cut-off current	$V_{G2-S} = 4 \text{ V}; V_{G1-S(B)} = 0 \text{ V};$ $V_{G1-S(A)} = V_{DS(A)} = V_{DS(B)} = 0 \text{ V}$		-	-	20	nA

<sup>[1]</sup>  $R_{G1}$  connects gate1 (B) to  $V_{GG} = 0$  V (see Figure 3).

<sup>[2]</sup>  $R_{G1}$  connects gate1 (B) to  $V_{GG} = 5 \text{ V}$  (see Figure 3).

## **Dual N-channel dual gate MOSFET**



# 8. Dynamic characteristics

## 8.1 Dynamic characteristics for amplifier A

Table 8. Dynamic characteristics for amplifier A[1]

Common source;  $T_{amb} = 25$  °C;  $V_{G2-S} = 4$  V;  $V_{DS} = 5$  V;  $I_D = 19$  mA; unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Unit
forward transfer admittance	T <sub>j</sub> = 25 °C	26	31	41	mS
input capacitance at gate1	f = 1 MHz	-	2.2	2.7	pF
input capacitance at gate2	f = 1 MHz	-	3.0	-	pF
output capacitance	f = 1 MHz	-	0.9	-	pF
reverse transfer capacitance	f = 1 MHz	-	20	-	fF
power gain	$B_S = B_{S(opt)}; B_L = B_{L(opt)}$				
	$f = 200 \text{ MHz}; G_S = 2 \text{ mS}; G_L = 0.5 \text{ mS}$	32	36	40	dB
	$f = 400 \text{ MHz}; G_S = 2 \text{ mS}; G_L = 1 \text{ mS}$	28	32	36	dB
	$f = 800 \text{ MHz}; G_S = 3.3 \text{ mS}; G_L = 1 \text{ mS}$	23	27	32	dB
noise figure	$f = 11 \text{ MHz}; G_S = 20 \text{ mS}; B_S = 0 \text{ S}$	-	3.0	-	dB
	$f = 400 \text{ MHz}; Y_S = Y_{S(opt)}$	-	1.3	1.9	dB
	$f = 800 \text{ MHz}; Y_S = Y_{S(opt)}$	-	1.4	2.1	dB
	forward transfer admittance input capacitance at gate1 input capacitance at gate2 output capacitance reverse transfer capacitance power gain	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$

#### **Dual N-channel dual gate MOSFET**

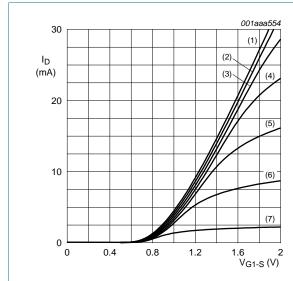
Table 8. Dynamic characteristics for amplifier A[1] ...continued

Common source;  $T_{amb} = 25$  °C;  $V_{G2-S} = 4$  V;  $V_{DS} = 5$  V;  $I_D = 19$  mA; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
	cross-modulation	input level for $k = 1 \%$ ; $f_w = 50 \text{ MHz}$ ; $f_{unw} = 60 \text{ MHz}$	[2]				
		at 0 dB AGC		90	-	-	$dB\mu V$
		at 10 dB AGC		-	90	-	$dB\mu V$
		at 20 dB AGC		-	99	-	$dB\mu V$
	at 40 dB AGC		100	105	-	$dB\mu V$	

- [1] For the MOSFET not in use:  $V_{G1-S(B)} = 0 \text{ V}$ ;  $V_{DS(B)} = 0 \text{ V}$ .
- [2] Measured in Figure 33 test circuit.

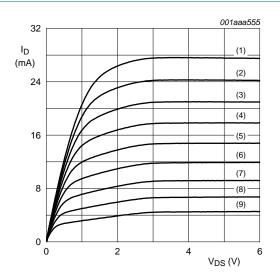
## 8.1.1 Graphics for amplifier A



- (1)  $V_{G2-S} = 4 \text{ V}$ .
- (2)  $V_{G2-S} = 3.5 \text{ V}.$
- (3)  $V_{G2-S} = 3 \text{ V}.$
- (4)  $V_{G2-S} = 2.5 \text{ V}.$
- (5)  $V_{G2-S} = 2 \text{ V}.$
- (6)  $V_{G2-S} = 1.5 \text{ V}.$
- (7)  $V_{G2-S} = 1 \text{ V}.$

 $V_{DS(A)} = 5 \text{ V}; V_{G1-S(B)} = V_{DS(B)} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}.$ 

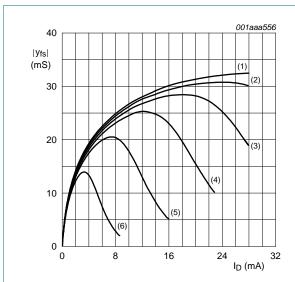




- (1)  $V_{G1-S(A)} = 1.8 \text{ V}.$
- (2)  $V_{G1-S(A)} = 1.7 \text{ V}.$
- (3)  $V_{G1-S(A)} = 1.6 \text{ V}.$
- (4)  $V_{G1-S(A)} = 1.5 \text{ V}.$
- (5)  $V_{G1-S(A)} = 1.4 \text{ V}.$
- (6)  $V_{G1-S(A)} = 1.3 \text{ V}.$
- (7)  $V_{G1-S(A)} = 1.2 \text{ V}.$ (8)  $V_{G1-S(A)} = 1.1 \text{ V}.$
- (9)  $V_{G1-S(A)} = 1 \text{ V}.$ 
  - $V_{G2-S} = 4 \text{ V}; V_{G1-S(B)} = V_{DS(B)} = 0 \text{ V}; T_j = 25 \text{ °C}.$

Fig 5. Amplifier A: output characteristics; typical values

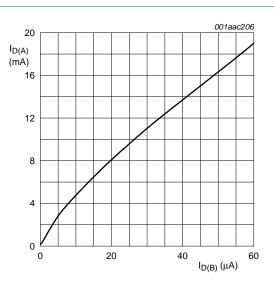
#### **Dual N-channel dual gate MOSFET**



- (1)  $V_{G2-S} = 4 V$ .
- (2)  $V_{G2-S} = 3.5 \text{ V}.$
- (3)  $V_{G2-S} = 3 \text{ V}.$
- (4)  $V_{G2-S} = 2.5 \text{ V}.$
- (5)  $V_{G2-S} = 2 \text{ V}$ .
- (6)  $V_{G2-S} = 1.5 \text{ V}.$

 $V_{DS(A)} = 5 \text{ V; } V_{G1\text{-}S(B)} = V_{DS(B)} = 0 \text{ V; } T_j = 25 \text{ }^{\circ}C.$ 



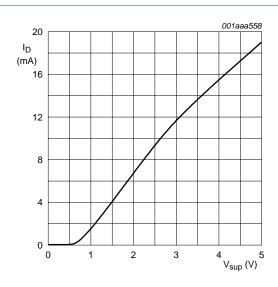


 $V_{DS(A)}=5$  V;  $V_{G2\text{-}S}=4$  V;  $V_{DS(B)}=5$  V;  $V_{G1\text{-}S(B)}=0$  V;  $T_j=25$  °C.

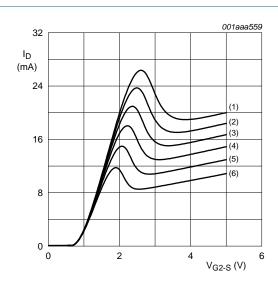
 $I_{D(B)}$  = internal G1 current = current in pin drain (B) if MOSFET (B) is switched off.

Fig 7. Amplifier A: drain current as a function of internal G1 current; typical values

#### **Dual N-channel dual gate MOSFET**



$$\begin{split} V_{DS(A)} &= V_{DS(B)} = V_{supply}; \ V_{G2\text{-}S} = 4 \ V; \ T_j = 25 \ ^{\circ}C; \\ R_{G1} &= 150 \ k\Omega \ \text{(connected to ground); see Figure 3.} \end{split}$$

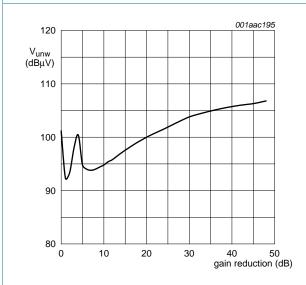


- (1)  $V_{DS(B)} = 5 \text{ V}.$
- (2)  $V_{DS(B)} = 4.5 \text{ V}.$
- (3)  $V_{DS(B)} = 4 \text{ V}.$
- (4)  $V_{DS(B)} = 3.5 \text{ V}.$
- (5)  $V_{DS(B)} = 3 \text{ V}.$
- (6)  $V_{DS(B)} = 2.5 \text{ V}.$

 $V_{DS(A)}$  = 5 V;  $V_{G1\text{-}S(B)}$  = 0 V; gate1 (A) = open;  $T_j$  = 25 °C.

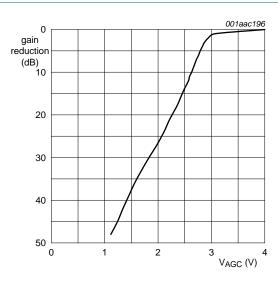
Fig 8. Amplifier A: drain current of amplifier A as a function of supply voltage of A and B amplifier; typical values





 $V_{DS(A)} = V_{DS(B)} = 5 \text{ V}; V_{G1-S(B)} = 0 \text{ V}; f_w = 50 \text{ MHz};$   $f_{unw} = 60 \text{ MHz}; T_{amb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 33}{\text{Figure } 33}.$ Fig. 10. Amplifier A: unwanted voltage for 1.9/

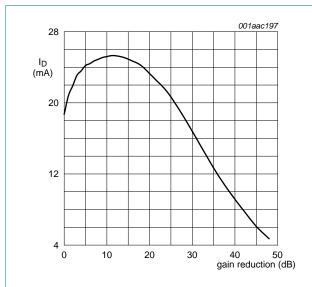
Fig 10. Amplifier A: unwanted voltage for 1 % cross-modulation as a function of gain reduction; typical values



 $V_{DS(A)} = V_{DS(B)} = 5$  V;  $V_{G1\text{-}S(B)} = 0$  V; f = 50 MHz; see Figure 33.

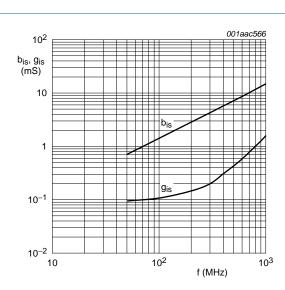
Fig 11. Amplifier A: gain reduction as a function of AGC voltage; typical values

## **Dual N-channel dual gate MOSFET**



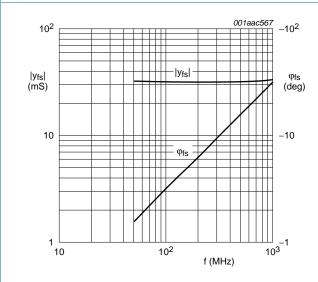
$$\begin{split} V_{DS(A)} &= V_{DS(B)} = 5 \text{ V; } V_{G1\text{-}S(B)} = 0 \text{ V; } f = 50 \text{ MHz;} \\ T_{amb} &= 25 \text{ °C; see } \underline{\text{Figure 33}}. \end{split}$$

Fig 12. Amplifier A: drain current as a function of gain reduction; typical values



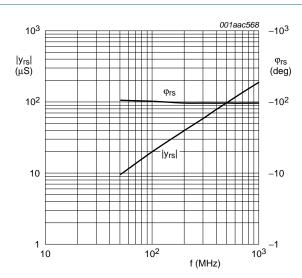
 $V_{DS(A)}$  = 5 V;  $V_{G2\text{-}S}$  = 4 V;  $V_{DS(B)}$  =  $V_{G1\text{-}S(B)}$  = 0 V;  $I_{D(A)}$  = 19 mA

Fig 13. Amplifier A: input admittance as a function of frequency; typical values



 $V_{DS(A)}=5$  V;  $V_{G2\text{-}S}=4$  V;  $V_{DS(B)}=V_{G1\text{-}S(B)}=0$  V;  $I_{D(A)}=19$  mA

Fig 14. Amplifier A: forward transfer admittance and phase as a function of frequency; typical values



 $V_{DS(A)}=5$  V;  $V_{G2\text{-}S}=4$  V;  $V_{DS(B)}=V_{G1\text{-}S(B)}=0$  V;  $I_{D(A)}=19$  mA

Fig 15. Amplifier A: reverse transfer admittance and phase as a function of frequency; typical values

#### **Dual N-channel dual gate MOSFET**

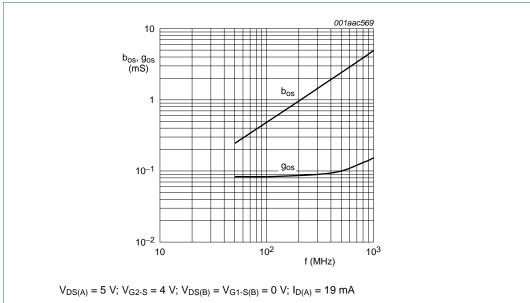


Fig 16. Amplifier A: output admittance as a function of frequency; typical values

#### 8.1.2 Scattering parameters for amplifier A

Table 9. Scattering parameters for amplifier A

 $V_{DS(A)} = 5 \text{ V; } V_{G2-S} = 4 \text{ V; } I_{D(A)} = 19 \text{ mA; } V_{DS(B)} = 0 \text{ V; } V_{G1-S(B)} = 0 \text{ V; } T_{amb} = 25 \text{ °C; typical values.}$ 

†	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
(MHz)	Magnitude (ratio)	Angle (deg)						
50	0.991	-3.86	3.08	175.91	0.0009	77.41	0.992	-1.41
100	0.990	-7.73	3.03	171.76	0.0019	78.10	0.991	-2.81
200	0.986	-15.43	2.99	163.68	0.0037	78.39	0.990	-5.57
300	0.980	-22.98	2.94	155.54	0.0054	73.53	0.989	-8.34
400	0.970	-30.44	2.89	147.55	0.0070	68.74	0.986	-11.08
500	0.960	-37.60	2.82	139.76	0.0085	63.64	0.983	-13.78
600	0.948	-44.62	2.75	132.16	0.0098	59.62	0.980	-16.45
700	0.935	-51.44	2.67	124.70	0.0110	55.09	0.977	-19.10
800	0.921	-58.04	2.58	117.39	0.0120	50.79	0.973	-21.69
900	0.908	-64.41	2.50	110.20	0.0128	46.62	0.970	-24.28
1000	0.894	-70.49	2.40	103.31	0.0135	42.78	0.967	-26.87

## 8.1.3 Noise data for amplifier A

Table 10. Noise data for amplifier A

 $V_{DS(A)} = 5$  V;  $V_{G2-S} = 4$  V;  $I_{D(A)} = 19$  mA;  $V_{DS(B)} = 0$  V;  $V_{G1-S(B)} = 0$  V;  $T_{amb} = 25$  °C; typical values; unless otherwise specified.

f (MHz)	NF <sub>min</sub> (dB)	$\Gamma_{opt}$		r <sub>n</sub> (Ω)
		ratio	(deg)	
400	1.3	0.718	16.06	0.683
800	1.4	0.677	37.59	0.681

## **Dual N-channel dual gate MOSFET**

# 8.2 Dynamic characteristics for amplifier B

Table 11. Dynamic characteristics for amplifier B[1]

Common source;  $T_{amb} = 25$  °C;  $V_{G2-S} = 4$  V;  $V_{DS} = 5$  V;  $I_D = 13$  mA; unless otherwise specified.

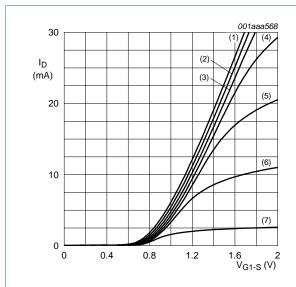
	, amb					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
y <sub>fs</sub>	forward transfer admittance	T <sub>j</sub> = 25 °C	28	33	43	mS
C <sub>iss(G1)</sub>	input capacitance at gate1	f = 1 MHz	-	2.0	2.5	pF
C <sub>iss(G2)</sub>	input capacitance at gate2	f = 1 MHz	-	3.4	-	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz	-	0.85	-	pF
C <sub>rss</sub>	reverse transfer capacitance	f = 1 MHz	-	20	-	fF
G <sub>tr</sub>	power gain	$B_{S} = B_{S(opt)};  B_{L} = B_{L(opt)}$				
		$f = 200 \text{ MHz}; G_S = 2 \text{ mS}; G_L = 0.5 \text{ mS}$	33	37	41	dB
		$f = 400 \text{ MHz}; G_S = 2 \text{ mS}; G_L = 1 \text{ mS}$	30	34	38	dB
		$f = 800 \text{ MHz}; G_S = 3.3 \text{ mS}; G_L = 1 \text{ mS}$	29	33	37	dB
NF	noise figure	$f = 11 \text{ MHz}; G_S = 20 \text{ mS}; B_S = 0 \text{ S}$	-	5	-	dB
		$f = 400 \text{ MHz}; Y_S = Y_{S(opt)}$	-	1.3	1.9	dB
		$f = 800 \text{ MHz}; Y_S = Y_{S(opt)}$	-	1.4	2.1	dB
Xmod	cross-modulation	input level for $k = 1 \%$ ; $f_w = 50 \text{ MHz}$ ; $f_{unw} = 60 \text{ MHz}$	[2]			
		at 0 dB AGC	90	-	-	dΒμV
		at 10 dB AGC	-	88	-	dΒμV
		at 20 dB AGC	-	94	-	dΒμV
		at 40 dB AGC	100	103	-	dΒμV

<sup>[1]</sup> For the MOSFET not in use:  $V_{G1-S(A)} = 0 \text{ V}$ ;  $V_{DS(A)} = 0 \text{ V}$ .

<sup>[2]</sup> Measured in Figure 34 test circuit.

## **Dual N-channel dual gate MOSFET**

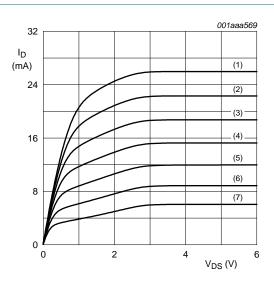
## 8.2.1 Graphics for amplifier B



- (1)  $V_{G2-S} = 4 \text{ V}$ .
- (2)  $V_{G2-S} = 3.5 \text{ V}.$
- (3)  $V_{G2-S} = 3 \text{ V}.$
- (4)  $V_{G2-S} = 2.5 \text{ V}.$
- (5)  $V_{G2-S} = 2 V$ .
- (6)  $V_{G2-S} = 1.5 \text{ V}.$
- (7)  $V_{G2-S} = 1 \text{ V}.$

 $V_{DS(B)} = 5 \text{ V}; \ V_{DS(A)} = V_{G1\text{-}S(A)} = 0 \text{ V}; \ T_j = 25 \text{ }^{\circ}C.$ 

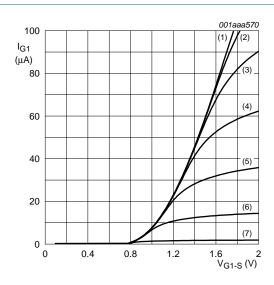
Fig 17. Amplifier B: transfer characteristics; typical values



- (1)  $V_{G1-S(B)} = 1.6 \text{ V}.$
- (2)  $V_{G1-S(B)} = 1.5 \text{ V}.$
- (3)  $V_{G1-S(B)} = 1.4 \text{ V}.$
- (4)  $V_{G1-S(B)} = 1.3 \text{ V}.$
- (5)  $V_{G1-S(B)} = 1.2 \text{ V}.$
- (6)  $V_{G1-S(B)} = 1.1 \text{ V}.$ (7)  $V_{G1-S(B)} = 1 \text{ V}.$ 
  - $V_{G2-S} = 4 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V}; T_j = 25 \text{ °C}.$

Fig 18. Amplifier B: output characteristics; typical values

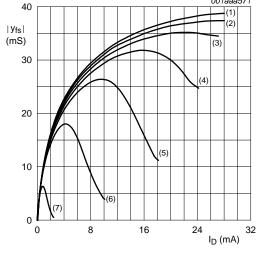
#### **Dual N-channel dual gate MOSFET**



- (1)  $V_{G2-S} = 4 V$ .
- (2)  $V_{G2-S} = 3.5 \text{ V}.$
- (3)  $V_{G2-S} = 3 \text{ V}.$
- (4)  $V_{G2-S} = 2.5 \text{ V}.$
- (5)  $V_{G2-S} = 2 \text{ V}.$
- (6)  $V_{G2-S} = 1.5 \text{ V}.$
- (7)  $V_{G2-S} = 1 V$ .

 $V_{DS(B)} = 5 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}.$ 

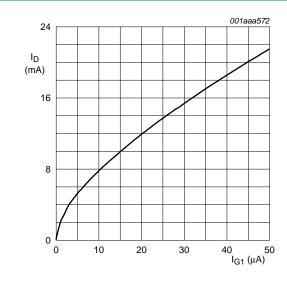
Fig 19. Amplifier B: gate1 current as a function of gate1 voltage; typical values



- (1)  $V_{G2-S} = 4 \text{ V}$ .
- (2)  $V_{G2-S} = 3.5 \text{ V}.$
- (3)  $V_{G2-S} = 3 \text{ V}.$
- (4)  $V_{G2-S} = 2.5 \text{ V}.$
- (5)  $V_{G2-S} = 2 V$ .
- (6)  $V_{G2-S} = 1.5 \text{ V}.$
- (7)  $V_{G2-S} = 1 \text{ V}$ .

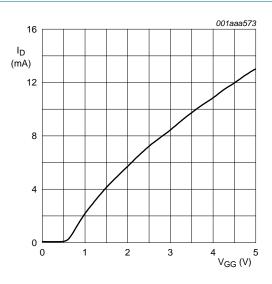
 $V_{DS(B)} = 5 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}.$ 

Fig 20. Amplifier B: forward transfer admittance as a function of drain current; typical values



 $V_{DS(B)} = 5 \text{ V}; V_{G2-S} = 4 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V}; T_i = 25 ^{\circ}C.$ 

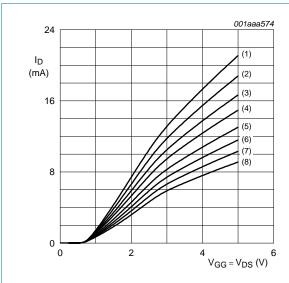
Fig 21. Amplifier B: drain current as a function of gate1 current; typical values



 $V_{DS(B)}$  = 5 V;  $V_{G2\text{-}S}$  = 4 V;  $V_{DS(A)}$  =  $V_{G1\text{-}S(A)}$  = 0 V;  $T_j$  = 25 °C;  $R_{G1}$  = 150 k $\Omega$  (connected to  $V_{GG}$ ); see Figure 3.

Fig 22. Amplifier B: drain current as a function of gate1 supply voltage; typical values

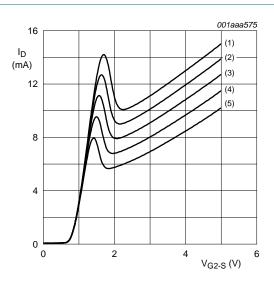
## **Dual N-channel dual gate MOSFET**



- (1)  $R_{G1} = 68 \text{ k}\Omega$ .
- (2)  $R_{G1} = 82 \text{ k}\Omega$ .
- (3)  $R_{G1} = 100 \text{ k}\Omega$ .
- (4)  $R_{G1} = 120 \text{ k}\Omega$ .
- (5)  $R_{G1} = 150 \text{ k}\Omega$ .
- (6)  $R_{G1} = 180 kΩ$ .
- (7)  $R_{G1} = 220 \text{ k}\Omega$ .
- (8)  $R_{G1} = 270 \text{ k}\Omega$ .

 $V_{G2\text{-S}}=4$  V;  $V_{DS(A)}=V_{G1\text{-S}(A)}=0$  V;  $T_j=25$  °C;  $R_{G1}$  is connected to  $V_{GG};$  see Figure 3.

Fig 23. Amplifier B: drain current as a function of gate1 supply voltage and drain supply voltage; typical values

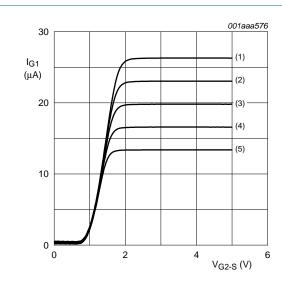


- (1)  $V_{GG} = 5.0 \text{ V}.$
- (2)  $V_{GG} = 4.5 \text{ V}.$
- (3)  $V_{GG} = 4.0 \text{ V}.$
- (4)  $V_{GG} = 3.5 \text{ V}.$
- (5)  $V_{GG} = 3.0 \text{ V}.$

 $V_{DS(B)} = 5$  V;  $V_{DS(A)} = V_{G1\text{-}S(A)} = 0$  V;  $T_j = 25$  °C;  $R_{G1} = 150$  k $\Omega$  (connected to  $V_{GG}$ ); see Figure 3.

Fig 24. Amplifier B: drain current as a function of gate2 voltage; typical values

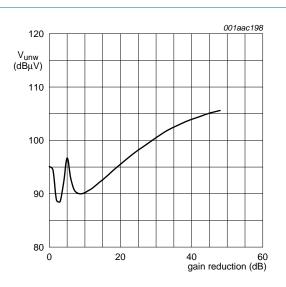
#### **Dual N-channel dual gate MOSFET**



- (1)  $V_{GG} = 5.0 \text{ V}.$
- (2)  $V_{GG} = 4.5 \text{ V}.$
- (3)  $V_{GG} = 4.0 \text{ V}.$
- (4)  $V_{GG} = 3.5 \text{ V}.$
- (5)  $V_{GG} = 3.0 \text{ V}.$

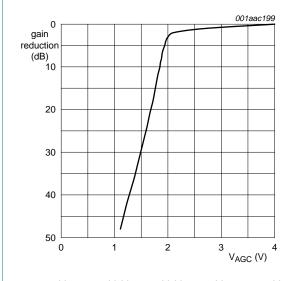
 $V_{DS(B)} = 5 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$  $R_{G1} = 150 \text{ k}\Omega$  (connected to  $V_{GG}$ ); see Figure 3.

Fig 25. Amplifier B: gate1 current as a function of gate2 voltage; typical values



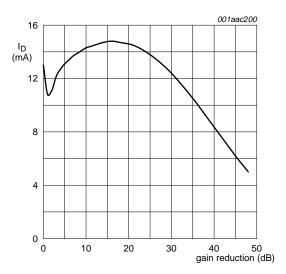
 $\begin{array}{l} V_{DS(B)} = 5 \text{ V; } V_{GG} = 5 \text{ V; } V_{DS(A)} = V_{G1\text{-}S(A)} = 0 \text{ V; } \\ R_{G1} = 150 \text{ } k\Omega \text{ (connected to } V_{GG); } f_w = 50 \text{ MHz; } \\ f_{unw} = 60 \text{ MHz; } T_{amb} = 25 \text{ }^{\circ}\text{C; see Figure 34.} \end{array}$ 

Fig 26. Amplifier B: unwanted voltage for 1 % cross-modulation as a function of gain reduction; typical values



$$\begin{split} &V_{DS(B)}=5~\text{V; }V_{GG}=5~\text{V; }V_{DS(A)}=V_{G1\text{-}S(A)}=0~\text{V;}\\ &R_{G1}=150~\text{k}\Omega~\text{(connected to }V_{GG})\text{; }f=50~\text{MHz;}\\ &T_{amb}=25~\text{°C; see}~\underset{Figure}{Figure}~34. \end{split}$$

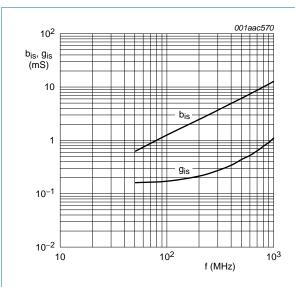
Fig 27. Amplifier B: gain reduction as a function of AGC voltage; typical values



 $V_{DS(B)} = 5 \text{ V}; V_{GG} = 5 \text{ V}; V_{DS(A)} = V_{G1\text{-}S(A)} = 0 \text{ V};$   $R_{G1} = 150 \text{ k}\Omega$  (connected to  $V_{GG}$ ); f = 50 MHz;  $T_{amb} = 25 \text{ °C};$  see Figure 34.

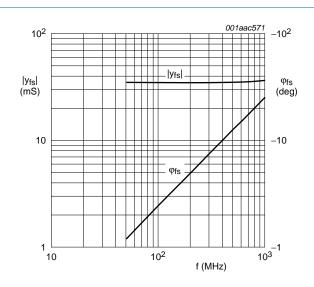
Fig 28. Amplifier B: drain current as a function of gain reduction; typical values

#### **Dual N-channel dual gate MOSFET**



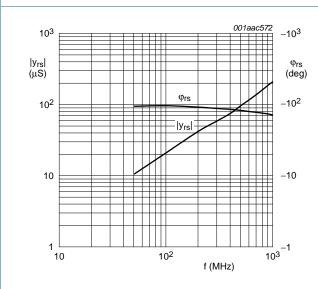
 $V_{DS(B)}=5$  V;  $V_{G2\text{-}S}=4$  V;  $V_{DS(A)}=V_{G1\text{-}S(A)}=0$  V;  $I_{D(B)}=13$  mA

Fig 29. Amplifier B: input admittance as a function of frequency; typical values



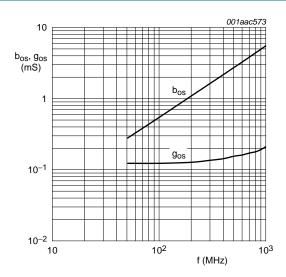
 $V_{DS(B)}=5$  V;  $V_{G2\text{-}S}=4$  V;  $V_{DS(A)}=V_{G1\text{-}S(A)}=0$  V;  $I_{D(B)}=13$  mA

Fig 30. Amplifier B: forward transfer admittance and phase as a function of frequency; typical values



 $V_{DS(B)} = 5 \text{ V}; V_{G2-S} = 4 \text{ V}; V_{DS(A)} = V_{G1-S(A)} = 0 \text{ V};$   $I_{D(B)} = 13 \text{ mA}$ 

Fig 31. Amplifier B: reverse transfer admittance and phase as a function of frequency; typical values



 $V_{DS(B)}$  = 5 V;  $V_{G2\text{-}S}$  = 4 V;  $V_{DS(A)}$  =  $V_{G1\text{-}S(A)}$  = 0 V;  $I_{D(B)}$  = 13 mA

Fig 32. Amplifier B: output admittance as a function of frequency; typical values

## **Dual N-channel dual gate MOSFET**

## 8.2.2 Scattering parameters for amplifier B

Table 12. Scattering parameters for amplifier B

 $V_{DS(B)} = 5 \text{ V}; V_{G2-S} = 4 \text{ V}; I_{D(B)} = 13 \text{ mA}; V_{DS(A)} = 0 \text{ V}; V_{G1-S(A)} = 0 \text{ V}; T_{amb} = 25 ^{\circ}\text{C}; typical values.$ 

f (MHz)	s <sub>11</sub>		s <sub>21</sub>		s <sub>12</sub>		S <sub>22</sub>	
	Magnitude (ratio)	Angle (deg)						
50	0.985	-3.42	3.33	176.41	0.0010	87.55	0.988	-1.60
100	0.984	-6.96	3.31	172.70	0.0020	83.45	0.988	-3.16
200	0.980	-13.51	3.27	165.59	0.0039	82.84	0.987	-6.31
300	0.975	-20.07	3.23	158.42	0.0054	82.01	0.986	-9.40
400	0.969	-26.61	3.19	151.34	0.0068	79.73	0.984	-12.46
500	0.961	-32.89	3.14	144.33	0.0085	77.91	0.982	-15.57
600	0.955	-39.19	3.07	137.54	0.0100	76.31	0.980	-18.62
700	0.945	-45.39	3.00	130.72	0.0115	73.76	0.977	-21.70
800	0.938	-51.39	2.93	123.98	0.0131	71.58	0.974	-24.76
900	0.930	-57.36	2.85	117.31	0.0145	69.18	0.971	-27.81
1000	0.920	-63.10	2.77	110.39	0.0157	67.54	0.967	-30.86

## 8.2.3 Noise data for amplifier B

Table 13. Noise data for amplifier B

 $V_{DS(B)} = 5$  V;  $V_{G2-S} = 4$  V;  $I_{D(B)} = 13$  mA;  $V_{DS(A)} = 0$  V;  $V_{G1-S(A)} = 0$  V;  $T_{amb} = 25$  °C; typical values; unless otherwise specified.

f (MHz)	NF <sub>min</sub> (dB)	$\Gamma_{opt}$		r <sub>n</sub> (Ω)
		ratio	(deg)	
400	1.3	0.695	13.11	0.694
800	1.4	0.674	32.77	0.674

## **Dual N-channel dual gate MOSFET**

# 9. Test information

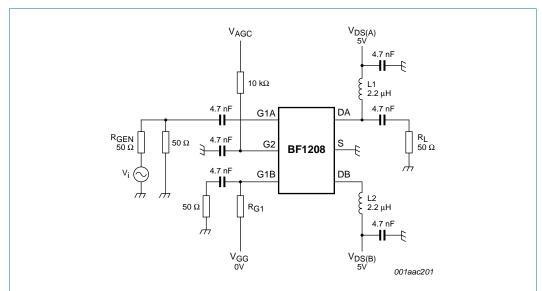


Fig 33. Cross-modulation test set-up for amplifier A

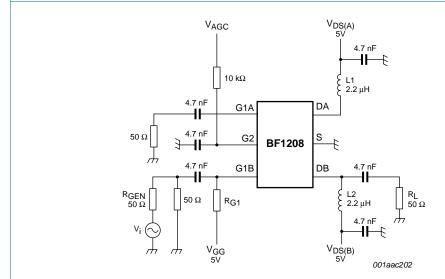


Fig 34. Cross-modulation test set-up for amplifier B

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## **Dual N-channel dual gate MOSFET**

# 10. Package outline

## **SOT666** Plastic surface-mounted package; 6 leads - A Χ S pin 1 index - ⊕ w M A detail X 2 mm scale **DIMENSIONS (mm are the original dimensions)** UNIT Ε D Α bp С e<sub>1</sub> $H_{\mathsf{E}}$ $L_p$ у 0.6 0.27 1.7 1.5 1.7 1.5 0.3 0.1 0.18 1.3 0.5 0.17 0.08 1.1 REFERENCES **EUROPEAN** OUTLINE ISSUE DATE VERSION JEDEC **PROJECTION** IEC

Fig 35. Package outline SOT666

SOT666

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04-11-08

06-03-16

**JEITA** 

## **Dual N-channel dual gate MOSFET**

# 11. Revision history

## Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1208 v.2	20110907	Product data sheet	-	BF1208 v.1
Modifications:	guidelines o  Legal texts	of this data sheet has been of NXP Semiconductors. have been adapted to the ruthine drawings have been u	new company name whe	re appropriate.
BF1208 v.1 (9397 750 14254)	20050316	Product data sheet	-	-

#### **Dual N-channel dual gate MOSFET**

## 12. Legal information

#### 12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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#### **Dual N-channel dual gate MOSFET**

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**BF1208 NXP Semiconductors** 

## **Dual N-channel dual gate MOSFET**

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