PCA9557

8-bit I²C-bus and SMBus I/O port with reset

Rev. 7 — 10 December 2013 Product data sheet

1. General description

The PCA9557 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus and I²C-bus applications. The PCA9557 consists of an 8-bit input port register, 8-bit output port register, and an I²C-bus/SMBus interface. It has low current consumption and a high-impedance open-drain output pin, IO0.

The system master can enable the PCA9557's I/O as either input or output by writing to the configuration register. The system master can also invert the PCA9557 inputs by writing to the active HIGH polarity inversion register. Finally, the system master can reset the PCA9557 in the event of a time-out by asserting a LOW in the reset input.

The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

2. Features and benefits

- Lower voltage, higher performance migration path for the PCA9556
- 8 general purpose input/output expander/collector
- Input/output configuration register
- Active HIGH polarity inversion register
- I²C-bus and SMBus interface logic
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active LOW reset input
- 3 address pins allowing up to 8 devices on the I²C-bus/SMBus
- High-impedance open-drain on IO0
- No glitch on power-up
- Power-up with all channels configured as inputs
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs/outputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Three packages offered: SO16, TSSOP16, HVQFN16

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9557BS	9557	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9557D	PCA9557D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
PCA9557PW	PCA9557	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9557BS	PCA9557BS,118	HVQFN16	Reel 13” Q1/T1 *Standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCA9557D	PCA9557D,112	SO16	Standard marking * IC’s tube - DSC bulk pack	1000	T_{amb} = −40 °C to +85 °C
	PCA9557D,118	SO16	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9557PW	PCA9557PW,112	TSSOP16	Standard marking * IC’s tube - DSC bulk pack	2400	T_{amb} = −40 °C to +85 °C
	PCA9557PW,118	TSSOP16	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

4. Block diagram

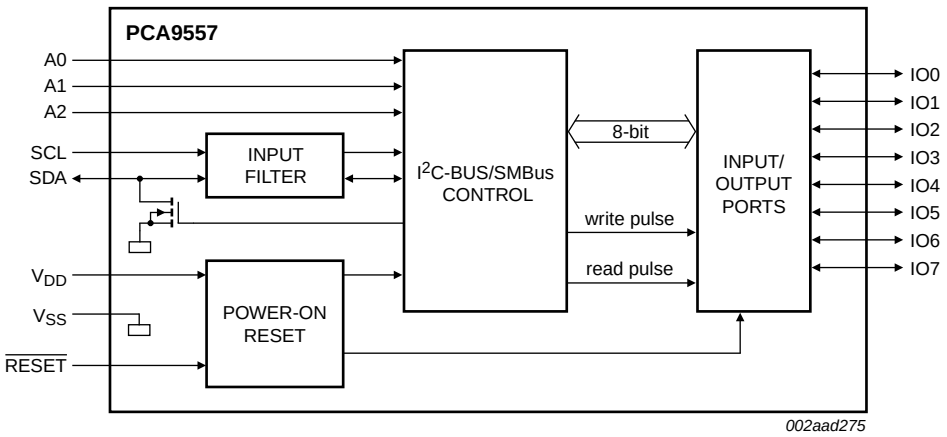
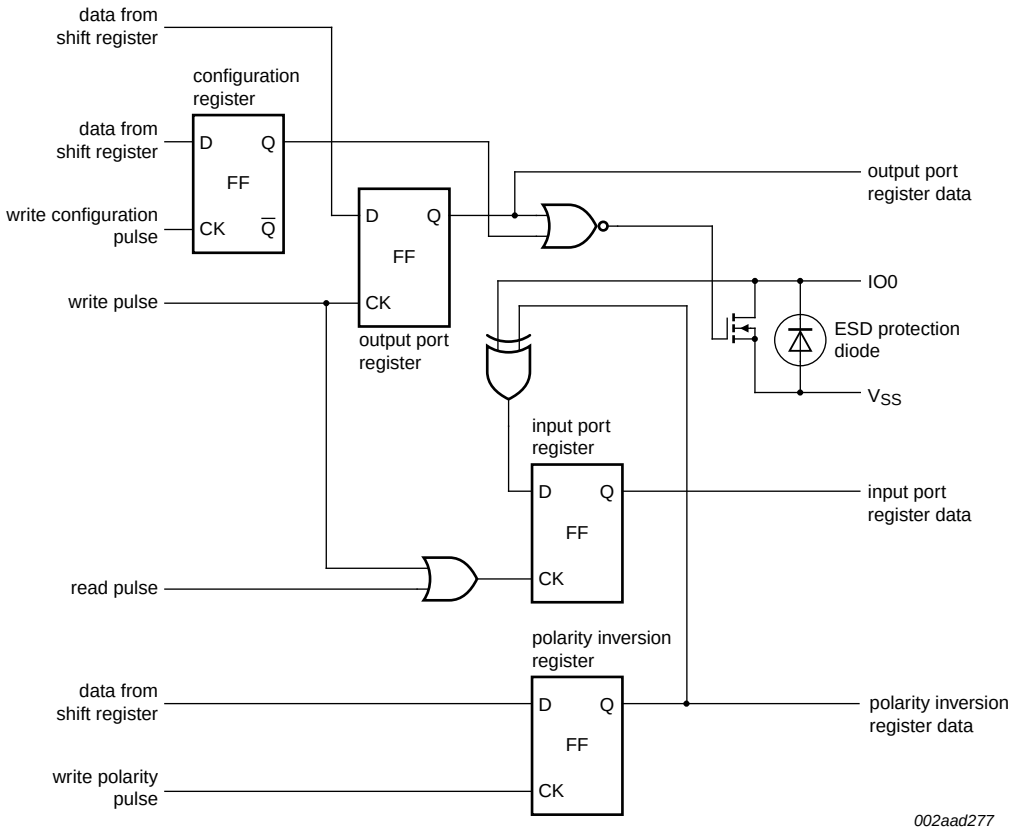
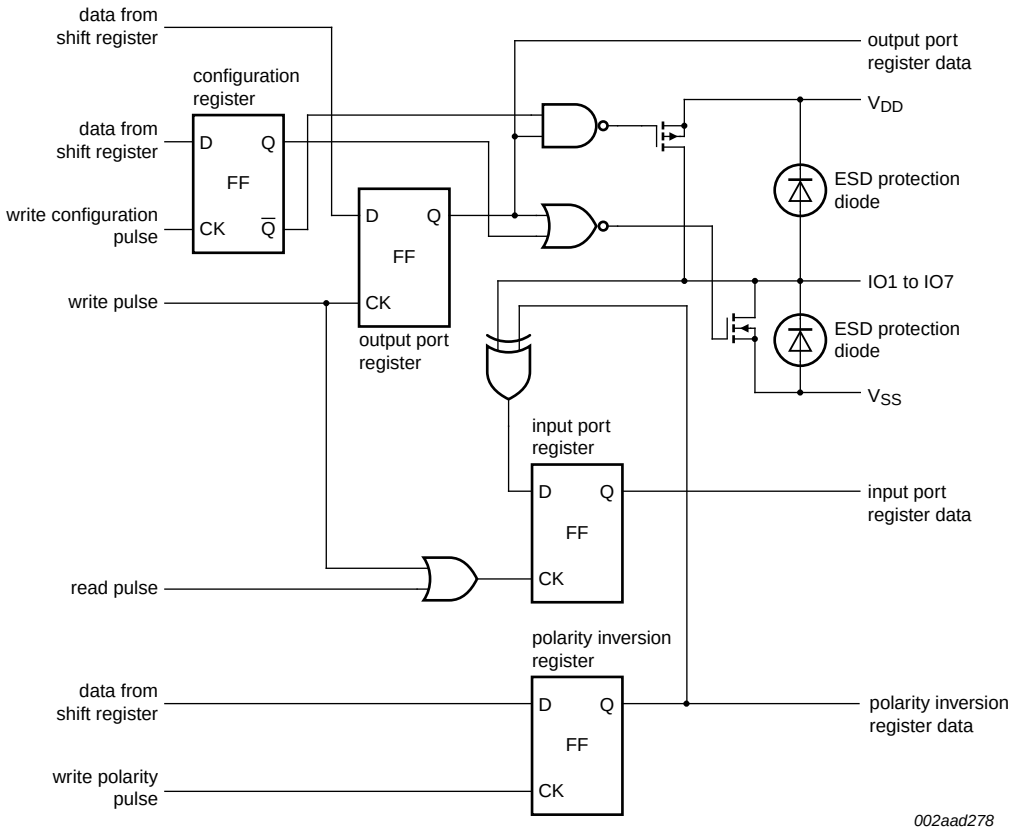


Fig 1. Block diagram of PCA9557



On power-up or reset, all registers return to default values.

Fig 2. Simplified schematic of IO0



On power-up or reset, all registers return to default values.

Fig 3. Simplified schematic of IO1 to IO7

5. Pinning information

5.1 Pinning

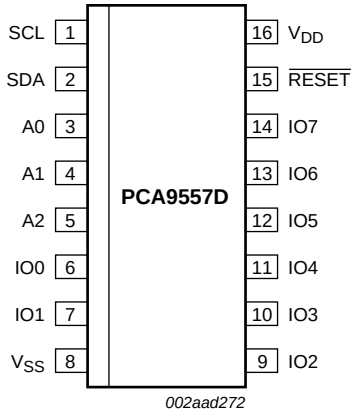


Fig 4. Pin configuration for SO16

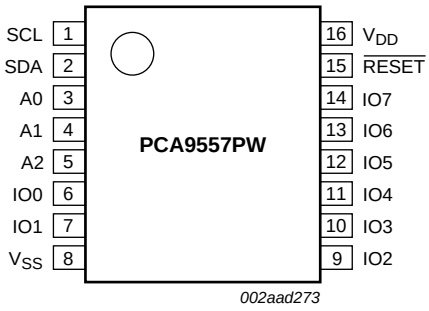


Fig 5. Pin configuration for TSSOP16

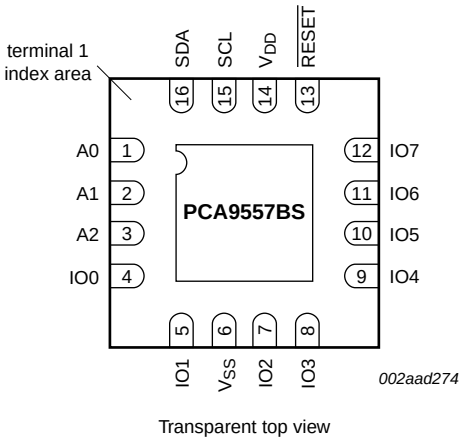


Fig 6. Pin configuration for HVQFN16

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
SCL	1	15	serial clock line
SDA	2	16	serial data line
A0	3	1	address input 0
A1	4	2	address input 1
A2	5	3	address input 2
IO0	6	4	input/output 0 (open-drain)
IO1	7	5	input/output 1

Table 3. Pin description *...continued*

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
V_{SS}	8	6[1]	supply ground
IO2	9	7	input/output 2
IO3	10	8	input/output 3
IO4	11	9	input/output 4
IO5	12	10	input/output 5
IO6	13	11	input/output 6
IO7	14	12	input/output 7
$\overline{RESET}$	15	13	active LOW reset input
V_{DD}	16	14	supply voltage

[1] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

6. System diagram

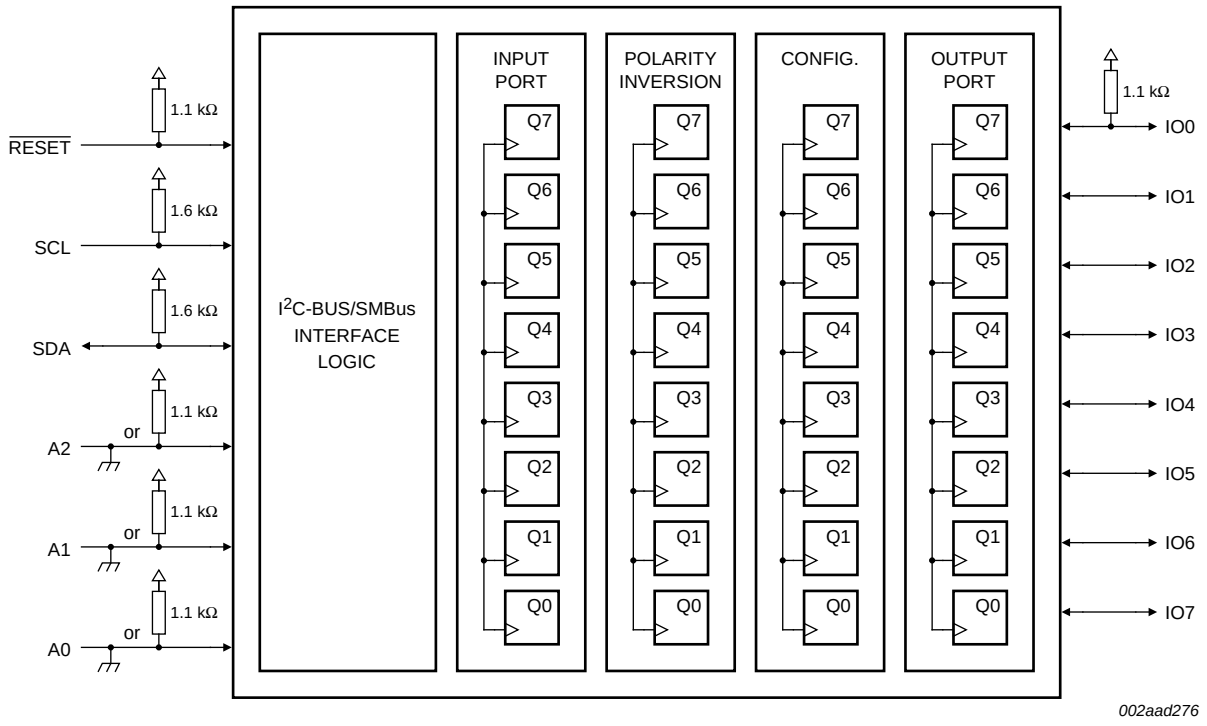


Fig 7. System diagram

7. Functional description

Refer to Figure 1 “Block diagram of PCA9557”.

7.1 Device address

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9557 is shown in Figure 8. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

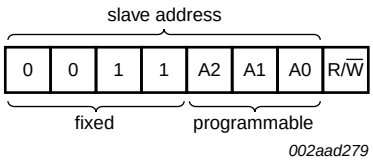


Fig 8. PCA9557 device address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9557, which will be stored in the control register. This register can be written and read via the I²C-bus.

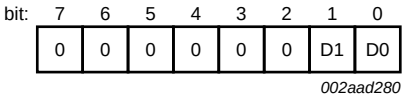


Fig 9. Control register

Table 4. Register definition

D1	D0	Name	Access	Description
0	0	Register 0	read-only	Input port register
0	1	Register 1	read/write	Output port register
1	0	Register 2	read/write	Polarity inversion register
1	1	Register 3	read/write	Configuration register

7.3 Register descriptions

7.3.1 Register 0 - Input port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. Writes to this register have no effect.

Table 5. Register 0 - Input port register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0

7.3.2 Register 1 - Output port register

This register reflects the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output port register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

7.3.3 Register 2 - Polarity inversion register

This register enables polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with logic 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with logic 0), the corresponding port pin's original polarity is retained.

Table 7. Register 2 - Polarity inversion register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	1	1	1	1	0	0	0	0

7.3.4 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output.

Table 8. Register 3 - Configuration register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

7.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9557 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9557 registers and I²C-bus/SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.5 $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9557 registers and SMBus/I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input requires a pull-up resistor to V_{DD} if no active connection is used.

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

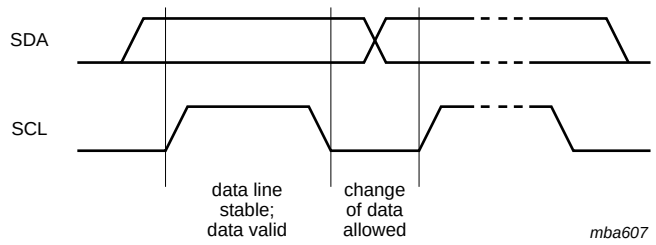


Fig 10. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 11).

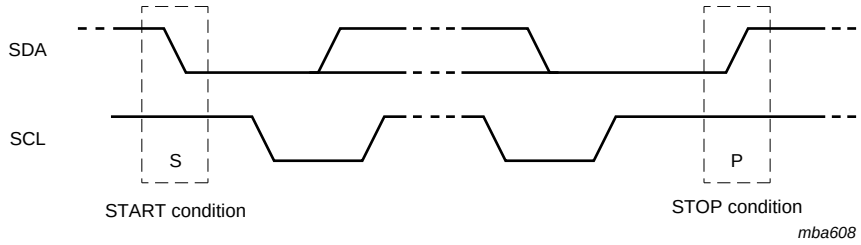


Fig 11. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 12).

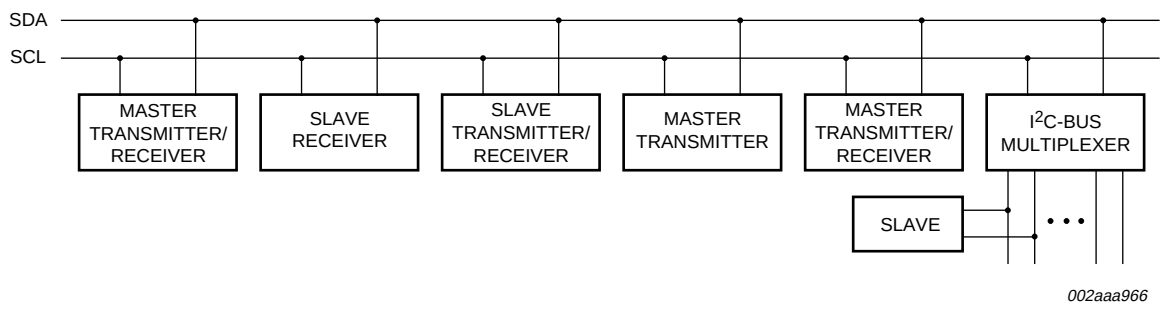


Fig 12. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

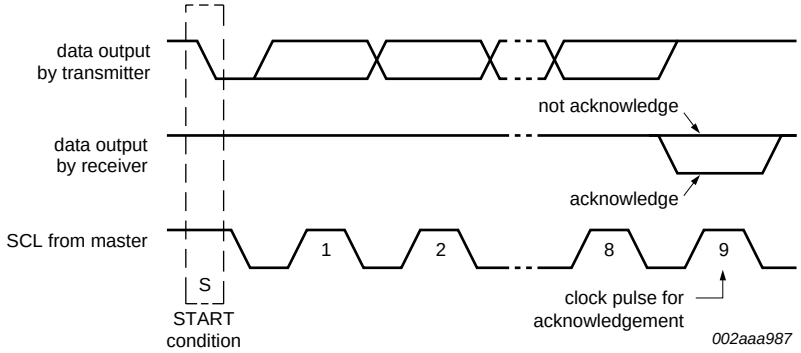


Fig 13. Acknowledgement on the I²C-bus

8.4 Bus transactions

Data is transmitted to the PCA9557 registers using Write Byte transfers (see Figure 14 and Figure 15). Data is read from the PCA9557 registers using Read and Receive Byte transfers (see Figure 16 and Figure 17).

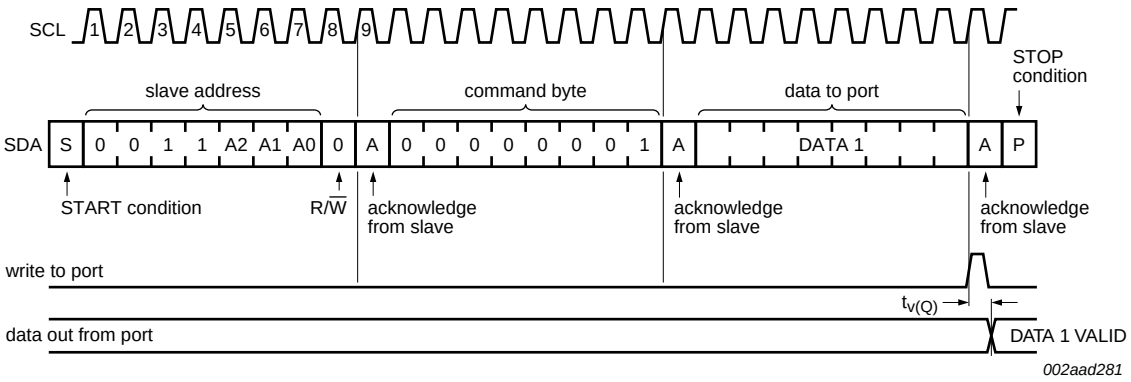


Fig 14. Write to output port register

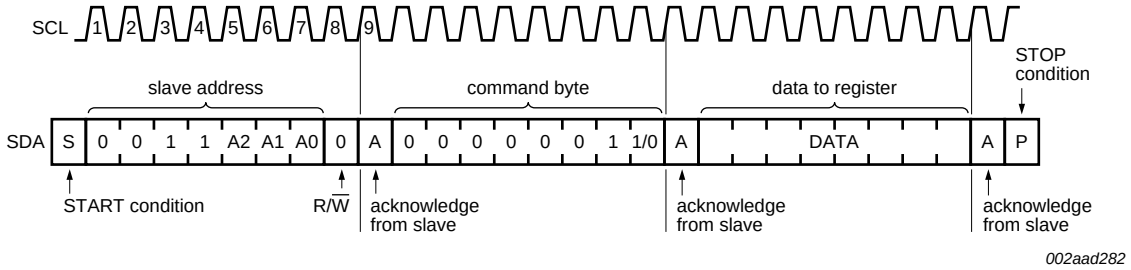


Fig 15. Write to I/O configuration or polarity inversion registers

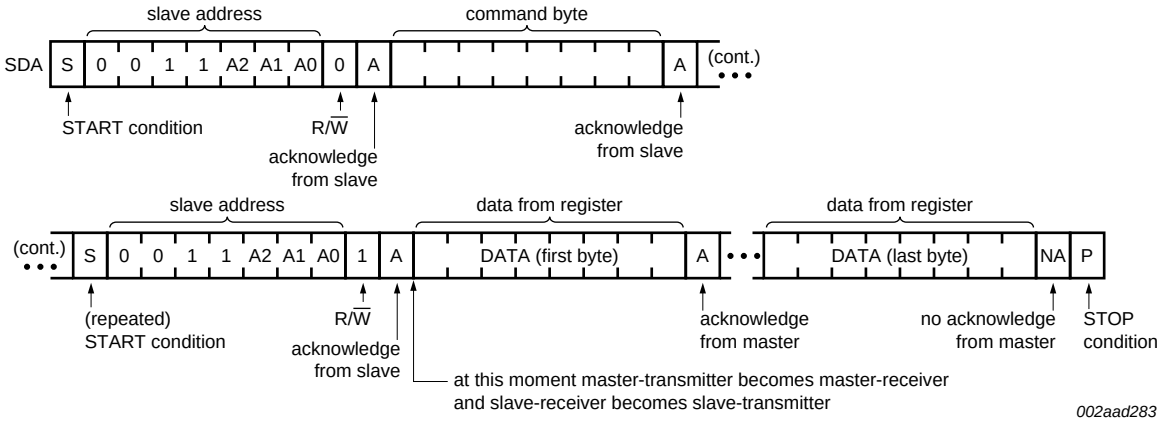
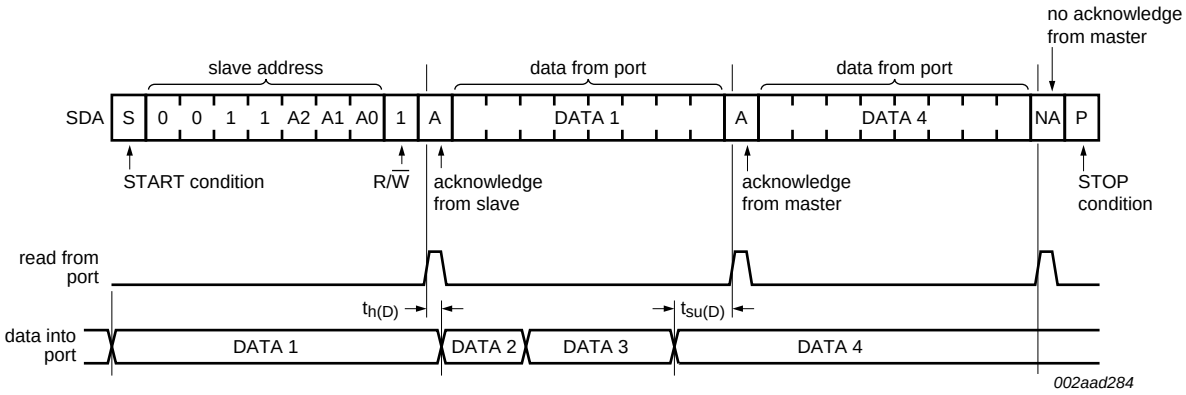


Fig 16. Read from register

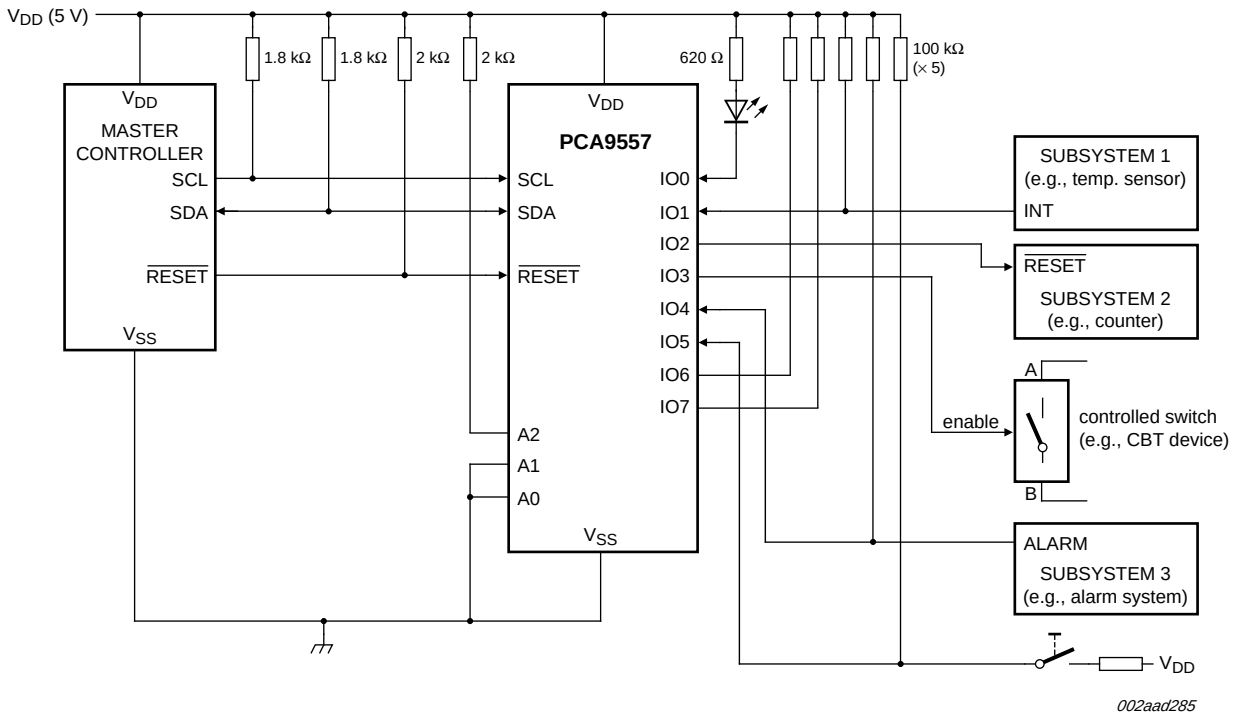


Remark: This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig 17. Read input port register

9. Application design-in information



Device address configured as 0011 100x for this example.

IO0, IO2, IO3 configured as outputs.

IO1, IO4, IO5 configured as inputs.

IO6, IO7 are not used.

Fig 18. Typical application

9.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 18. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 19 shows a high value resistor in parallel with the LED. Figure 20 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

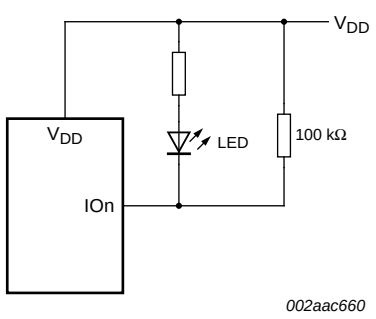


Fig 19. High value resistor in parallel with the LED

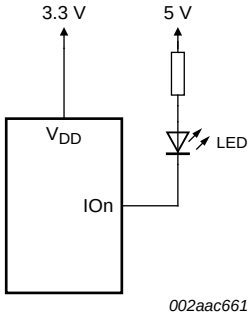


Fig 20. Device supplied by a lower voltage

10. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6	V
V_I	input voltage		V_{SS} – 0.5	5.5	V
I_I	input current		-	±20	mA
$I_{IHL(max)}$	maximum allowed input current through protection diode (IO1 to IO7)	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	-	±400	μA
$V_{I/O}$	voltage on an input/output pin	I/O as an input, except IO0	V_{SS} – 0.5	5.5	V
		IO0 as an input	V_{SS} – 0.5	5.5	V
$I_{I/O}$	input/output current	IO0 as an input	-	+400	μA
			-	–20	mA
$I_{O(IOn)}$	output current on pin IOn		-	±50	mA
I_{DD}	supply current		-	85	mA
I_{SS}	ground supply current		-	100	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

11. Static characteristics

Table 10. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz		-	19	25	µA
I_{stbL}	LOW-level standby current	standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
I_{stbH}	HIGH-level standby current	standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
ΔI_{stb}	additional standby current	standby mode; V_{DD} = 5.5 V; every LED I/O at V_I = 4.3 V; f_{SCL} = 0 kHz		-	0.8	1	mA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.65	2.1	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		3	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 5.5 V; V_{DD} = 2.3 V	[2]	8	10	-	mA
I_{OH}	HIGH-level output current	except pin IO0; V_{OH} = 2.4 V	[3]	4	-	-	mA
		pin IO0; V_{OH} = 4.6 V		-	-	1	µA
		pin IO0; V_{OH} = 3.3 V		-	-	1	µA
I_{LI}	input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}		-	-	−100	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF
Select inputs A0, A1, A2 and $\overline{\text{RESET}}$							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] The total amount sunk by all I/Os must be limited to 100 mA and 25 mA per bit.

[3] The total current sourced by all I/Os must be limited to 85 mA and 20 mA per bit.

12. Dynamic characteristics

Table 11. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	-	1	-	0.9	µs
$t_{VD;DAT}$	data valid time	[2]	-	1	-	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [3]	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	data output valid time	pin IO0	-	250	-	250	ns
		pins IO1 to IO7	-	200	-	200	ns
$t_{su(D)}$	data input set-up time		0	-	0	-	ns
$t_{h(D)}$	data input hold time		200	-	200	-	ns
Reset timing							
$t_{w(rst)}$	reset pulse width		6	-	6	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	ns
t_{rst}	reset time		400	-	400	-	ns

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

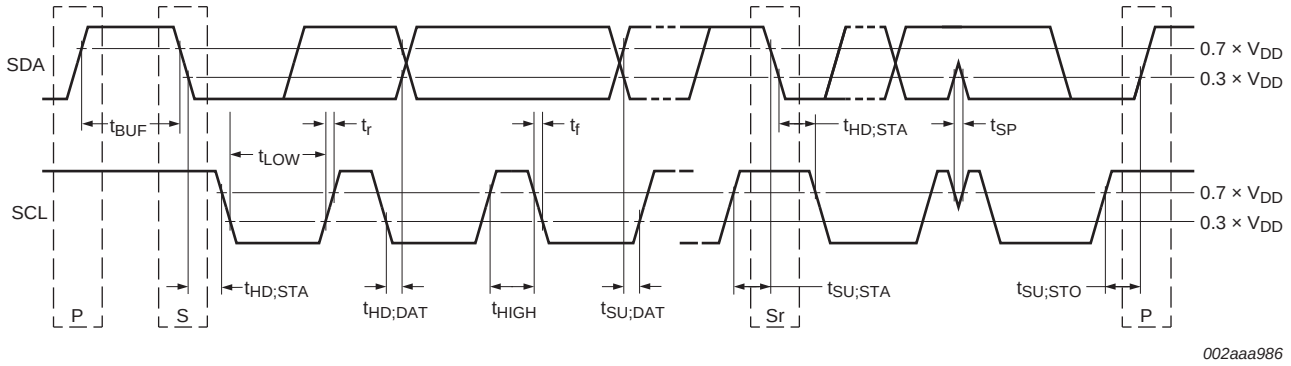


Fig 21. Definition of timing on the I²C-bus

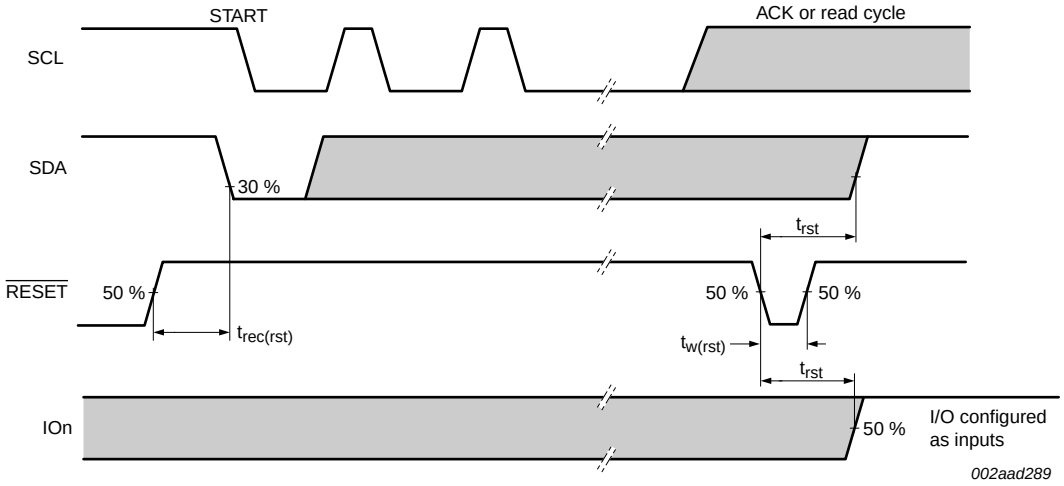
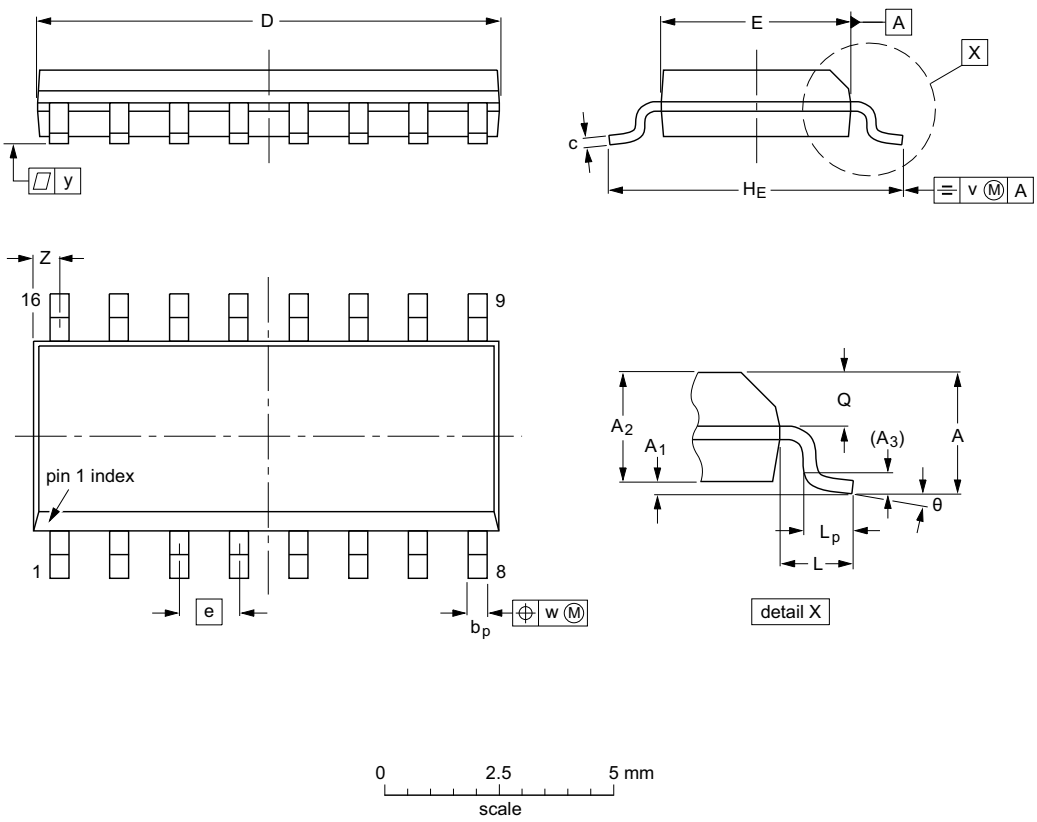


Fig 22. Definition of $\overline{\text{RESET}}$ timing

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

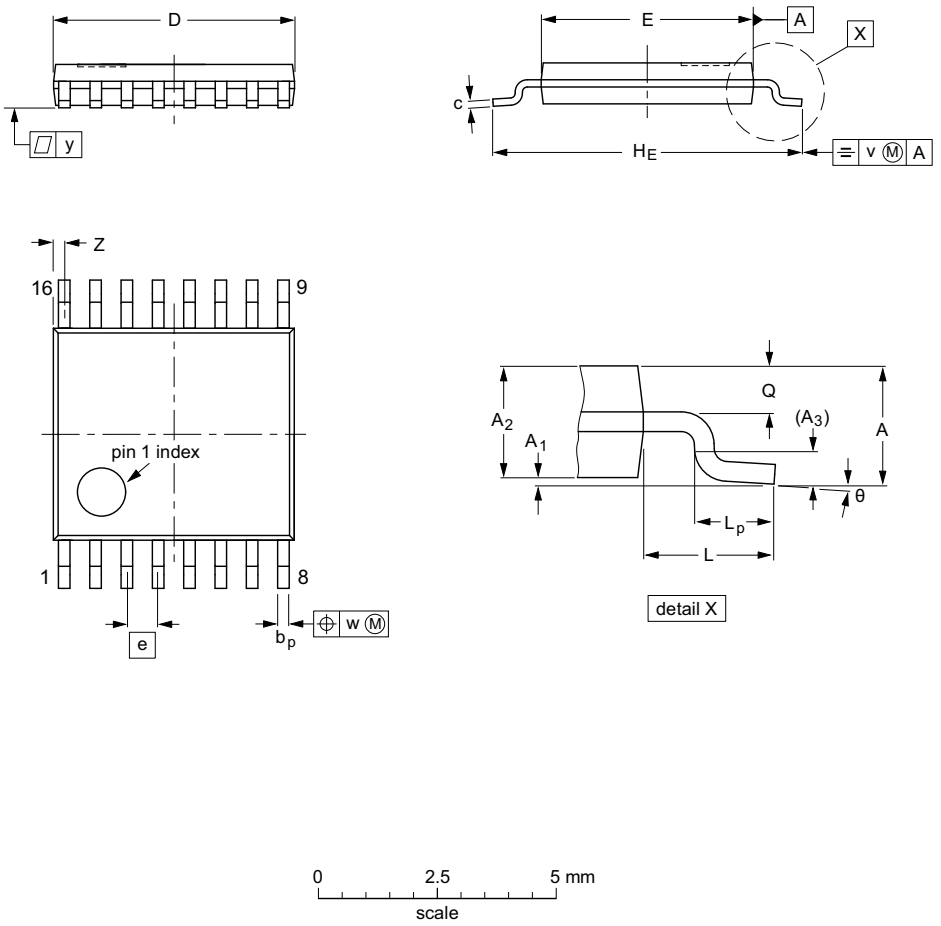
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

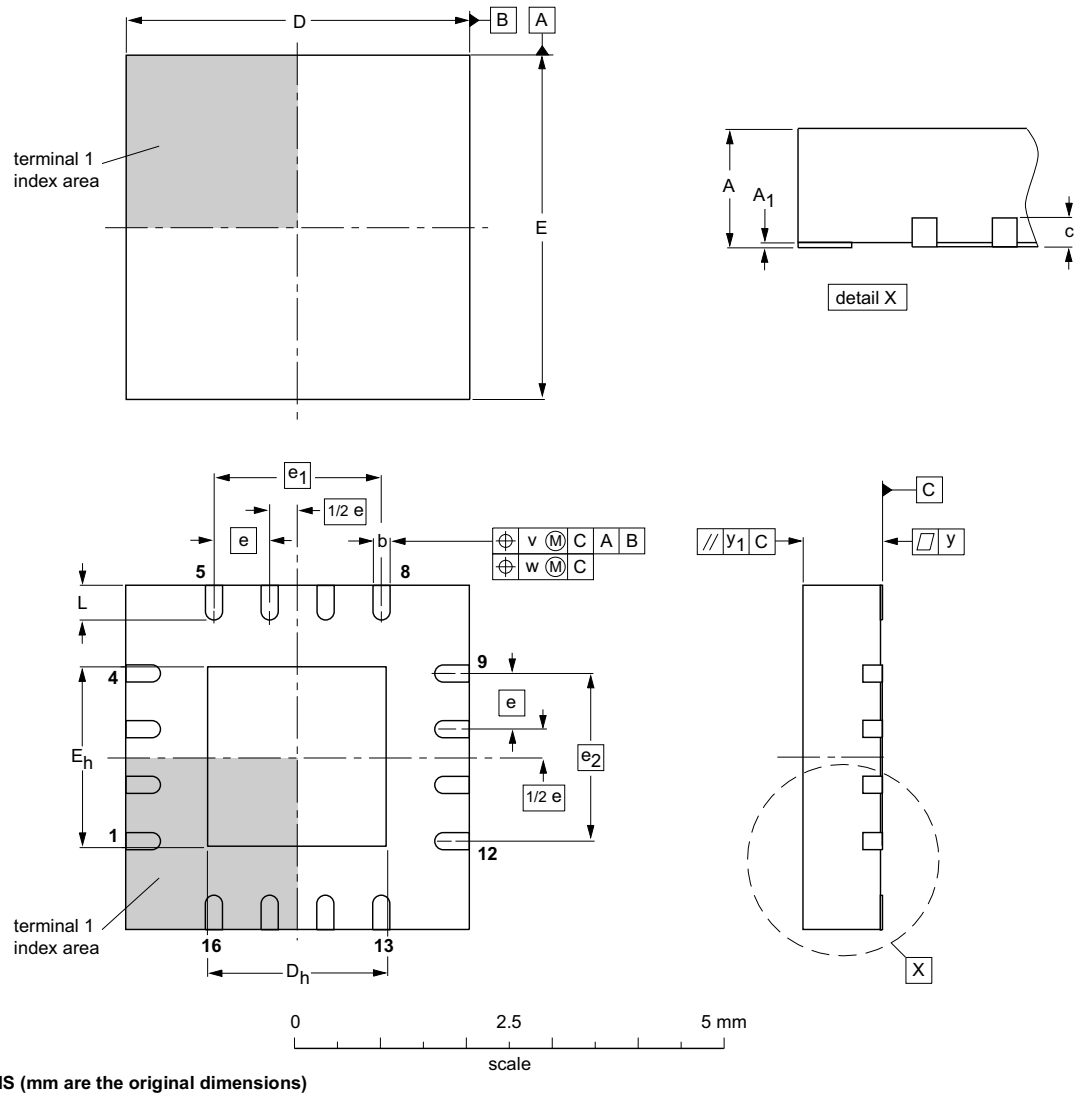
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 24. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 25. Package outline SOT629-1 (HVQFN16)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020D)

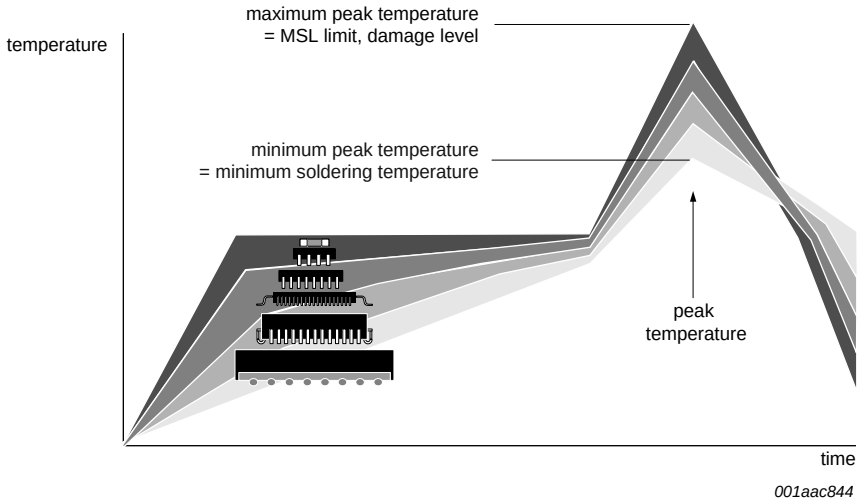
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



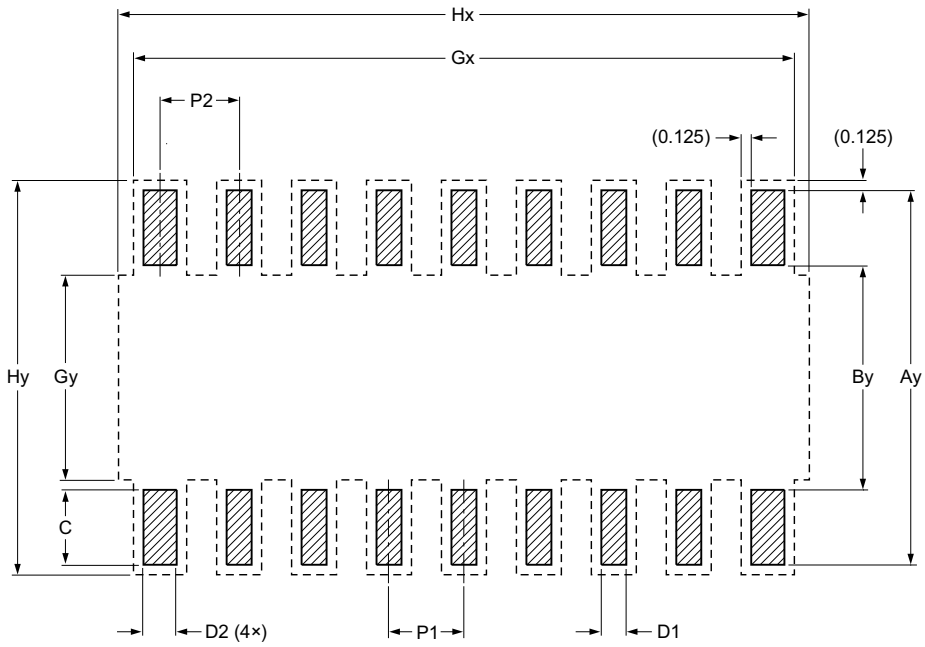
MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Soldering: PCB footprints

Footprint information for reflow soldering of SO16 package **SOT109-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

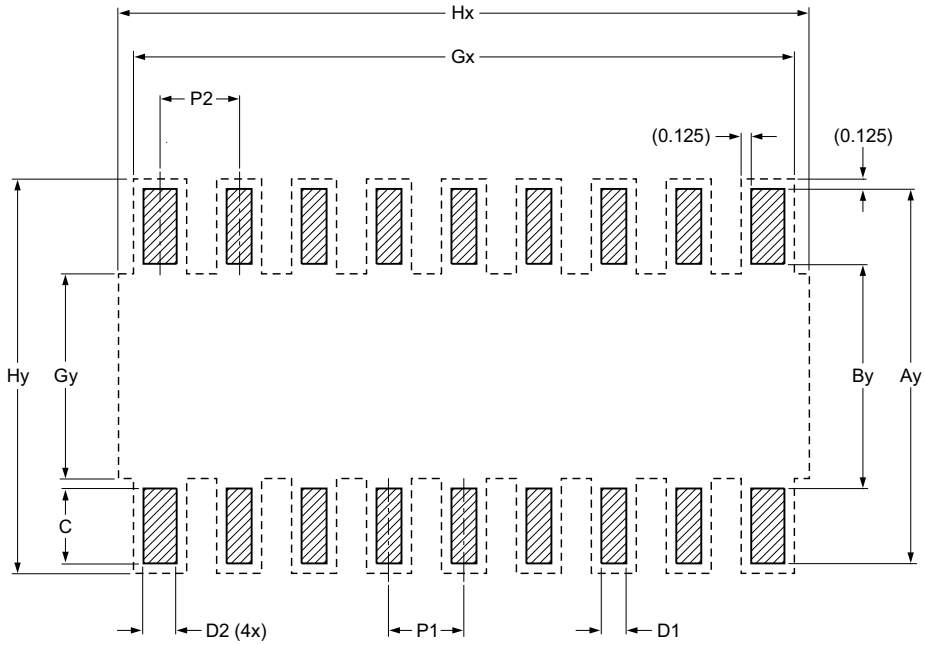
occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	7.400	3.900	1.750	0.700	0.800	10.040	5.200	11.900	7.650

Fig 27. PCB footprint for SOT109-1 (SO16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

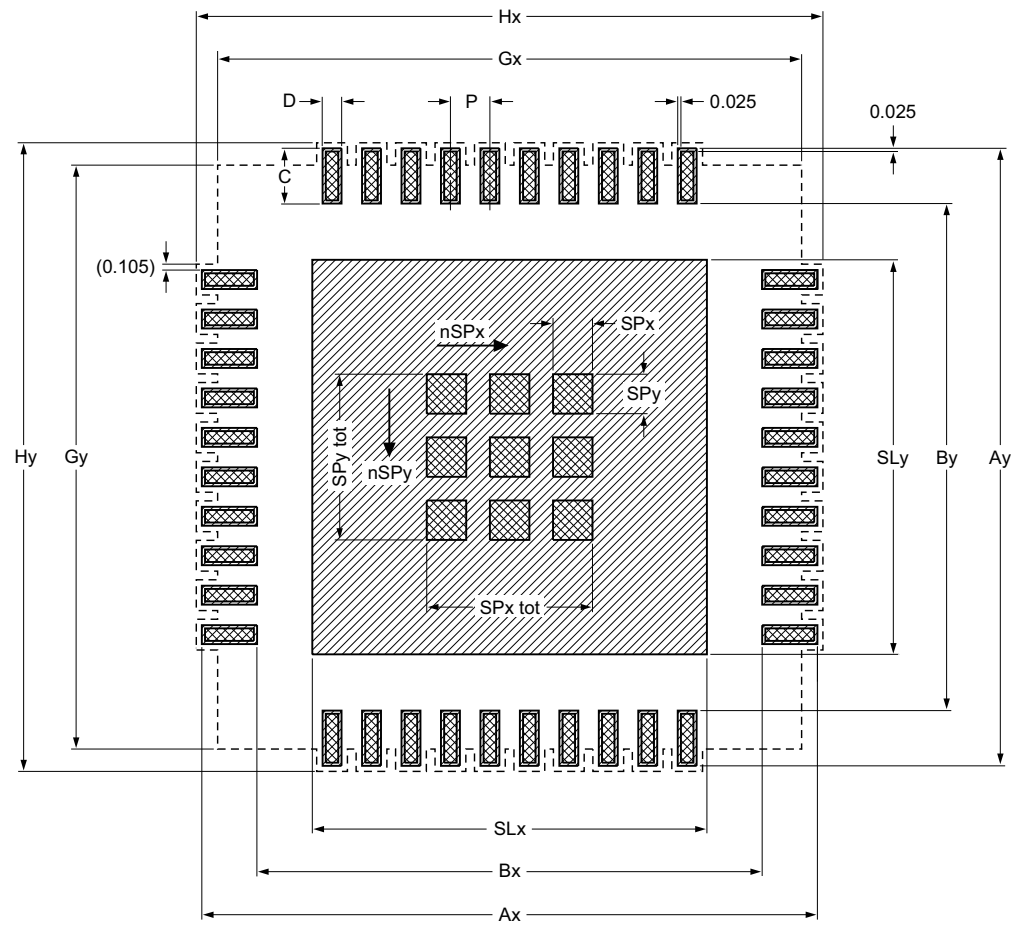
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 28. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of HVQFN16 package **SOT629-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.650	5.000	5.000	2.800	2.800	1.100	0.300	2.000	2.000	1.200	1.200	0.450	0.450	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot629-1_fr*

Fig 29. PCB footprint for SOT629-1 (HVQFN16); reflow soldering

17. Abbreviations

Table 14. Abbreviations

Acronym	Description
CBT	Cross Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

18. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9557 v.7	20131210	Product data sheet	-	PCA9557 v.6
Modifications:	• Section 2 “Features and benefits”, 17th bullet item: deleted phrase “150 V MM per JESD22-A115” • Table 1 “Ordering information”: added column ‘Topside marking’ (moved from Table 2) • Table 2 “Ordering options”: – deleted column ‘Topside mark’ (moved to Table 1) – added columns ‘Orderable part number’, ‘Package’, ‘Packing method’ and ‘Minimum order quantity’ • Table 10 “Static characteristics”, sub-section “Input SCL; input/output SDA”: – I_{OL}: added “V_{DD} = 2.3 V” to Conditions • Table 10 “Static characteristics”, sub-section “I/Os”: – I_{OL}: added “V_{OL} = 0.55 V; V_{DD} = 2.3 V” to Conditions • Table 11 “Dynamic characteristics”, $t_{VD;DAT}$: Unit corrected from “ms” to “µs” (this is a correction to documentation only, no change to device) • Added Section 16 “Soldering: PCB footprints”			
PCA9557 v.6	20080611	Product data sheet	-	PCA9557 v.5
PCA9557 v.5	20070912	Product data sheet	-	PCA9557 v.4
PCA9557 v.4 (9397 750 13336)	20041124	Product data sheet	-	PCA9557 v.3
PCA9557 v.3 (9397 750 10872)	20021213	Product data	ECN 853-2308 29160 of 06 Nov 2002	PCA9557 v.2
PCA9557 v.2 (9397 750 09819)	20020513	Product data	ECN 853-2308 28188 of 13 May 2002	PCA9557 v.1
PCA9557 v.1	20011212	Product data	ECN 853-2308 27449 of 12 Dec 2001	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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