NX5DV330

Quad 1-of-2 video multiplexer/demultiplexer

Rev. 03 — 5 August 2009 Product data sheet

1. General description

The NX5DV330 is a quad 1-of-2 high-speed TTL-compatible video multiplexer/demultiplexer. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise

It has a digital select input (S), four independent inputs/outputs (nY0, nY1), a common input/output (nZ) and an active LOW enable input ($\overline{E}$). When pin $\overline{E}$ is HIGH, the switch is turned off.

Schmitt-trigger action at the enable input ($\overline{E}$) and select input (S) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 4.0 V to 5.5 V.

The NX5DV330 is characterized for operation from –40 °C to +85 °C.

2. Features

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection:
  - HBM JESD22-A114E Class 2A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5DV330D	–40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
NX5DV330DS	–40 °C to +85 °C	SSOP16[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
NX5DV330PW	–40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NX5DV330BQ	–40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

[1] Also known as QSOP16.

4. Functional diagram

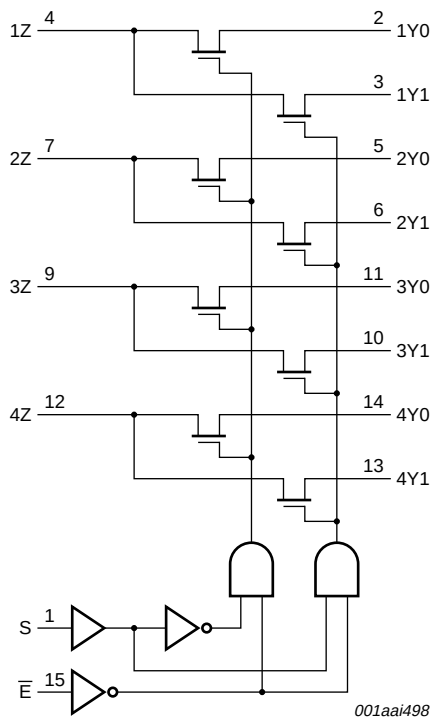


Fig 1. Logic diagram

© NXP B.V. 2009. All rights reserved.

5. Pinning information

5.1 Pinning

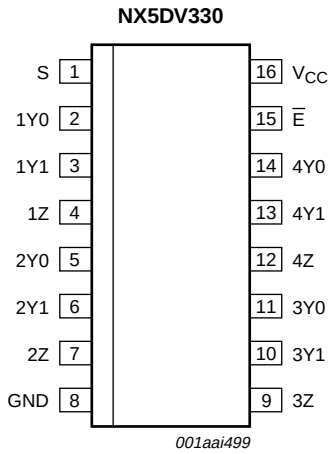


Fig 2. Pin configuration for SOT109-1 (SO16)

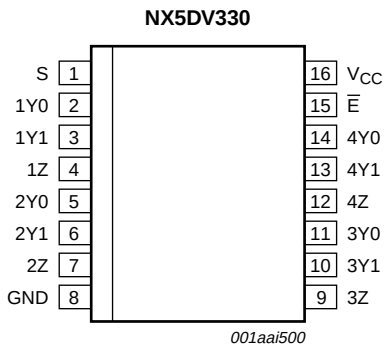


Fig 3. Pin configuration for SOT519-1 (SSOP16)

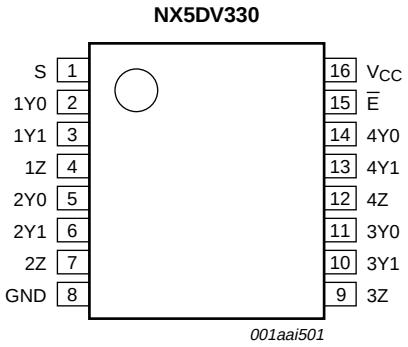


Fig 4. Pin configuration for SOT403-1 (TSSOP16)

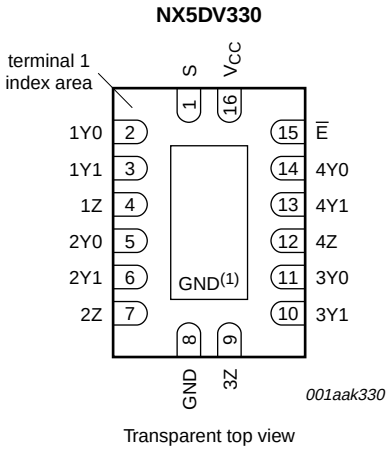


Fig 5. Pin configuration for SOT763-1 (DHVQFN16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1Y0, 1Y1, 2Y0, 2Y1, 3Y1, 3Y0, 4Y1, 4Y0	2, 3, 5, 6, 10, 11, 13, 14	independent input or output
1Z, 2Z, 3Z, 4Z	4, 7, 9, 12	independent input or output
GND	8	ground (0 V)
$\overline{E}$	15	enable input (active LOW)
V_{CC}	16	positive supply voltage

© NXP B.V. 2009. All rights reserved.

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
$\overline{E}$	S	
L	L	Y0 to Z or Z to Y0
L	H	Y1 to Z or Z to Y1
H	X	switch off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–0.5	+7.0	V
I_{SW}	switch current	continuous current through each switch		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[2][3][4]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 (QSOP16) and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.0	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_H	hysteresis voltage	pin S, $\overline{E}$	-	45	-	mV
T_{amb}	ambient temperature	operating in free-air	–40	+25	+85	°C

© NXP B.V. 2009. All rights reserved.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = −18 mA		-	-	−1.2	V
I_I	input leakage current	pin S, $\overline{E}$; V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 5.5 V; V_I = GND; V_O = 0 V to 5.5 V		-	-	±1	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I = V_O = 0 V to 5.5 V		-	-	±1	μA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	-	3	μA
ΔI_{CC}	additional supply current	pin S, $\overline{E}$; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	[2]	-	-	2.5	mA
C_I	input capacitance	pin S, $\overline{E}$; V_I = 5 V or 0 V		-	3.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	Z port; V_{CC} = 5 V; V_O = 5 V or 0 V; $\overline{E}$ = V_{CC}		-	6.0	-	pF
		Y port; V_{CC} = 5 V; V_O = 5 V or 0 V; $\overline{E}$ = V_{CC}		-	4.0	-	pF
$C_{io(on)}$	on-state input/output capacitance	Z port; V_{CC} = 5 V; V_O = 5 V or 0 V; $\overline{E}$ = GND		-	14	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V	[3]				
		V_I = 1.0 V; I_I = 13 mA		-	3	7	Ω
		V_I = 2.0 V; I_I = 26 mA		-	7	10	Ω

[1] All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the Z and the Y terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Z or Y) terminals.

10. Dynamic characteristics

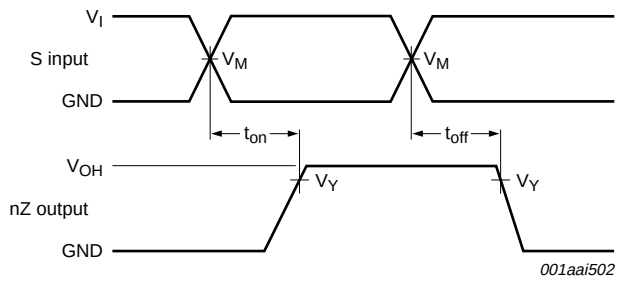
Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{on}	turn-on time	S to nZ; see Figure 6				
		V_{CC} = 4.5 V to 5.5 V	-	4.0	6.0	ns
t_{off}	turn-off time	S to nZ; see Figure 6				
		V_{CC} = 4.5 V to 5.5 V	-	2.3	6.0	ns

© NXP B.V. 2009. All rights reserved.

11. Waveforms



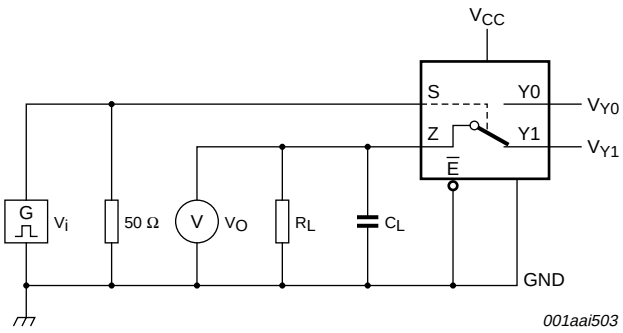
Measurement points are given in Table 8.

V_{OH} is the typical voltage output level that occurs with the output load.

Fig 6. Input (S) to output (nZ) turn-on and turn-off time

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_Y
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	$0.9V_{OH}$



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring turn-on and turn-off times

Table 9. Test data

Input					Load	
V_I	f_i	t_r, t_f	V_{Y0}	V_{Y1}	R_L	C_L
GND to 3.0 V	≤ 10 MHz	≤ 2.5 ns	GND to 3.0 V	3.0 V to GND	75 Ω	20 pF

© NXP B.V. 2009. All rights reserved.

12. Additional dynamic characteristics

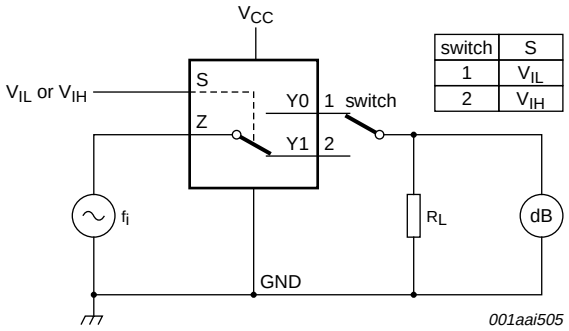
Table 10. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); T_{amb} = 25 °C; V_{CC} = 4.5 V to 5.5 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_{dif}	differential gain	f_i = 3.58 MHz; R_L = 150 Ω		-	0.64	-	%
φ_{dif}	differential phase	f_i = 3.58 MHz; R_L = 150 Ω		-	0.1	-	deg
$f_{(-3dB)}$	–3 dB frequency response	R_L = 150 Ω; see Figure 8		300	-	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 10 MHz; R_L = 150 Ω; see Figure 9		-	–60	-	dB
Xtalk	crosstalk	between switches; see Figure 10; f_i = 10 MHz; R_L = 150 Ω; R_i = 10 Ω	[1]	-	–63	-	dB

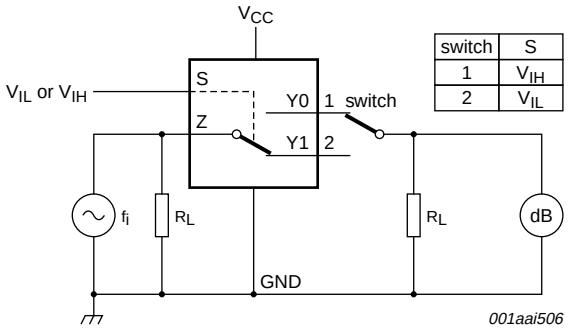
[1] All unused analog input pins (nZ) and outputs pins (nYn) are connected through 10 Ω and 50 Ω pull-down resistors, respectively.

13. Test circuits



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads –3 dB.

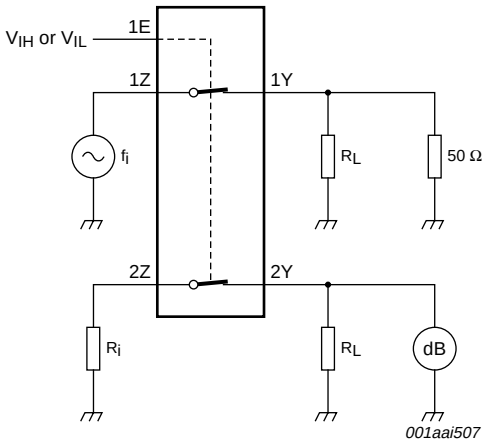
Fig 8. Test circuit for measuring the frequency response when channel is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig 9. Test circuit for measuring isolation (OFF-state)

© NXP B.V. 2009. All rights reserved.



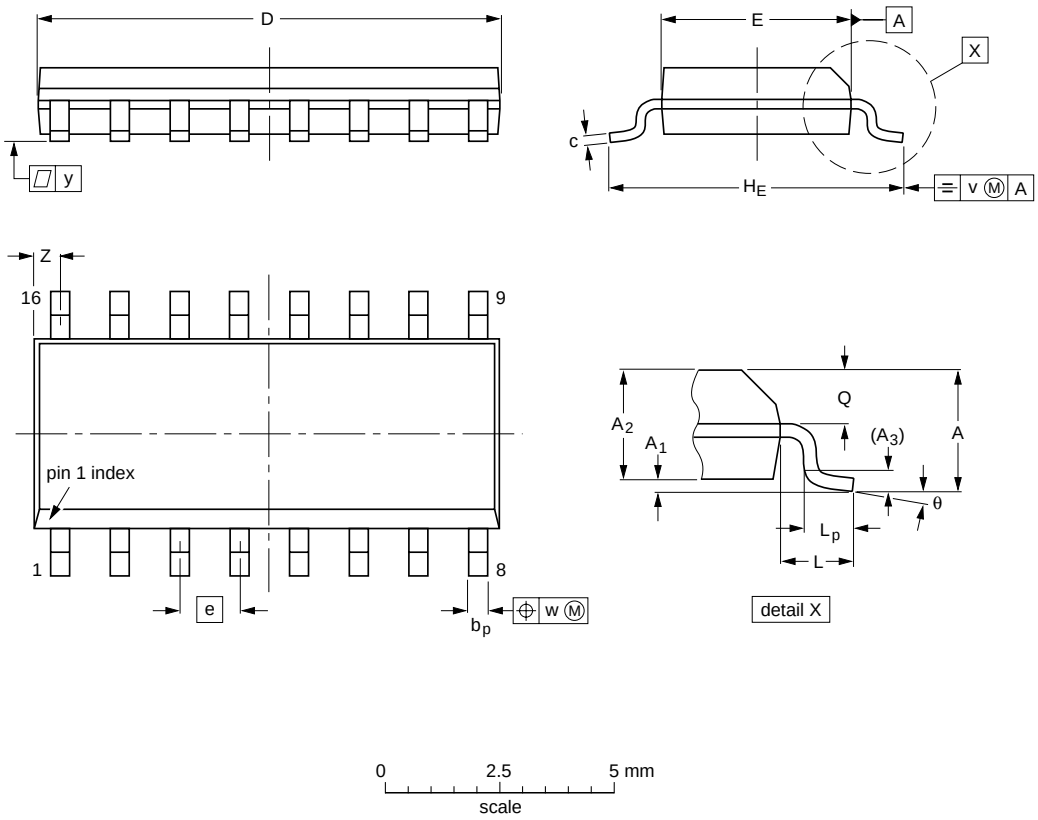
Adjust f_i voltage to obtain 0 dBm level at input.

Fig 10. Test circuit for measuring crosstalk voltage between digital inputs and switch

© NXP B.V. 2009. All rights reserved.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

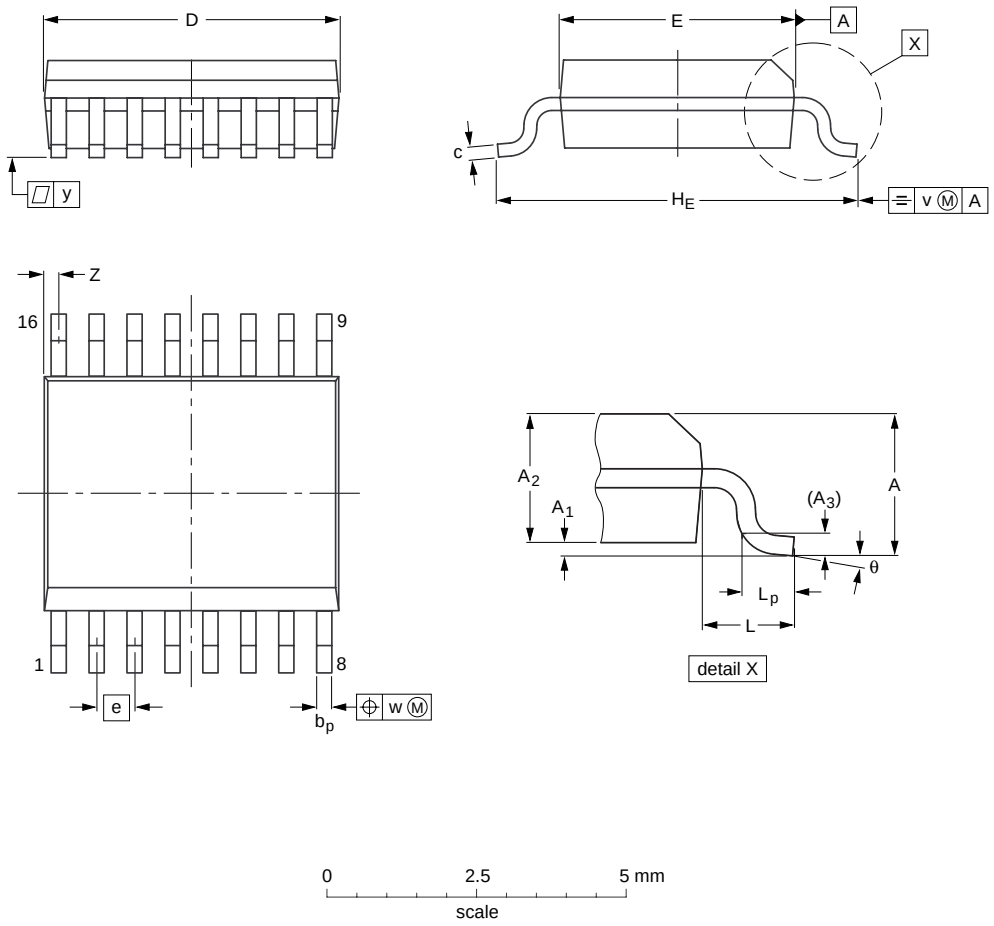
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

© NXP B.V. 2009. All rights reserved.

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

Note

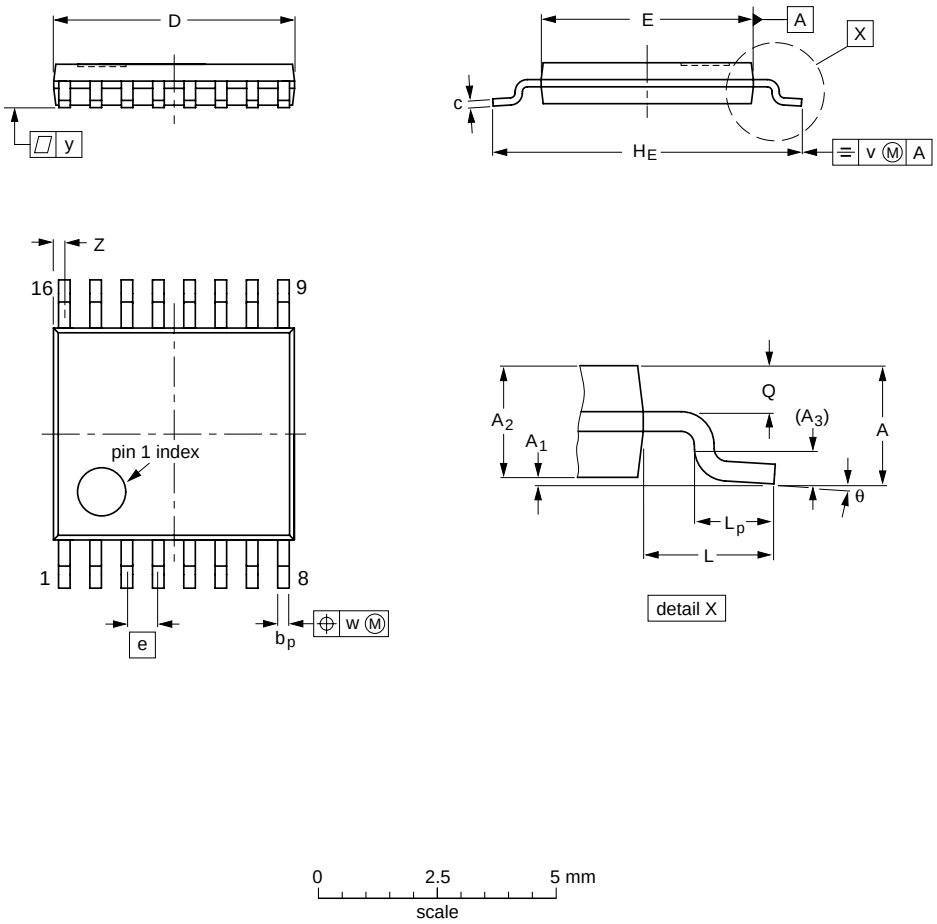
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						~~99-05-04~~ 03-02-18

Fig 12. Package outline SOT519-1 (SSOP16)

© NXP B.V. 2009. All rights reserved.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

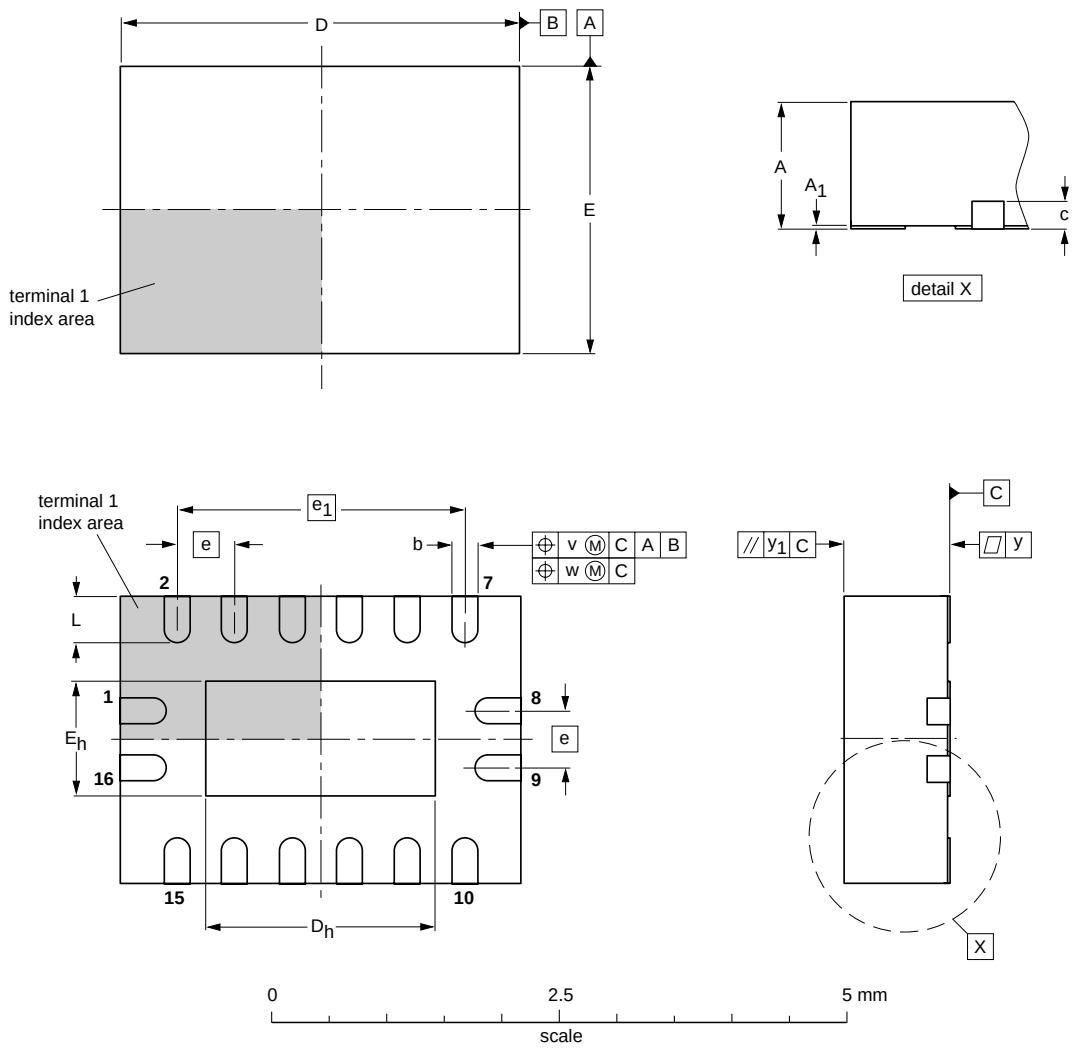
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT403-1 (TSSOP16)

© NXP B.V. 2009. All rights reserved.

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 14. Package outline SOT763-1 (DHVQFN16)

© NXP B.V. 2009. All rights reserved.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5DV330_3	20090805	Product data sheet	-	NX5DV330_2
Modifications:	• Added type number NX5DV330BQ (DHVQFN16 package)			
NX5DV330_2	20080825	Product data sheet	-	NX5DV330_1
NX5DV330_1	20080815	Product data sheet	-	-

© NXP B.V. 2009. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2009. All rights reserved.

19. Contents

1 General description 1
2 Features 1
3 Ordering information 2
4 Functional diagram 2
5 Pinning information 3
5.1 Pinning 3
5.2 Pin description 3
6 Functional description 4
7 Limiting values 4
8 Recommended operating conditions 4
9 Static characteristics 5
10 Dynamic characteristics 5
11 Waveforms 6
12 Additional dynamic characteristics 7
13 Test circuits 7
14 Package outline 9
15 Abbreviations 13
16 Revision history 13
17 Legal information 14
17.1 Data sheet status 14
17.2 Definitions 14
17.3 Disclaimers 14
17.4 Trademarks 14
18 Contact information 14
19 Contents 15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by PHILIPS

© NXP B.V. 2009. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 5 August 2009
Document identifier: NX5DV330_3