

# CBTV4020

20-bit DDR SDRAM 2 : 1 MUX

Rev. 03 — 4 April 2008

Product data sheet

## 1. General description

This 20-bit bus switch is designed for 2.3 V to 2.7 V  $V_{DD}$  operation and SSTL\_2 select input levels.

Each host port pin is multiplexed to one of two DIMM port pins. When the SEL pin is HIGH the A DIMM port is turned on and the B DIMM port is off. The ON-state connects the host port to the DIMM port through a 20  $\Omega$  nominal series resistance. When the port is off a high-impedance state exists between the Host and disabled DIMM. The DIMM port is terminated with a 100  $\Omega$  resistor to ground. When the SEL pin is LOW the B DIMM port is turned on and the A DIMM port is off.

The part incorporates a very low crosstalk design. It has a very low skew between outputs (< 50 ps) and low skew (< 50 ps) for rising and falling edges. The part has optimal performance in DDR data bus applications.

Each switch has been optimized for connection to 1-bank or 2-bank DIMMs.

The low internal RC time constant of the switch (20  $\Omega \times 7$  pF) allows data transfer to be made with minimal propagation delay.

The CBTV4020 is characterized for operation from 0 °C to +85 °C.

## 2. Features

- SEL signal is SSTL\_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Designed to be used with 400 Mbit/s 200 MHz DDR data bus
- Switch ON resistance is designed to eliminate the need for series resistor to DDR SDRAM
- $R_{ON} \sim 20 \Omega$
- Internal 100  $\Omega$  pull-down resistors on DIMM side when path is disabled
- Low differential skew
- Matched rise/fall slew rate
- Low crosstalk
- One DIMM select control line
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 1500 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

3. Quick reference data

Table 1. Quick reference data

| Symbol          | Parameter               | Conditions   | Min   | Typ | Max | Unit |
|-----------------|-------------------------|--|-------|-----|-----|------|
| t <sub>PD</sub> | propagation delay       | from input DHn or DAn/DBn to output DAn/DBn or DHn | [1] - | 140 | -   | ps   |
| C <sub>in</sub> | control pin capacitance | V <sub>I</sub> = 2.5 V or 0 V                      | [2] - | 4   | -   | pF   |
| C <sub>on</sub> | switch on capacitance   | V <sub>I</sub> = 1.5 V                             | [2] - | -   | 10  | pF   |

- [1] The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 20 Ω × 7 pF. Load capacitance = 7 pF. This parameter is not production tested.
- [2] Capacitance values are measured at 10 MHz and a bias voltage 3 V. Capacitance is not production tested.

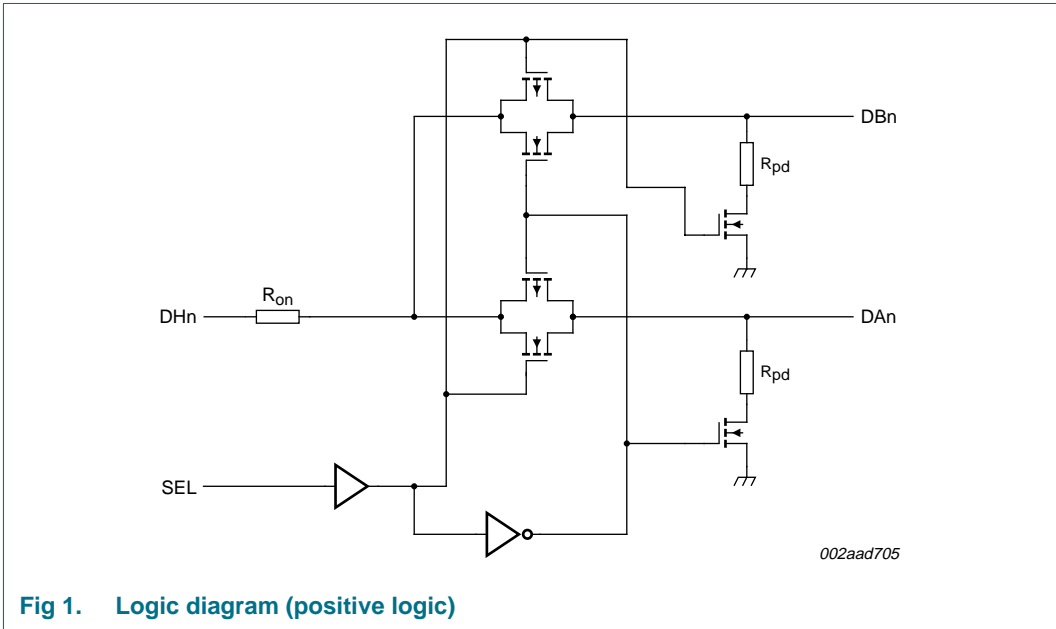
4. Ordering information

Table 2. Ordering information

T<sub>amb</sub> = 0 °C to +85 °C

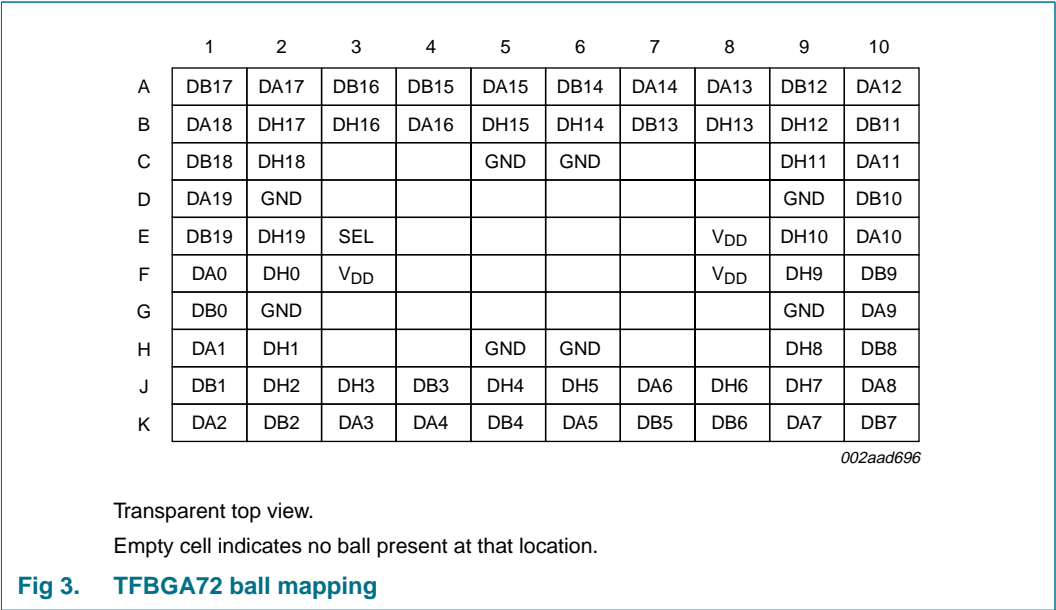
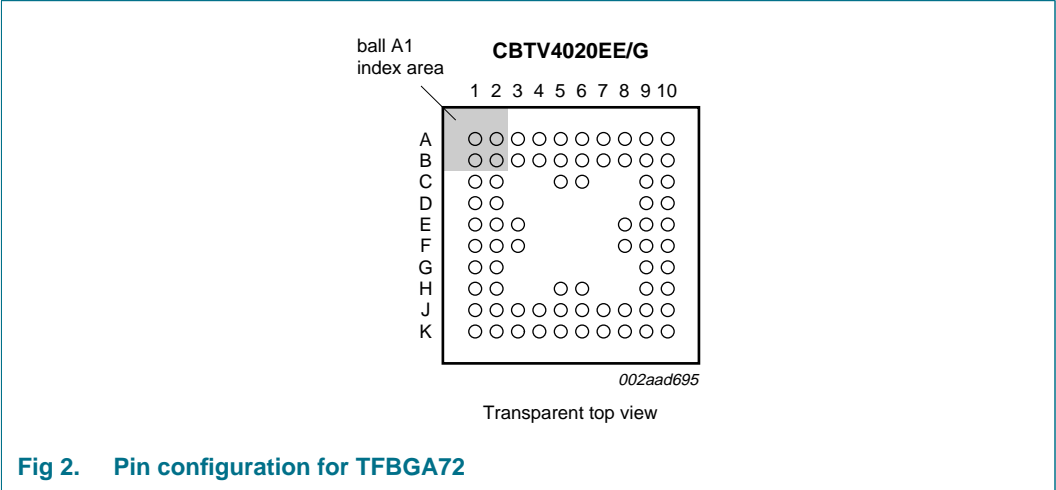
| Type number  | Package |  | Version  |
|--------------|---------|--|----------|
|              | Name    | Description  |          |
| CBTV4020EE/G | TFBGA72 | plastic thin fine-pitch ball grid array package; 72 balls; body 6 × 6 × 0.8 mm | SOT761-1 |

5. Functional diagram



6. Pinning information

6.1 Pinning



## 6.2 Pin description

Table 3. Pin description

| Symbol          | Pin                            | Description             |
|-----------------|--------------------------------|-------------------------|
| DH0             | F2                             | host ports              |
| DH1             | H2                             |                         |
| DH2             | J2                             |                         |
| DH3             | J3                             |                         |
| DH4             | J5                             |                         |
| DH5             | J6                             |                         |
| DH6             | J8                             |                         |
| DH7             | J9                             |                         |
| DH8             | H9                             |                         |
| DH9             | F9                             |                         |
| DH10            | E9                             |                         |
| DH11            | C9                             |                         |
| DH12            | B9                             |                         |
| DH13            | B8                             |                         |
| DH14            | B6                             |                         |
| DH15            | B5                             |                         |
| DH16            | B3                             |                         |
| DH17            | B2                             |                         |
| DH18            | C2                             |                         |
| DH19            | E2                             |                         |
| SEL             | E3                             | select                  |
| GND             | C5, C6, D2, D9, G2, G9, H5, H6 | ground                  |
| V <sub>DD</sub> | E8, F3, F8                     | positive supply voltage |
| DA0             | F1                             | A DIMM ports            |
| DA1             | H1                             |                         |
| DA2             | K1                             |                         |
| DA3             | K3                             |                         |
| DA4             | K4                             |                         |
| DA5             | K6                             |                         |
| DA6             | J7                             |                         |
| DA7             | K9                             |                         |
| DA8             | J10                            |                         |
| DA9             | G10                            |                         |
| DA10            | E10                            |                         |
| DA11            | C10                            |                         |
| DA12            | A10                            |                         |
| DA13            | A8                             |                         |
| DA14            | A7                             |                         |
| DA15            | A5                             |                         |

**Table 3.** Pin description ...continued

| Symbol | Pin | Description              |
|--------|-----|--------------------------|
| DA16   | B4  | A DIMM ports (continued) |
| DA17   | A2  |                          |
| DA18   | B1  |                          |
| DA19   | D1  |                          |
| DB0    | G1  | B DIMM ports             |
| DB1    | J1  |                          |
| DB2    | K2  |                          |
| DB3    | J4  |                          |
| DB4    | K5  |                          |
| DB5    | K7  |                          |
| DB6    | K8  |                          |
| DB7    | K10 |                          |
| DB8    | H10 |                          |
| DB9    | F10 |                          |
| DB10   | D10 |                          |
| DB11   | B10 |                          |
| DB12   | A9  |                          |
| DB13   | B7  |                          |
| DB14   | A6  |                          |
| DB15   | A4  |                          |
| DB16   | A3  |                          |
| DB17   | A1  |                          |
| DB18   | C1  |                          |
| DB19   | E1  |                          |

## 7. Functional description

Refer to [Figure 1 “Logic diagram \(positive logic\)”](#).

### 7.1 Function selection

**Table 4.** Function selection

*H = HIGH voltage level; L = LOW voltage level.*

| Input SEL | Function   |
|-----------|--|
| L         | host port = B DIMM port<br>A DIMM port = 100 $\Omega$ to GND |
| H         | host port = A DIMM port<br>B DIMM port = 100 $\Omega$ to GND |

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*The package thermal impedance is calculated in accordance with JESD 51.*

| Symbol    | Parameter              | Conditions      | Min      | Max            | Unit |
|-----------|------------------------|-----------------|----------|----------------|------|
| $V_{DD}$  | supply voltage         |                 | -0.5     | +3.3           | V    |
| $I_{IK}$  | input clamping current | $V_{I/O} < 0$ V | -50      | -              | mA   |
| $V_I$     | input voltage          | SEL pin only    | [1] -0.3 | $V_{DD} + 0.3$ | V    |
|           |                        | except SEL pin  | [1] -0.5 | +3.3           | V    |
| $T_{stg}$ | Storage temperature    |                 | -65      | +150           | °C   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamping current ratings are observed.

## 9. Recommended operating conditions

**Table 6. Operating conditions**

*All unused control inputs of the device must be held at  $V_{DD}$  or GND to ensure proper device operation.*

| Symbol    | Parameter                | Conditions               | Min | Typ | Max | Unit |
|-----------|--------------------------|--------------------------|-----|-----|-----|------|
| $V_{DD}$  | supply voltage           |                          | 2.3 | 2.5 | 2.7 | V    |
| $V_{IH}$  | HIGH-level input voltage | DIMM port and host (SEL) | 1.6 | -   | -   | V    |
| $V_{IL}$  | LOW-level input voltage  | DIMM port and host (SEL) | -   | -   | 0.9 | V    |
| $T_{amb}$ | ambient temperature      | operating in free air    | 0   | -   | 85  | °C   |

## 10. Static characteristics

**Table 7. Static characteristics**

$T_{amb} = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| Symbol   | Parameter                | Conditions  | Min               | Typ <sup>[1]</sup> | Max       | Unit          |
|----------|--------------------------|---|-------------------|--------------------|-----------|---------------|
| $V_{IK}$ | input clamping current   | $V_{DD} = 2.3\text{ V}$ ; $I_I = -18\text{ mA}$                           | -                 | -                  | -1.2      | V             |
| $I_{LI}$ | input leakage current    | $V_{DD} = 2.5\text{ V}$ ; $V_I = V_{DD}$ or GND;<br>SEL = GND or $V_{DD}$ |                   |                    |           |               |
|          |                          | SEL   | -                 | -                  | $\pm 100$ | $\mu\text{A}$ |
|          |                          | host port   | <sup>[2]</sup> -  | -                  | $\pm 100$ | $\mu\text{A}$ |
|          |                          | SEL = GND for $I_{LI}$ (test)   |                   |                    |           |               |
|          |                          | DIMM port   | <sup>[2]</sup> -  | -                  | $\pm 100$ | $\mu\text{A}$ |
| $I_{DD}$ | supply current           | $V_{DD} = 2.5\text{ V}$ ; $I_O = 0\text{ mA}$ ; $V_I = V_{DD}$ or GND     | -                 | 55                 | 150       | $\mu\text{A}$ |
| $I_{OL}$ | LOW-level output current | on DBn or DAn; $V_{OL} = 1\text{ V}$                                      | <sup>[3]</sup> -  | 9.5                | -         | mA            |
| $C_{in}$ | control pin capacitance  | $V_I = 2.5\text{ V}$ or $0\text{ V}$                                      | <sup>[4]</sup> -  | 4                  | -         | pF            |
| $C_{on}$ | switch on capacitance    | $V_I = 1.5\text{ V}$  | <sup>[4]</sup> -  | -                  | 10        | pF            |
| $R_{ON}$ | ON resistance            | $V_{DD} = 2.5\text{ V}$ ; $V_A = 0.8\text{ V}$ ; $V_B = 1.0\text{ V}$     | <sup>[5]</sup> 16 | 20                 | 30        | $\Omega$      |
|          |                          | $V_{DD} = 2.5\text{ V}$ ; $V_A = 1.7\text{ V}$ ; $V_B = 1.5\text{ V}$     | <sup>[5]</sup> 16 | 20                 | 30        | $\Omega$      |
| $R_{pd}$ | pull-down resistance     | output; DAn (SEL = GND) or<br>DBn (SEL = $V_{DD}$ ) = $0.5V_{DD}$         | <sup>[3]</sup> -  | 105                | -         | $\Omega$      |

[1] All typical values are at  $V_{DD} = 2.5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ .

[2] When SEL is HIGH, DBn must be open and DAn can be HIGH or LOW. When SEL is LOW, DAn must be open and DBn can be HIGH or LOW.

[3] SEL = GND for testing DAn, and SEL =  $V_{DD}$  for testing DBn.

[4] Capacitance values are measured at 10 MHz and a bias voltage 3 V. Capacitance is not production tested.

[5] Measured by the current between the host and the DIMM terminals at the indicated voltages on each side of the switch.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

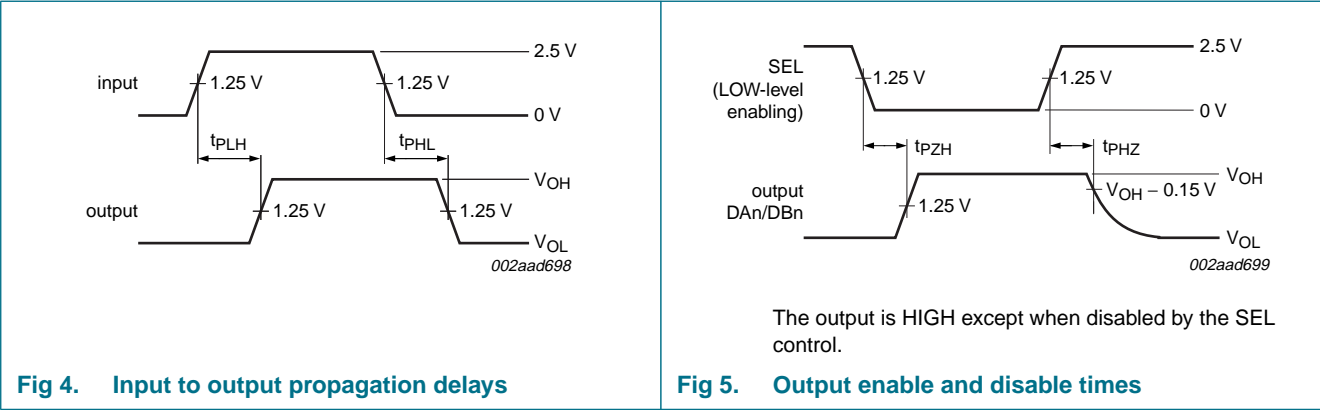
$V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$ .

| Symbol         | Parameter         | Conditions   | Min              | Typ | Max | Unit |
|----------------|-------------------|--|------------------|-----|-----|------|
| $t_{PD}$       | propagation delay | from input DHn or DAn/DBn<br>to output DAn/DBn or DHn  | <sup>[1]</sup> - | 140 | -   | ps   |
| $t_{en}$       | enable time       | from input SEL to output DAn/DBn or DHn  | 1                | -   | 2   | ns   |
| $t_{dis}$      | disable time      | from input SEL to output DAn/DBn or DHn  | 1                | -   | 3   | ns   |
| $t_{sk(o)}$    | output skew time  | any output to any output; <a href="#">Figure 7</a>   | <sup>[2]</sup> - | 25  | 50  | ps   |
| $t_{sk(edge)}$ | edge skew time    | difference of rising edge propagation delay<br>and falling edge propagation delay;<br><a href="#">Figure 8</a> | <sup>[2]</sup> - | 25  | 50  | ps   |

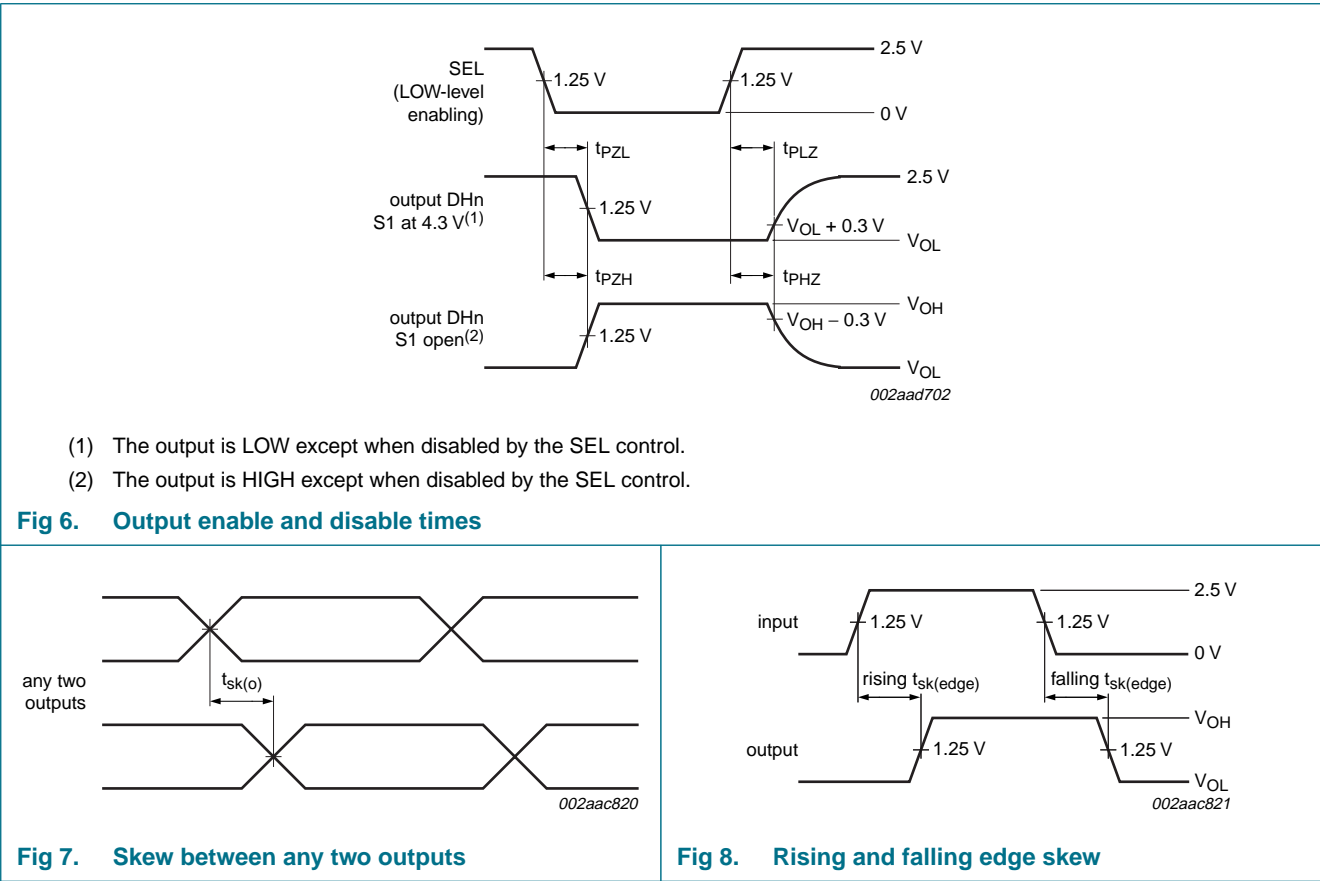
[1] The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance);  $20\text{ }\Omega \times 7\text{ pF}$ . Load capacitance = 7 pF. This parameter is not production tested.

[2] Skew is not production tested.

11.1 DHn to DAn/DBn AC waveforms



11.2 DAn/DBn to DHn AC waveforms





12. Test information

All input pulses are supplied by generators having the following characteristics:  
 $PRR \leq 10\text{ MHz}$ ;  $Z_o = 50\ \Omega$ ;  $t_r \leq 2.5\text{ ns}$ ;  $t_f \leq 2.5\text{ ns}$ .

The outputs are measured one at a time with one transition per measurement.

$C_L$  = load capacitance; includes jig and probe capacitance.

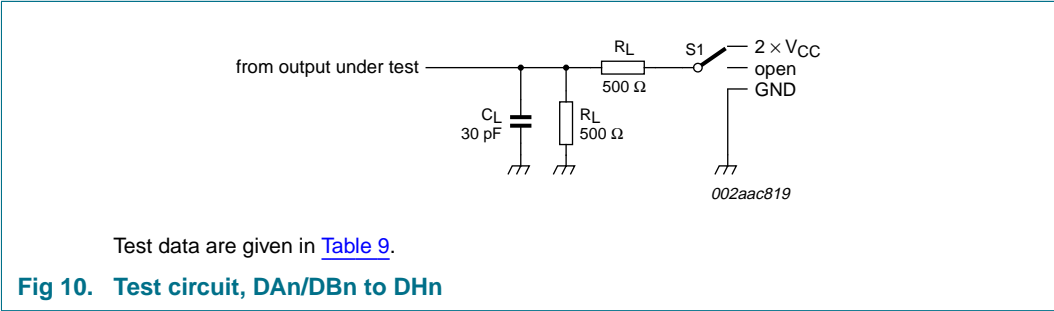
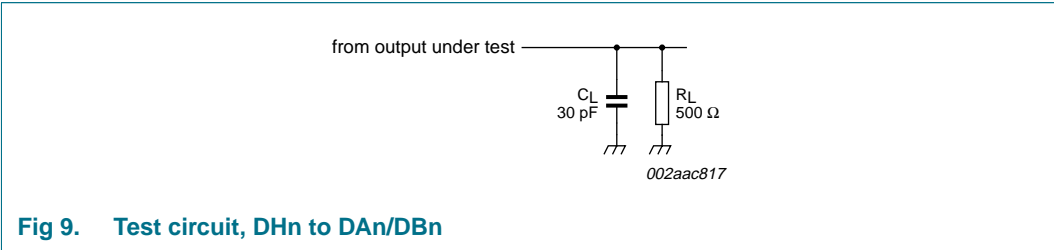


Table 9. Test data

| Test                  | Load  |              | Switch S1         |
|-----------------------|-------|--------------|-------------------|
|                       | $C_L$ | $R_L$        |                   |
| $t_{PD}$              | 30 pF | 500 $\Omega$ | open              |
| $t_{PLZ}$ , $t_{PZL}$ | 30 pF | 500 $\Omega$ | $2 \times V_{CC}$ |
| $t_{PHZ}$ , $t_{PZH}$ | 30 pF | 500 $\Omega$ | GND               |

13. Package outline

TFBGA72: plastic thin fine-pitch ball grid array package; 72 balls; body 6 x 6 x 0.8 mmSOT761-1

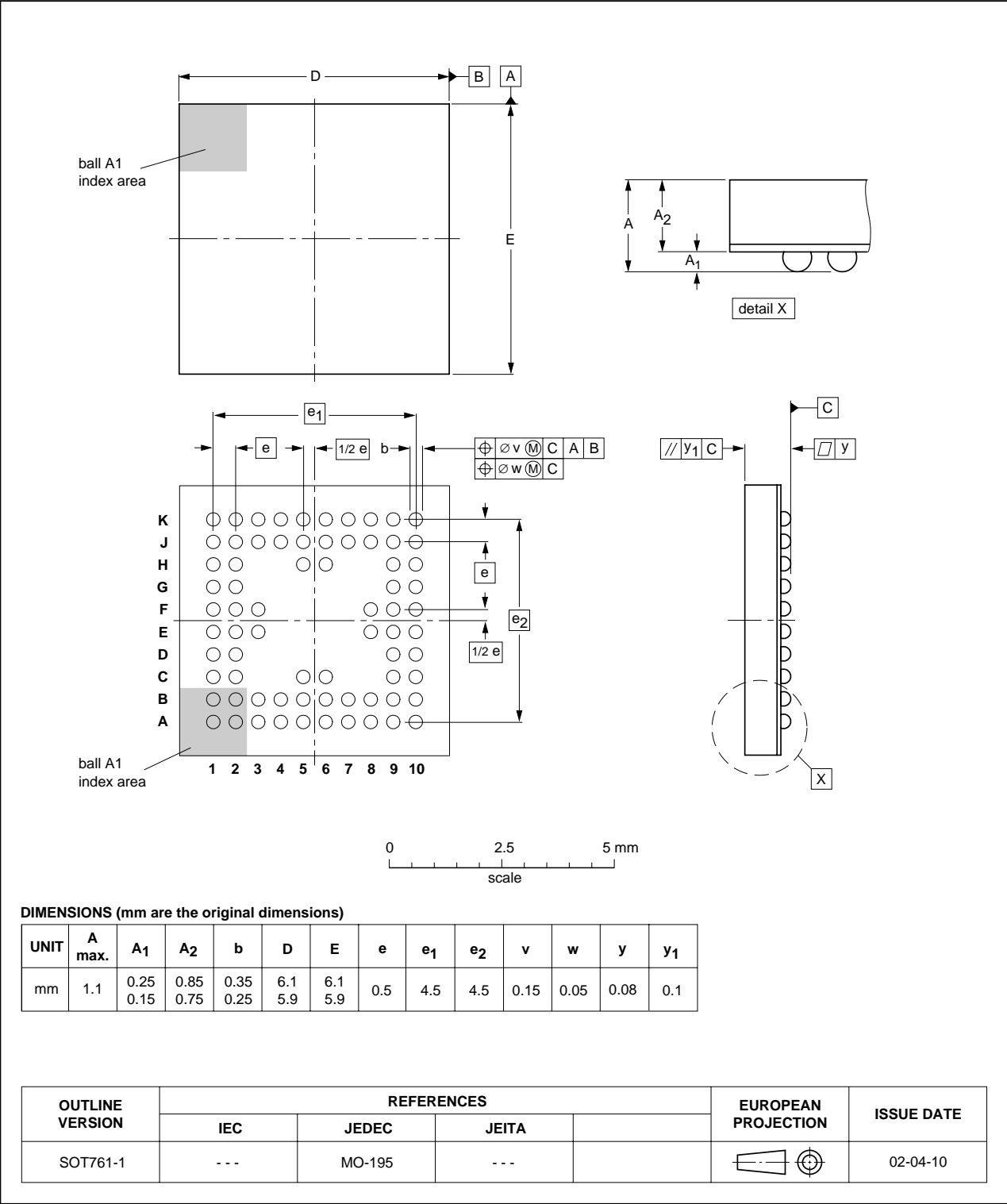


Fig 11. Package outline SOT761-1 (TFBGA72)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 12](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

**Table 10. SnPb eutectic process (from J-STD-020C)**

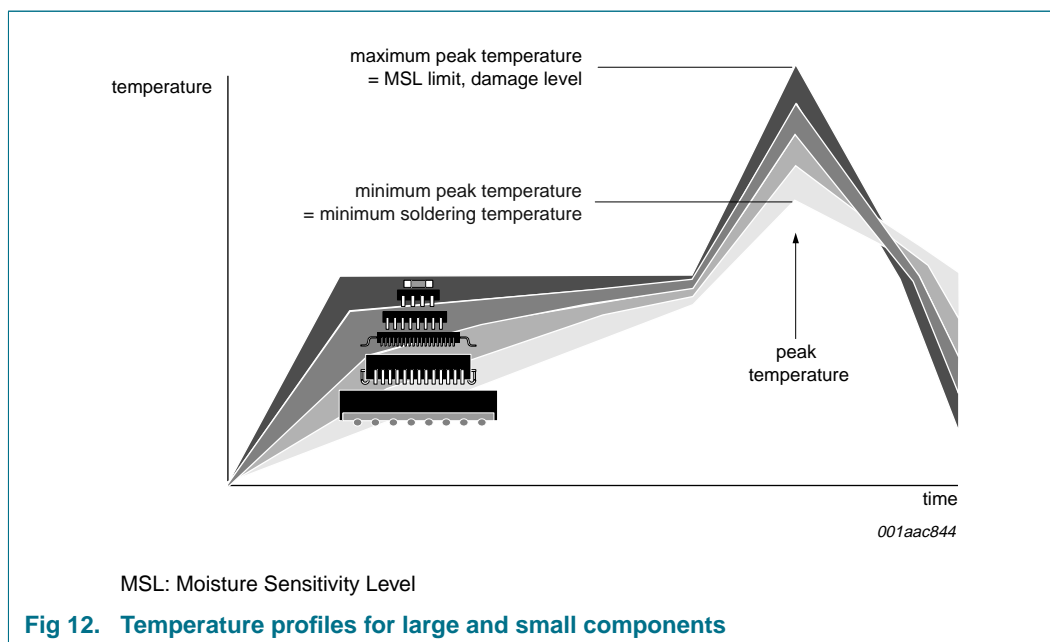
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 11. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 12](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description                              |
|---------|--|
| CDM     | Charged-Device Model                     |
| DDR     | Double Data Rate                         |
| DIMM    | Dual In-Line Memory Module               |
| ESD     | ElectroStatic Discharge                  |
| HBM     | Human Body Model                         |
| MM      | Machine Model                            |
| PRR     | Pulse Repetition Rate                    |
| RC      | Resistor-Capacitor network               |
| SDRAM   | Synchronous Dynamic Random Access Memory |
| SSTL_2  | Stub Series Terminated Logic for 2.5 V   |

## 16. Revision history

**Table 13. Revision history**

| Document ID                      | Release date  | Data sheet status  | Change notice                        | Supersedes   |
|----------------------------------|---|--------------------|--------------------------------------|--------------|
| CBTV4020_3                       | 20080404  | Product data sheet | -                                    | CBTV4020_N_2 |
| Modifications:                   | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2 “Features”</a>: <ul style="list-style-type: none"> <li>5<sup>th</sup> bullet item: changed “r<sub>on</sub>” to “R<sub>ON</sub>”</li> <li>9<sup>th</sup> bullet item: changed from “Low cross-talk data-data/data-DQM” to “Low crosstalk”</li> </ul> </li> <li><a href="#">Section 3 “Quick reference data”</a> re-written (rows are now direct copies from <a href="#">Table 7 “Static characteristics”</a> and <a href="#">Table 8 “Dynamic characteristics”</a>)</li> <li><a href="#">Table 2 “Ordering information”</a>: deleted type number CBTV4020EE</li> <li>Added <a href="#">Figure 2 “Pin configuration for TFBGA72”</a></li> <li><a href="#">Table 3 “Pin description”</a>: expanded to detail pin assignments</li> <li><a href="#">Table 5 “Limiting values”</a>: <ul style="list-style-type: none"> <li>deleted (old) Table note [1] (this statement now given in <a href="#">Section 17.3 “Disclaimers”</a>)</li> <li>under conditions for V<sub>I</sub>: changed “S pin” to “SEL pin”</li> <li>separated Min and Max values</li> </ul> </li> <li><a href="#">Table 7 “Static characteristics”</a>: <ul style="list-style-type: none"> <li>changed symbol for “input leakage current” from “I<sub>I</sub>” to “I<sub>LI</sub>”</li> <li>changed symbol from “r<sub>on</sub>” to “R<sub>ON</sub>”</li> <li>changed symbol from “r<sub>pd</sub>” to “R<sub>pd</sub>”</li> <li>under Conditions for R<sub>pd</sub>, changed “An” to “DAn” and changed “Bn” to “DBn”</li> </ul> </li> <li><a href="#">Table 8 “Dynamic characteristics”</a>: <ul style="list-style-type: none"> <li>changed symbol from “t<sub>pd</sub>” to “t<sub>PD</sub>”</li> <li>changed symbol from “t<sub>osk</sub>” to “t<sub>sk(o)</sub>”</li> <li>changed symbol from “t<sub>esk</sub>” to “t<sub>sk(edge)</sub>”</li> </ul> </li> <li>added information on soldering SMD packages</li> <li>added <a href="#">Section 15 “Abbreviations”</a></li> </ul> |                    |                                      |              |
| CBTV4020_N_2<br>(9397 750 13594) | 20060515  | Product data sheet | -                                    | CBTV4020_N_1 |
| CBTV4020_N_1<br>(9397 750 10411) | 20020927  | Product data       | ECN 853-2387 28989<br>of 2002 Sep 26 | -            |

## 17. Legal information

### 17.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 17.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

### 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 19. Contents

|           |   |           |
|-----------|---|-----------|
| <b>1</b>  | <b>General description</b> .....              | <b>1</b>  |
| <b>2</b>  | <b>Features</b> .....                         | <b>1</b>  |
| <b>3</b>  | <b>Quick reference data</b> .....             | <b>2</b>  |
| <b>4</b>  | <b>Ordering information</b> .....             | <b>2</b>  |
| <b>5</b>  | <b>Functional diagram</b> .....               | <b>2</b>  |
| <b>6</b>  | <b>Pinning information</b> .....              | <b>3</b>  |
| 6.1       | Pinning .....                                 | 3         |
| 6.2       | Pin description .....                         | 4         |
| <b>7</b>  | <b>Functional description</b> .....           | <b>5</b>  |
| 7.1       | Function selection .....                      | 5         |
| <b>8</b>  | <b>Limiting values</b> .....                  | <b>6</b>  |
| <b>9</b>  | <b>Recommended operating conditions</b> ..... | <b>6</b>  |
| <b>10</b> | <b>Static characteristics</b> .....           | <b>7</b>  |
| <b>11</b> | <b>Dynamic characteristics</b> .....          | <b>7</b>  |
| 11.1      | DHn to DAn/DBn AC waveforms .....             | 8         |
| 11.2      | DAn/DBn to DHn AC waveforms .....             | 8         |
| <b>12</b> | <b>Test information</b> .....                 | <b>9</b>  |
| <b>13</b> | <b>Package outline</b> .....                  | <b>10</b> |
| <b>14</b> | <b>Soldering of SMD packages</b> .....        | <b>11</b> |
| 14.1      | Introduction to soldering .....               | 11        |
| 14.2      | Wave and reflow soldering .....               | 11        |
| 14.3      | Wave soldering .....                          | 11        |
| 14.4      | Reflow soldering .....                        | 12        |
| <b>15</b> | <b>Abbreviations</b> .....                    | <b>13</b> |
| <b>16</b> | <b>Revision history</b> .....                 | <b>14</b> |
| <b>17</b> | <b>Legal information</b> .....                | <b>15</b> |
| 17.1      | Data sheet status .....                       | 15        |
| 17.2      | Definitions .....                             | 15        |
| 17.3      | Disclaimers .....                             | 15        |
| 17.4      | Trademarks .....                              | 15        |
| <b>18</b> | <b>Contact information</b> .....              | <b>15</b> |
| <b>19</b> | <b>Contents</b> .....                         | <b>16</b> |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

**PHILIPS**

© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 4 April 2008

Document identifier: CBTV4020\_3