CBTL06DP211

DisplayPort Gen1 2 : 1 multiplexer

Rev. 1 — 21 February 2011 Product data sheet

1. General description

CBTL06DP211 is a multi-channel high-speed multiplexer meant for DisplayPort (DP) v1.1a or Embedded DisplayPort applications operating at data rate of 1.62 Gbit/s or 2.7 Gbit/s. It is designed using NXP proprietary high-bandwidth pass-gate technology and it can be used for 1 : 2 switching or 2 : 1 multiplexing of four high-speed differential AC-coupled DP channels. Further, it is capable of switching/multiplexing of Hot Plug Detect (HPD) signal as well as Auxiliary (AUX) and Display Data Channel (DDC) signals. In order to support GPUs/CPUs that have dedicated AUX and DDC I/Os, CBTL06DP211 provides an additional level of multiplexing of AUX and DDC signals delivering true flexibility and choice.

CBTL06DP211 consumes very low current in operational mode (less than 1 mA typical) and provides for a shutdown function (ultra low current consumption less than 10 μA) to support power-sensitive or battery-powered applications. It is designed for delivering optimum performance at DP data rates of 1.62 Gbit/s and 2.7 Gbit/s.

A typical application of CBTL06DP211 is on motherboards where one of two GPU display sources needs to be selected to connect to a display sink device or connector. A controller chip selects which path to use by setting a select signal HIGH or LOW. Due to the non-directional nature of the signal paths (which use high-bandwidth pass-gate technology), the CBTL06DP211 can also be used in the reverse topology, e.g., to connect one display source device to one of two display sink devices or connectors.

Optionally, the CBTL06DP211 can be used in conjunction with an HDMI/DVI level shifter device (PTN3360A/B or PTN3360D) to allow for DisplayPort as well as HDMI/DVI connectivity.

2. Features and benefits

- 1 : 2 switching or 2 : 1 multiplexing of DisplayPort (v1.1a - 1.62 Gbit/s or 2.7 Gbit/s)
    - 4 high-speed differential channels with 2 : 1 multiplexing/switching for DisplayPort signals
    - 1 channel with 4 : 1 multiplexing/switching for AUX differential signals and DDC single-ended clock and data signals
    - 1 channel with 2 : 1 multiplexing/switching for single-ended HPD signals
- High-bandwidth analog pass-gate technology
- Very low lane intra-pair skew (5 ps typical)
- Very low inter-pair skew (< 180 ps)
- Switch/multiplexer position select CMOS input
- Shutdown mode CMOS input
- Shutdown mode delivers ultra low power consumption

- DDC and AUX ports tolerant to being pulled to +5 V via 2.2 kΩ resistor
  - Supports HDMI/DVI incorrect dongle connection
- Single 3.3 V power supply
- Very low operation current of 0.2 mA typical
- Very low shutdown current of < 10 μA
- ESD 8 kV HBM, 1 kV CDM
- ESD 2 kV HBM, 500 V CDM for control pins
- Available in 5 mm × 5 mm, 0.5 mm ball pitch TFBGA48 package

3. Applications

- Motherboard applications requiring DisplayPort and PCI Express switching/multiplexing
- Docking stations
- Notebook computers
- Chip sets requiring flexible allocation of PCI Express or DisplayPort I/O pins to board connectors

4. Ordering information

Table 1. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
CBTL06DP211EE	Pb-free (SnAgCu solder compound)	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 5 × 5 × 0.8 mm[1]	SOT918-1

[1] Total height including solder balls after printed-circuit board mounting = 1.15 mm.

5. Functional diagram

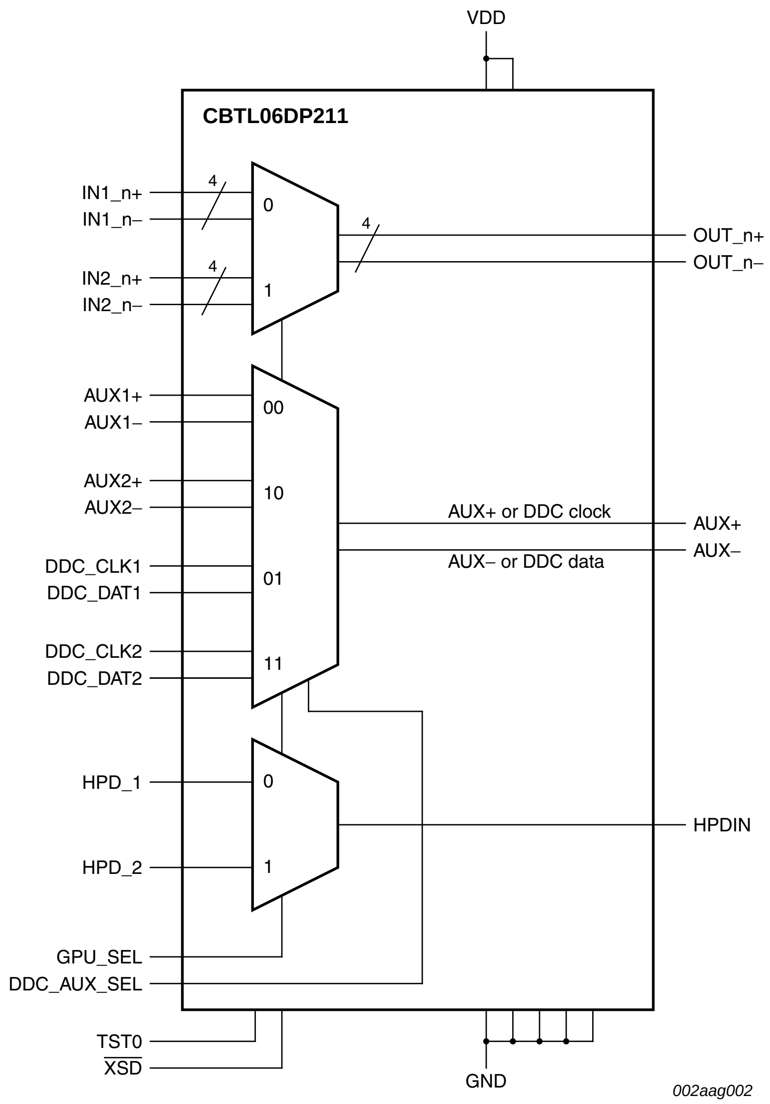
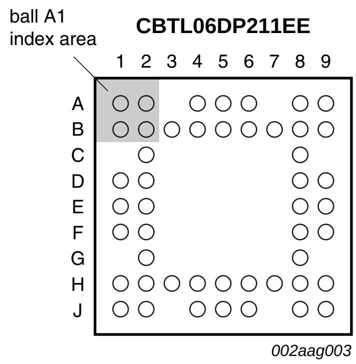


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for TFBGA48

	1	2	3	4	5	6	7	8	9
A	GPU_SEL	VDD		IN1_0–	IN1_1–	IN1_2–		IN1_3+	IN1_3–
B	OUT_0–	OUT_0+	GND	IN1_0+	IN1_1+	IN1_2+	$\overline{\text{XSD}}$	IN2_0+	IN2_0–
C		DDC_AUX _SEL						GND	
D	OUT_1–	OUT_1+						IN2_1+	IN2_1–
E	OUT_2–	OUT_2+						IN2_2+	IN2_2–
F	OUT_3–	OUT_3+						IN2_3+	IN2_3–
G		TST0						GND	
H	AUX–	AUX+	HPD_2	GND	DDC_CLK2	AUX2+	GND	DDC_CLK1	AUX1+
J	HPDIN	HPD_1		VDD	DDC_DAT2	AUX2–		DDC_DAT1	AUX1–

002aag004

Transparent top view

Fig 3. Ball mapping

6.2 Pin description

Table 2. Pin description

Symbol	Ball	Type	Description
GPU_SEL	A1	3.3 V low-voltage CMOS single-ended input	Selects between two multiplexer/switch paths. When HIGH, path 2 left-side is connected to its corresponding right-side I/O. When LOW, path 1 left-side is connected to its corresponding right-side I/O.
DDC_AUX_SEL	C2	3.3 V low-voltage CMOS single-ended input	Selects between DDC and AUX paths. When HIGH, the DDC_CLKn and DDC_DATn I/Os are connected to their respective AUX terminals. When LOW, the AUX+ and AUX– I/Os are connected to their respective AUX terminals.
$\overline{\text{XSD}}$	B7	3.3 V low-voltage CMOS single-ended input	Shutdown pin. Should be driven HIGH or connected to VDD for normal operation. When LOW, all paths are switched off (non-conducting) and supply current consumption is minimized.
TST0	G2	3.3 V low-voltage CMOS single-ended input	Test pin for NXP use only. Should be tied to ground in normal operation.
IN1_0+	B4	differential I/O	Four high-speed differential pairs for DisplayPort or PCI Express signals, path 1, left-side.
IN1_0–	A4	differential I/O	
IN1_1+	B5	differential I/O	
IN1_1–	A5	differential I/O	
IN1_2+	B6	differential I/O	
IN1_2–	A6	differential I/O	
IN1_3+	A8	differential I/O	
IN1_3–	A9	differential I/O	
IN2_0+	B8	differential I/O	Four high-speed differential pairs for DisplayPort or PCI Express signals, path 2, left-side.
IN2_0–	B9	differential I/O	
IN2_1+	D8	differential I/O	
IN2_1–	D9	differential I/O	
IN2_2+	E8	differential I/O	
IN2_2–	E9	differential I/O	
IN2_3+	F8	differential I/O	
IN2_3–	F9	differential I/O	
OUT_0+	B2	differential I/O	Four high-speed differential pairs for DisplayPort or PCI Express signals, right-side.
OUT_0–	B1	differential I/O	
OUT_1+	D2	differential I/O	
OUT_1–	D1	differential I/O	
OUT_2+	E2	differential I/O	
OUT_2–	E1	differential I/O	
OUT_3+	F2	differential I/O	
OUT_3–	F1	differential I/O	
AUX1+	H9	differential I/O	High-speed differential pair for AUX signals, path 1, left-side.
AUX1–	J9	differential I/O	
AUX2+	H6	differential I/O	High-speed differential pair for AUX signals, path 2, left-side.
AUX2–	J6	differential I/O	

Table 2. Pin description *...continued*

Symbol	Ball	Type	Description
DDC_CLK1	H8	differential I/O	Pair of single-ended terminals for DDC clock and data signals, path 1, left-side.
DDC_DAT1	J8	differential I/O	
DDC_CLK2	H5	differential I/O	Pair of single-ended terminals for DDC clock and data signals, path 2, left-side.
DDC_DAT2	J5	differential I/O	
AUX+	H2	differential I/O	High-speed differential pair for AUX or single-ended DDC signals, right-side.
AUX−	H1	differential I/O	
HPD_1	J2	single-ended I/O	Single ended channel for the HPD signal, path 1, left-side.
HPD_2	H3	single-ended I/O	Single ended channel for the HPD signal, path 2, left-side.
HPDIN	J1	single-ended I/O	Single ended channel for the HPD signal, right-side.
VDD	A2, J4	power supply	3.3 V power supply.
GND	B3, C8, G8, H4, H7	ground	Ground.

7. Functional description

Refer to Figure 1 "Functional diagram".

The CBTL06DP211 uses a 3.3 V power supply. All main signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. No clock or reset signal is needed for the multiplexer to function.

The switch position for the main channels is selected using the select signal GPU_SEL. Additionally, the signal DDC_AUX_SEL selects between AUX and DDC positions for the DDC / AUX channel. The detailed operation is described in Section 7.1.

7.1 Multiplexer/switch select functions

The internal multiplexer switch position is controlled by two logic inputs GPU_SEL and DDC_AUX_SEL as described below.

Table 3. Multiplexer/switch select control for IN and OUT channels

GPU_SEL	IN1_n	IN2_n
0	active; connected to OUT_n	high-impedance
1	high-impedance	active; connected to OUT_n

Table 4. Multiplexer/switch select control for HPD channel

GPU_SEL	HPD1	HPD2
0	active; connected to HPDIN	high-impedance
1	high-impedance	active; connected to HPDIN

Table 5. Multiplexer/switch select control for DDC and AUX channels

DDC_AUX_SEL	GPU_SEL	AUX1	AUX2	DDC_CLK1, DDC_DAT1	DDC_CLK2, DDC_DAT2
0	0	active; connected to AUX	high-impedance	high-impedance	high-impedance
0	1	high-impedance	active; connected to AUX	high-impedance	high-impedance
1	0	high-impedance	high-impedance	active; connected to AUX	high-impedance
1	1	high-impedance	high-impedance	high-impedance	active; connected to AUX

7.2 Shutdown function

The CBTL06DP211 provides a shutdown function to minimize power consumption when the application is not active but power to the CBTL06DP211 is provided. Pin XSD (active LOW) puts all channels in off mode (non-conducting high-impedance state) while reducing current consumption to near-zero.

Table 6. Shutdown function

XSD	State
0	shutdown
1	active

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.3	+5	V
T_{case}	case temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	8000	V
		HBM; CMOS inputs	[1]	-	2000	V
		CDM	[2]	-	1000	V
		CDM; CMOS inputs	[2]		500	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3.0	3.3	3.6	V
V_I	input voltage	CMOS inputs		–0.3	-	V_{DD} + 0.3	V
		HPD, DDC/AUX inputs	[1][2]	–0.3	-	V_{DD} + 0.3	V
		other inputs		–0.3	-	+2.6	V
T_{amb}	ambient temperature	operating in free air		–40	-	+85	°C

[1] HPD input is tolerant to 5 V input, provided a 1 kΩ series resistor between the voltage source and the pin is placed in series. See Section 11.1 "Special considerations".

[2] DDC/AUX inputs are tolerant to 5 V input, provided a 2.2 kΩ series resistor between the voltage source and the pin is placed in series. See Section 11.1 "Special considerations".

10. Characteristics

10.1 General characteristics

Table 9. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	operating mode ($\overline{XSD}$ = HIGH); V_{DD} = 3.3 V	-	0.2	1	mA
		shutdown mode ($\overline{XSD}$ = LOW); V_{DD} = 3.3 V	-	-	10	μA
P_{cons}	power consumption	operating mode ($\overline{XSD}$ = HIGH); V_{DD} = 3.3 V	-	-	5	mW
$t_{startup}$	start-up time	supply voltage valid or $\overline{XSD}$ going HIGH to channel specified operating characteristics	-	-	1	ms
t_{rcfg}	reconfiguration time	GPU_SEL or DDC_AUX_SEL state change to channel specified operating characteristics	-	-	1	ms

10.2 DisplayPort channel characteristics

Table 10. DisplayPort channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	+2.6	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage		-	-	1.2	V
DDIL	differential insertion loss	channel is on; f = 100 MHz	-	–1.6	-	dB
		channel is on; f = 1.5 GHz	-	–2.7	-	dB
		channel is off; 0 Hz ≤ f ≤ 1.5 GHz	-	–35	-	dB
DDRL	differential return loss	channel is on; 0 Hz ≤ f ≤ 1.5 GHz	-	–10	-	dB
DDNEXT	differential near-end crosstalk	adjacent channels are on; 0 Hz ≤ f ≤ 1.5 GHz	-	–40	-	dB
B	bandwidth	–3.0 dB intercept	-	2.0	-	GHz
t_{PD}	propagation delay	from left-side port to right-side port or vice versa	-	100	-	ps
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps
t_{sk}	skew time	inter-pair	-	-	180	ps

10.3 AUX and DDC ports

Table 11. AUX and DDC port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	V_{DD} + 0.3	V
V_O	output voltage	no load	-	-	V_{DD}	V
V_{IC}	common-mode input voltage	AUX	0	-	2.0	V
V_{ID}	differential input voltage		-	-	1.4	V
t_{PD}	propagation delay	from left-side port to right-side port or vice versa [1]	-	180	-	ps

[1] Time from DDC/AUX input changing state to AUX output changing state. Includes DDC/AUX rise/fall time.

10.4 HPDIN input, HPD_x outputs

Table 12. HPD input and output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	V_{DD} + 0.3	V
V_O	output voltage	no load	-	-	V_{DD}	V
t_{PD}	propagation delay	from HPDIN to HPD_x or vice versa [1]	-	180	-	ps

[1] Time from HPDIN changing state to HPD_x changing state. Includes HPD rise/fall time.

10.5 GPU_SEL, DDC_AUX_SEL and $\overline{\text{XSD}}$ inputs

Table 13. GPU_SEL, DDC_AUX_SEL, $\overline{\text{XSD}}$ input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{LI}	input leakage current	V_{DD} = 3.6 V; 0.3 V ≤ V_I ≤ 3.9 V	-	-	10	μA

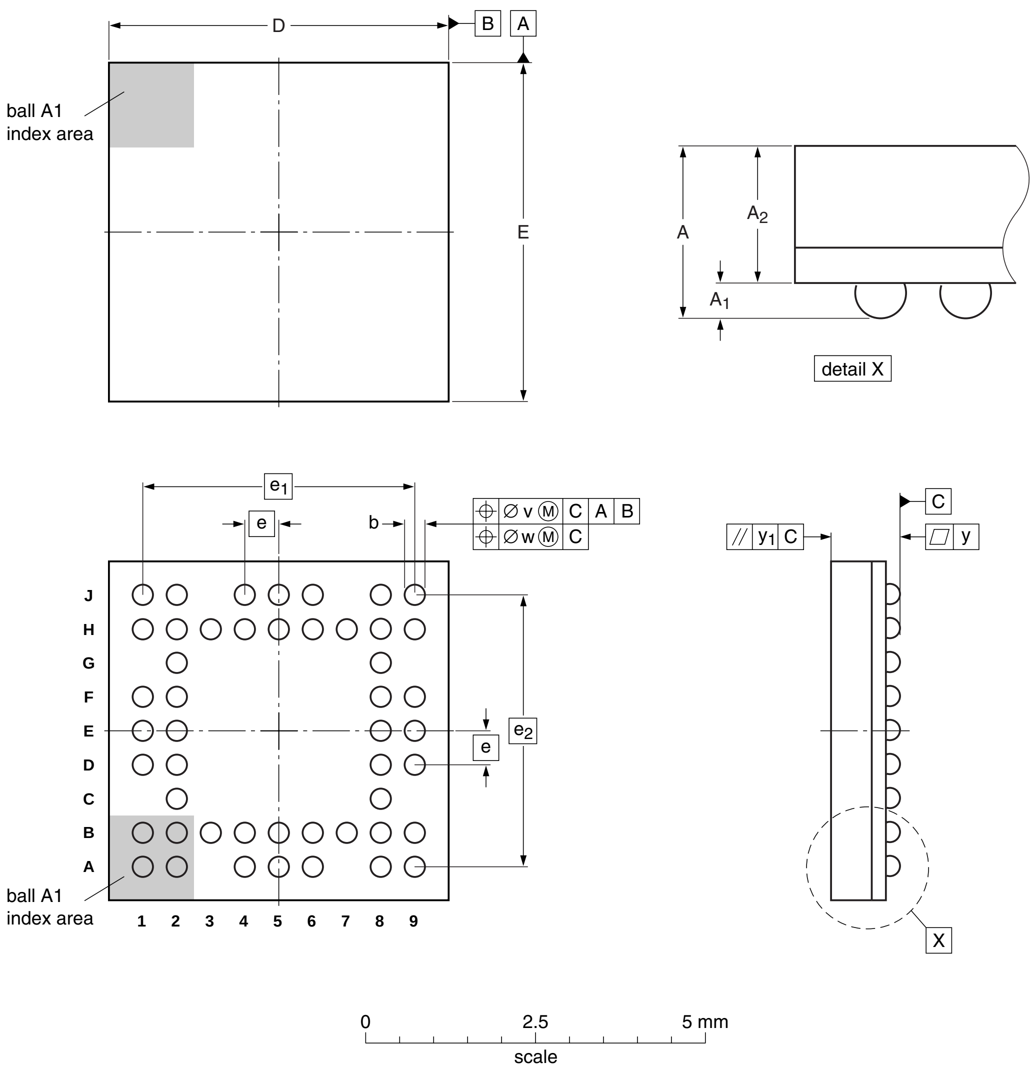
11. Application information

11.1 Special considerations

Certain cable or dongle misplug scenarios make it possible for a 5 V input condition to occur on pins AUX+ and AUX–, as well as HPDIN. When AUX+ and AUX– are connected through a minimum of 2.2 kΩ resistor each, the CBTL06DP211 will sink current but will not be damaged. Similarly, HPDIN may be connected to 5 V via at least a 1 kΩ resistor. (Correct functional operation to specification is not expected in these scenarios.) The latter also prevents the HPDIN input from loading down the system HPD signal when power to the CBTL06DP211 is off.

12. Package outline

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 5 x 5 x 0.8 mm **SOT918-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	5.1 4.9	5.1 4.9	0.5	4	4	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT918-1	- - -	MO-195	- - -			~~05-09-21~~ 05-10-13

Fig 4. Package outline TFBGA48 (SOT918-1)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 5) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020C)

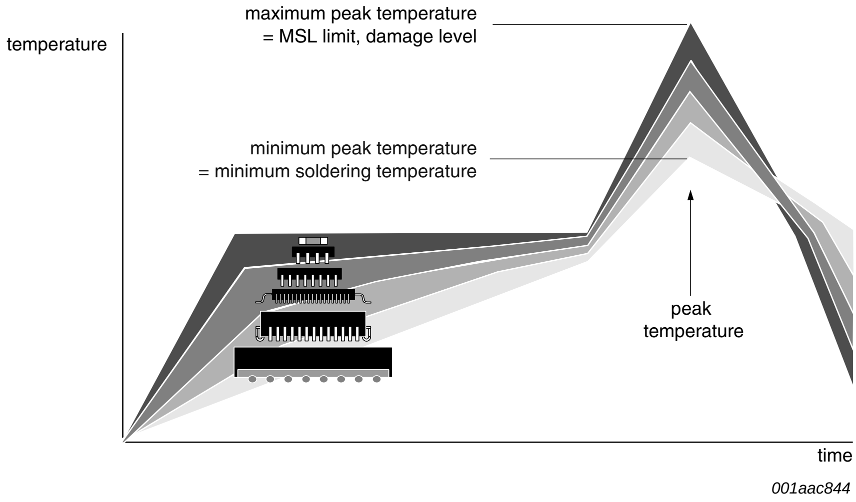
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 5.



MSL: Moisture Sensitivity Level

Fig 5. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 16. Abbreviations

Acronym	Description
AUX	Auxiliary channel (in DisplayPort definition)
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DDC	Display Data Channel
DVI	Digital Video Interface
GPU	Graphics Processor Unit
ESD	ElectroStatic Discharge
HBM	Human Body Model
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I/O	Input/Output

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL06DP211 v.1	20110221	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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